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DARE180U NEW ANALOG IPs

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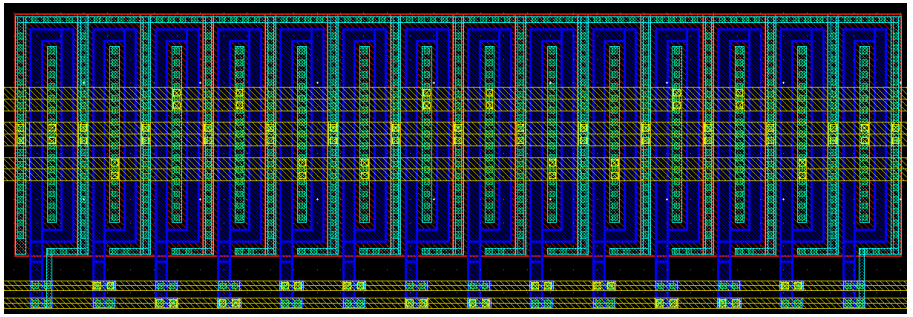
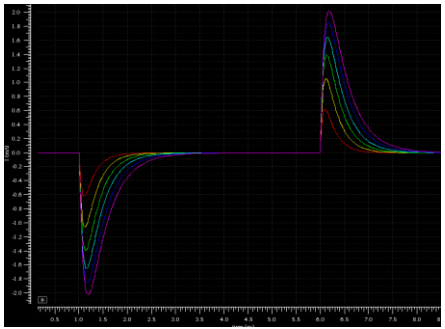
INTRODUCTION

- Technology and context
- High Density Dual Port SRAM
- General Purpose IO (GPIO) with local POC
- Voltage Monitor
- Power-On Reset
- Cristal Oscillator
- Extended Frequency Range PLL
- 11-BIT SAR ADC

TECHNOLOGY/CONTEXT

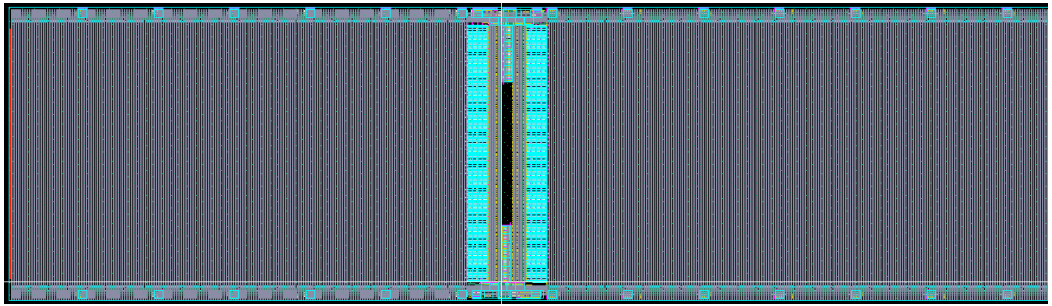
- UMC L180 MM/RF 1.8V/3.3V, Single Poly 6 Metal (1P6M), P-Sub/Twin-Well
- DARE180U platform/ecosystem
  - Single Event model
  - ELT transistor
    - PCELL
    - Enhanced Model (including asymmetry...).
  - ELT aging model
  - RAD layout rule check





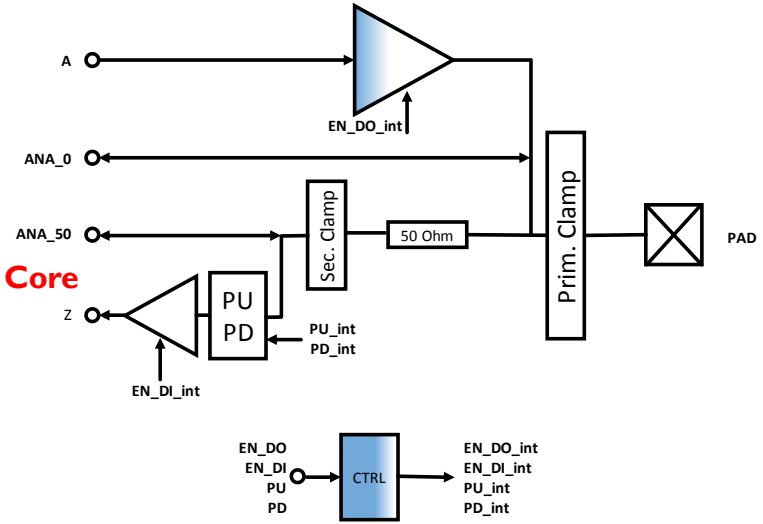
HIGH DENSITY DUAL PORT SRAM (DARE180U_HDRAM)

- High Density Dual port SRAM 4096x13 bits.
  - Clock to output available write: max. 3.8ns
  - Clock to output available read: max. 5.3ns
- Use of straight transistors only.
- Other RAD rules (N area isolation...) enforced.
- Clock tree and address decoder hardened against SET.
- Word bit's separation of 57µm (hardening versus MBU)
- Designed SEL free till 80 MeV*cm^2/mg
- Area reduction: 50%



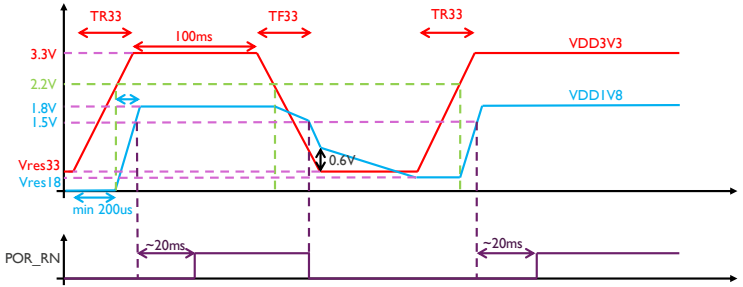
GENERAL PURPOSE IO (GPIO) WITH LOCAL POC (DARE180U_GPIO)

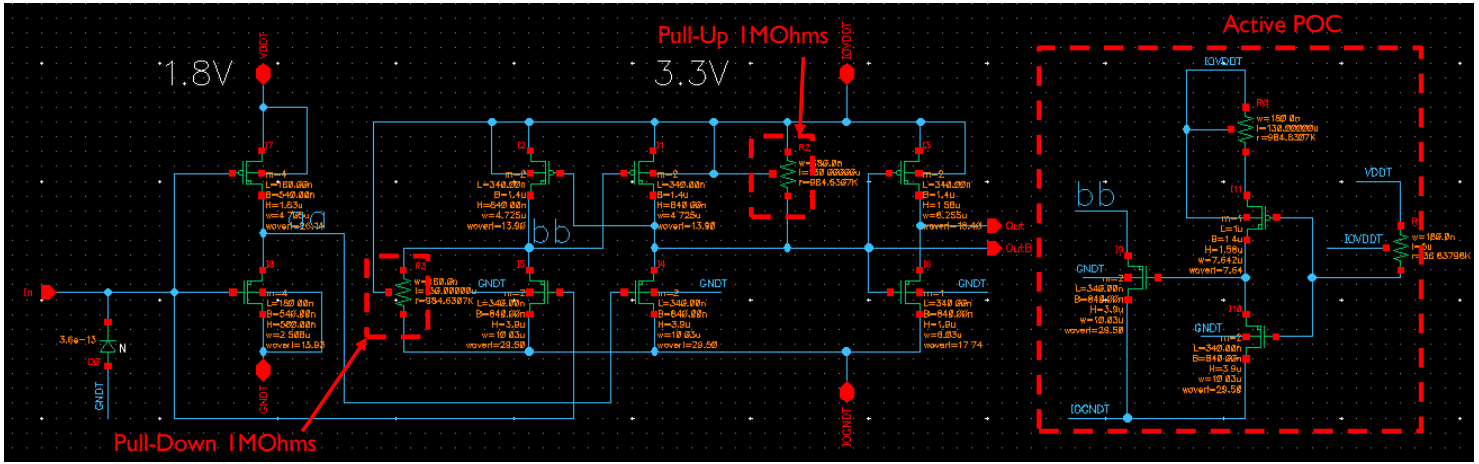
- Digital input (Schmitt trigger) with programmable pull-up/pull-down
- Digital output (4mA drive)
- Analog input (serial impedance of 50 Ohms with secondary ESD protection)
- Analog output
- Designed SEL and SET free till respectively 80 and 60 MeV*cm^2/mg



GENERAL PURPOSE IO (GPIO) WITH LOCAL POC (DARE180U_GPIO)

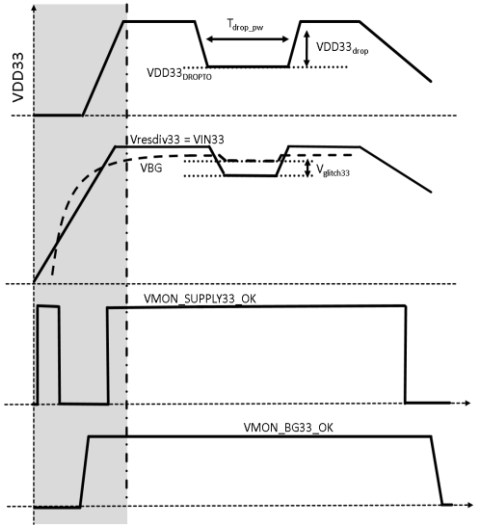
- Local Power On Control (POC) to prevent glitches during the power ramp-up and the power ramp-down

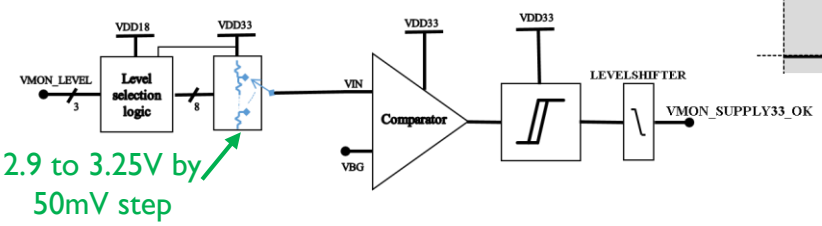


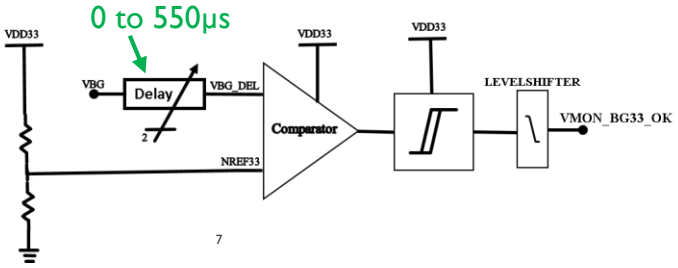


VOLTAGE MONITOR (DARE180U_VMON)

- 3.3V voltage monitor
  - 3 bits to setup the detection level from 2.9V till 3.25V (step of 50mV)
  - Glitches filtering (20µs)
  - Designed SEL and SET free till respectively 80 and 60 MeV*cm^2/mg
  - Hysteresis
  - Combined with BG_OK

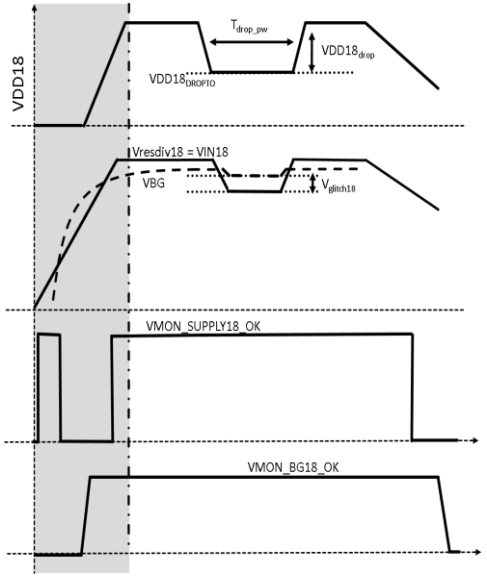


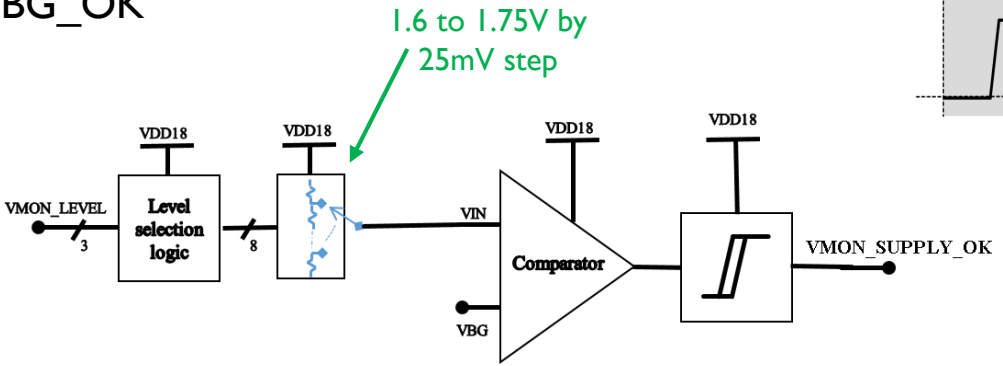




VOLTAGE MONITOR (DARE180U_VMON)

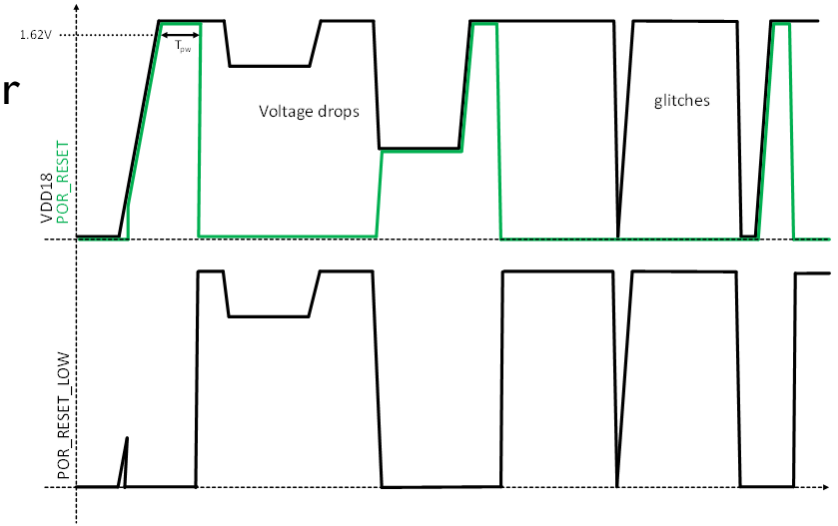
- 1.8V voltage monitor
  - 3 bits to setup the detection level from 1.6V till 1.75V (step of 25mV)
  - Glitches filtering (20µs)
  - Designed SEL and SET free till respectively 80 and 60 MeV*cm²/mg
  - Hysteresis
  - Combined with BG_OK

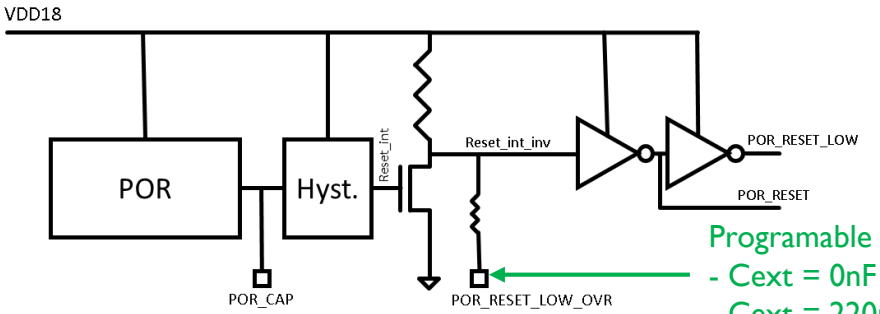




POWER-ON RESET (DARE180U_POR)

- 1.8V detection
- Programable reset pulse with external capacitor
- Designed SEL and SET free till respectively 80 and 60 MeV*cm^2/mg

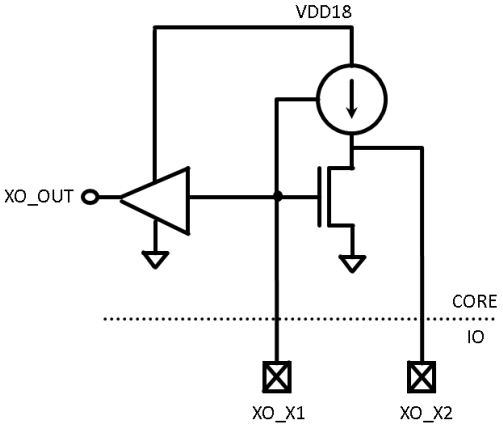


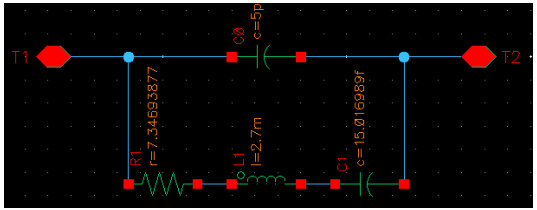


Programable pulse width:
- Cext = 0nF => 235µs typ
- Cext = 220nF => 150ms typ

CRISTAL OSCILLATOR (DARE180U_XO)

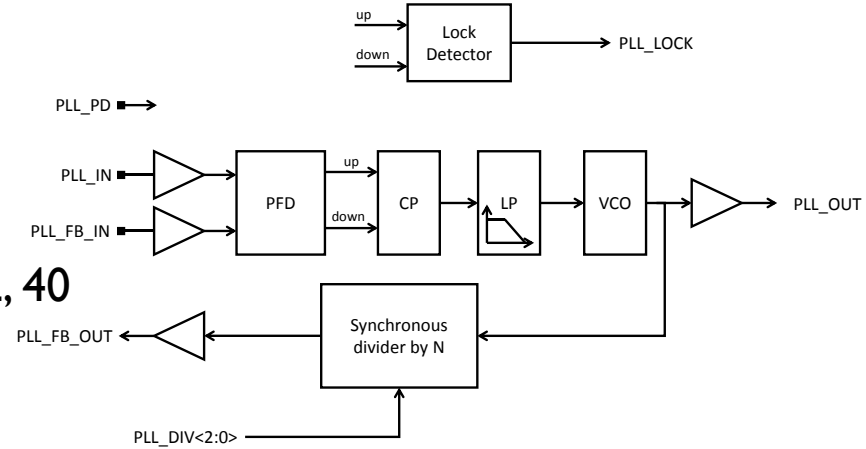
- Frequency range:
  - 5MHz (Rakon crystal ESCC 3501/019), 100µA typ., 18 ppm, startup time 1.4ms typ.
  - 25MHz (Rakon crystal ESCC 3501/01/8), 450µA typ., 11 ppm, startup time 1.8ms typ.
- Designed SEL free till 80 MeV*cm^2/mg
- Designed SET free till 60 MeV*cm^2/mg:
  - No double edge
  - Max. 1.1ns phase error at 25 MHz (~2% phase error)
  - Max. 3.8ns phase error at 5MHz (~2% phase error)





EXTENDED FREQUENCY RANGE PLL (DARE180U_PLL_EXT)

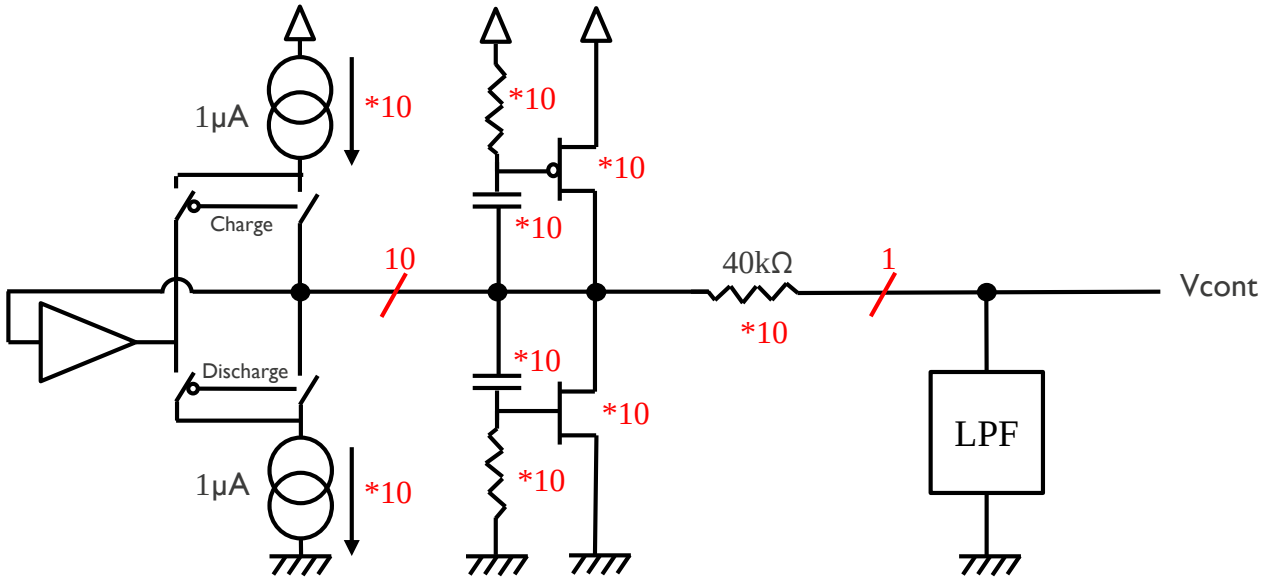
- VCO frequency range 280MHz till 400MHz
- Designed SEL free till 80 MeV*cm^2/mg
- Designed SET free till 60 MeV*cm^2/mg:
  - No double edge
  - Max. 160ps phase error @F_{VCO} = 400 MHz
  - Max. 600ps phase error @F_{VCO} = 280 MHz
- Programmable frequency division: 8, 16, 20, 32, 40 and 80.
- Thermal jitter: 1ps typ



EXTENDED FREQUENCY RANGE PLL (DARE180U_PLL_EXT)

HARDENING

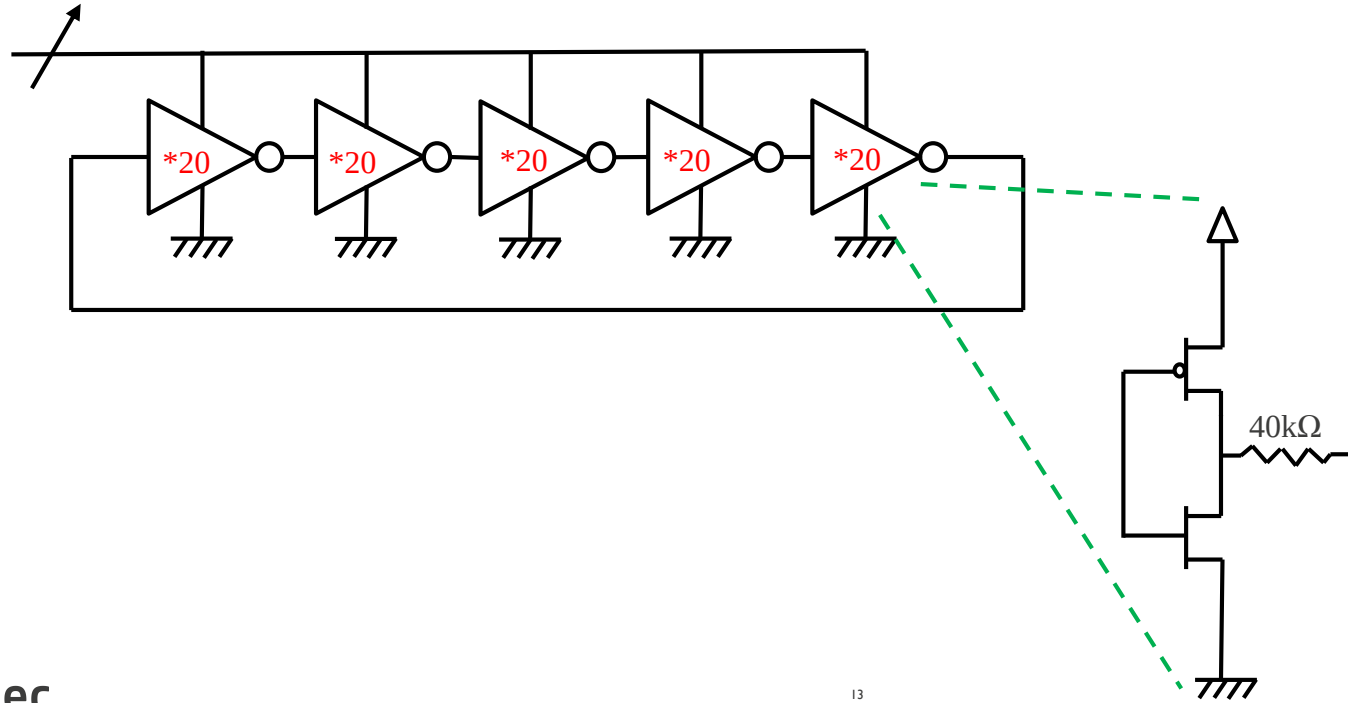
- PFD: by drive strength
- Synchronous divider: triplication with reset after each cycle (state-machine)
- Charge Pump: current limitation combined with clamp



EXTENDED FREQUENCY RANGE PLL (DARE180U_PLL_EXT)

HARDENING

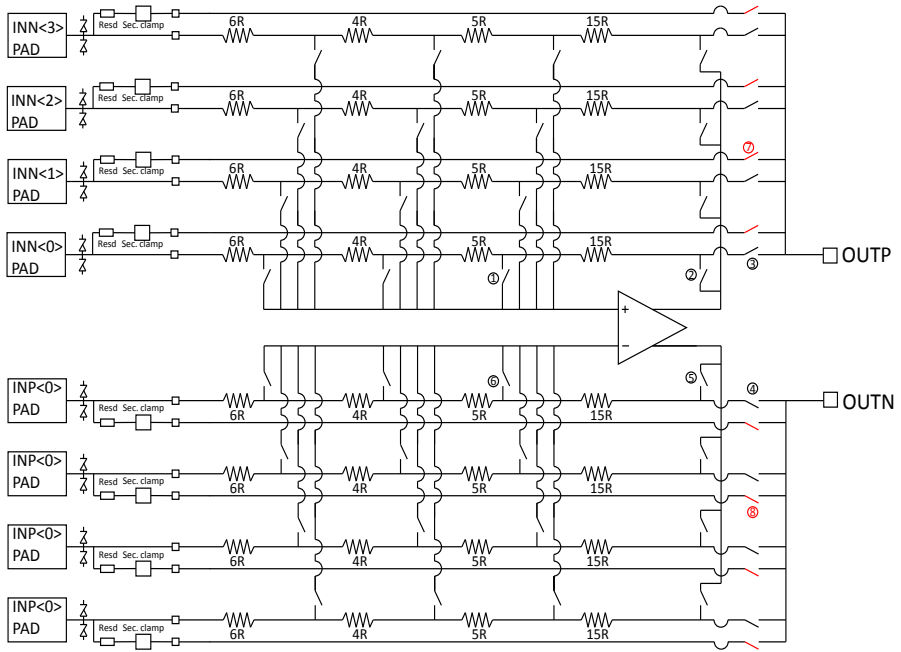
- VCO: analog averaging



11-BIT SAR ADC (DARE180U_ADC)

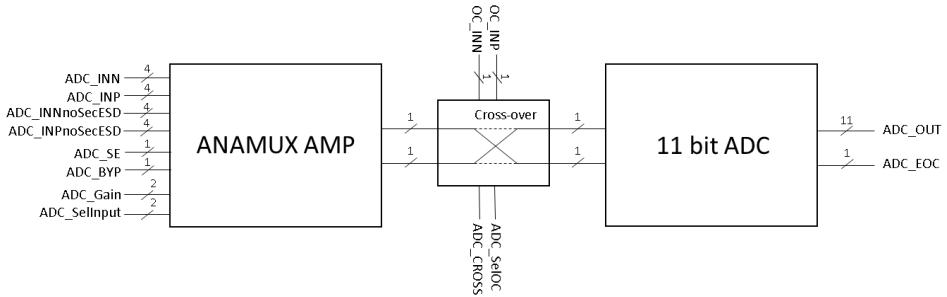
- 8:2 analog mux
  - Bypass
  - Auto zeroed differential amplifier (0dB, 6dB and 12dB).
  - Wide input common mode
  - Hardening: SET simulation result?

Gain [dB]	Min input CM [V]	Max input CM [V]	| INP<i> - INN<i> | [V]
0	0	VDDA	2
6	VDDA/8	7/8*VDDA	1
12	3/16*VDDA	13/16*VDDA	0.5



11-BIT SAR ADC (DARE180U_ADC)

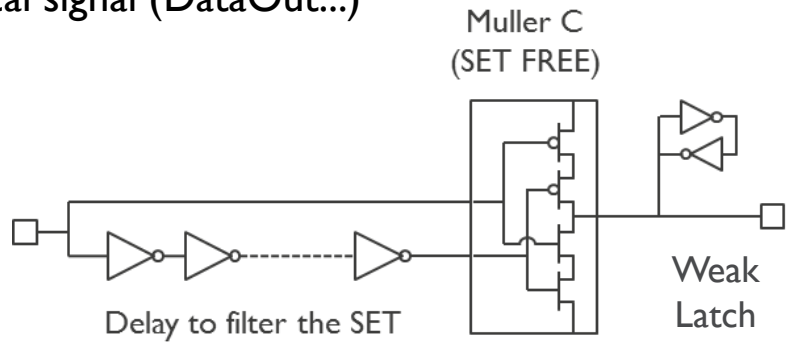
- SAR ADC configurable in differential or single-ended mode (11-bit interface, ENOB WC of 10 bits at 300kS/s)
- Internal voltage reference (external capacitor free)
- Auto zeroed comparator
- Total current consumption 5mA (including analog-mux amplifier)



11-BIT SAR ADC (DARE180U_ADC)

HARDENING

- Designed SEL free till 80 MeV*cm^2/mg
- Digital hardening by:
  - drive strength for the critical combinatorial gates
  - Use of Hit FF
  - Signal driving switches of the capa-bank are not hardened: the SET is filtered by the limited bandwidth
  - Muller-C filter for the non critical signal (DataOut...)



11-BIT SAR ADC (DARE180U_ADC)

HARDENING

- Comparator hardening:
  - Use an auto-zeroed architecture => don't need big input transistor
  - Comparator cross section of 80µm^2 @0.1 MeV*cm^2/mg for an error of 1 LSB
- Capa-bank hardening
  - Total capa-bank switches area: 240µm^2
  - Cunit = 12.5 fF
  - ➢ SEU of 1 LSB correspond to 0.6 MeV*cm^2/m

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