# Re-Thinking Reliability Analysis

Art Schaldenbrand, Cadence Design Systems

7th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA)
Session: Evaluation and Qualification
June  2018, Leuven Belgium

# Agenda

- The Challenge
- Modeling Device Degradation
- Advanced Aging Analysis
- Mission Profiles
- Conclusion

# The Challenge

# Semiconductor Requirements for Heterogenous Applications

## By market segment

| | *Consumer* | *Industrial* | *Automotive* | |
|---|---|---|---|---|
| Temperature | 0°C → 40°C | -10°C → 70°C | -40°C → 85°C/155°C | Reliability |
| Lifetime | 1-3 years | 5-10 years | > 15 years | Reliability |
| Test Coverage | ~ 95% | ~99% | Target = 0 dppm | Availability (Quality) |
| Safety Rating | ? | ASIL B | ASIL C, D | Safety |



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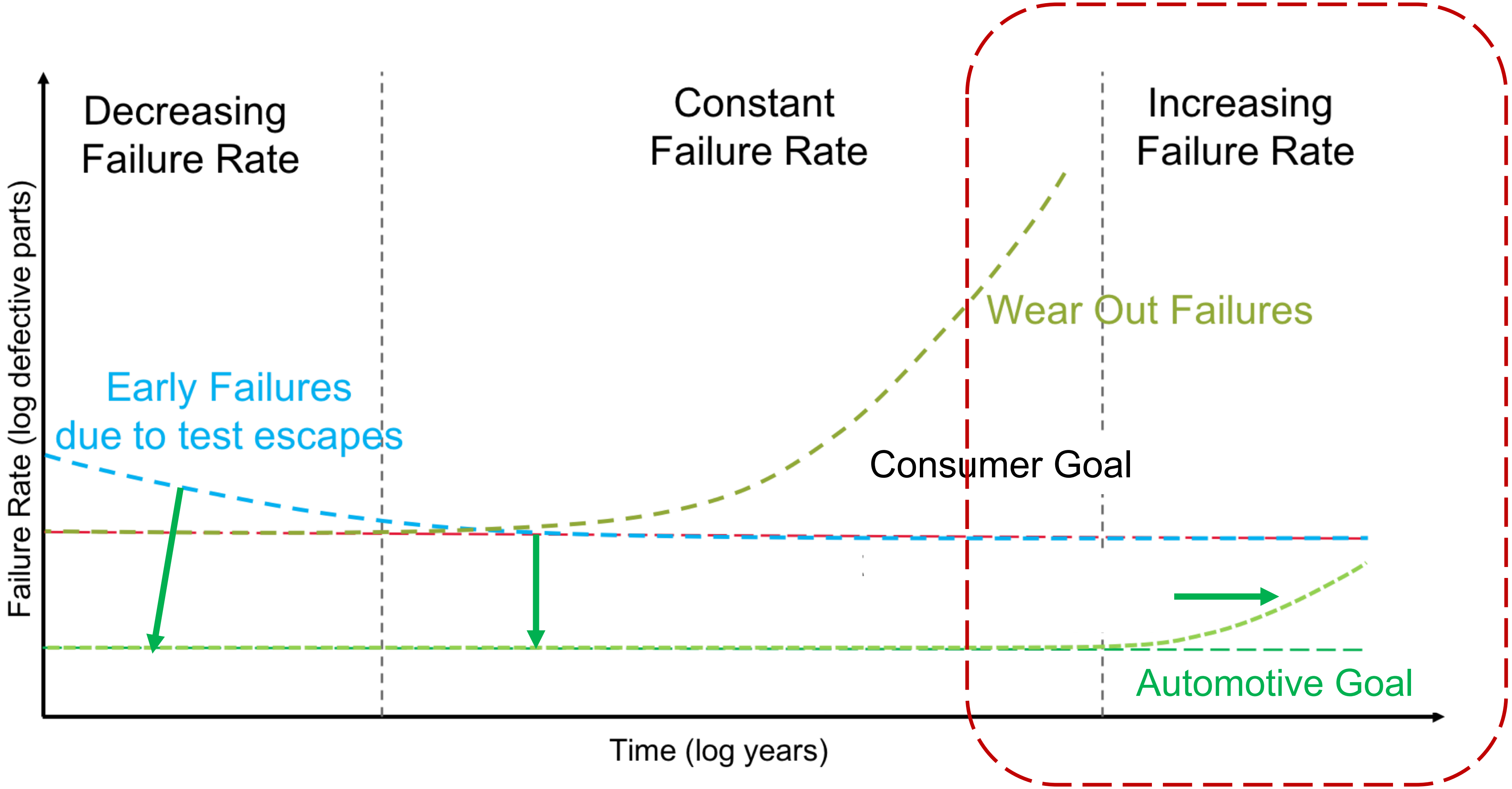
# The Challenge

## Multi-dimensional management of failure rate over product lifetime



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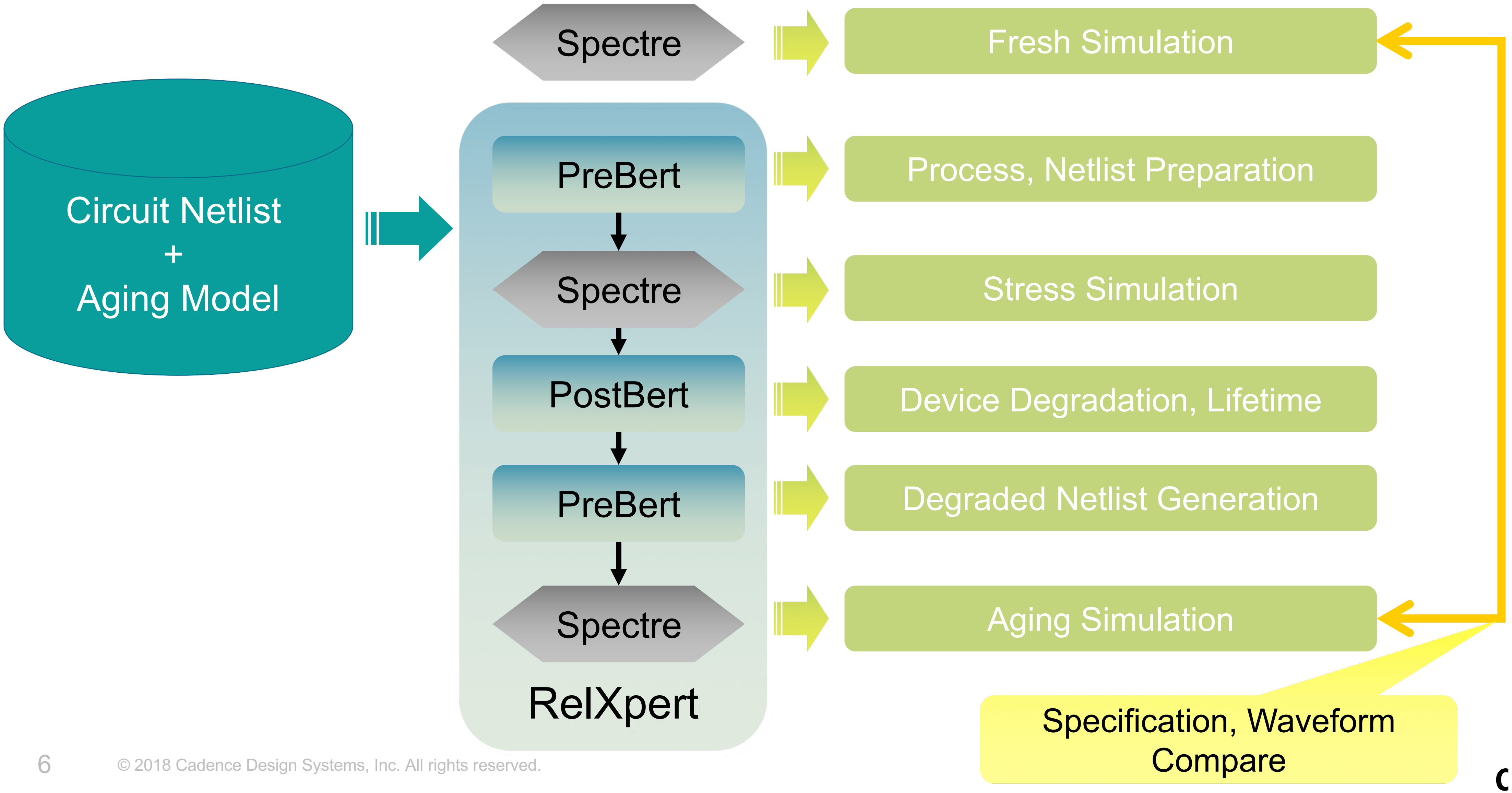
# RelXpert Integrated Reliability Analysis

## HCI and NBTI analysis flow



# Evolution of Aging Analysis

## *Inputs*

Circuit Netlist
+
Device Model

Reliability Model

Mission Profile
- Temp
- On/Off time
- Burn-in

## *Analysis*

Aging Analysis

Self-Heating Analysis

Extended Modeling

Monte Carlo Analysis

## *Outputs*

- Device/age information
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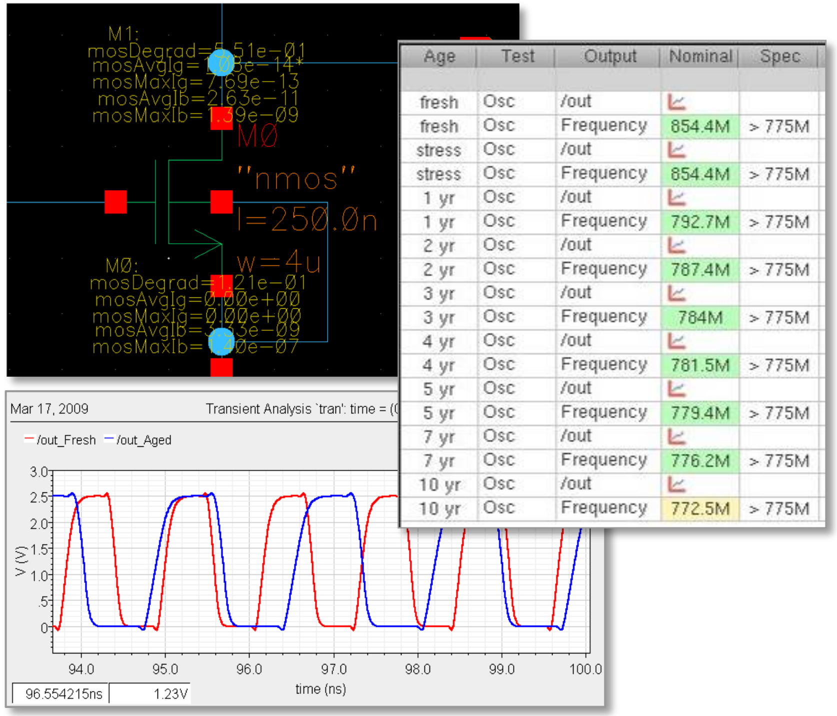


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# Modeling Device Degradation



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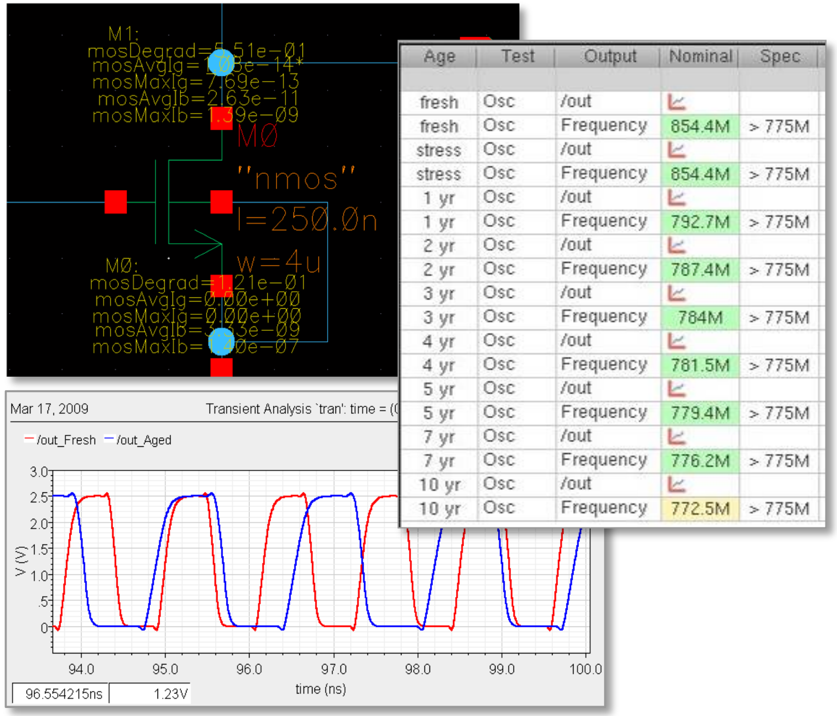

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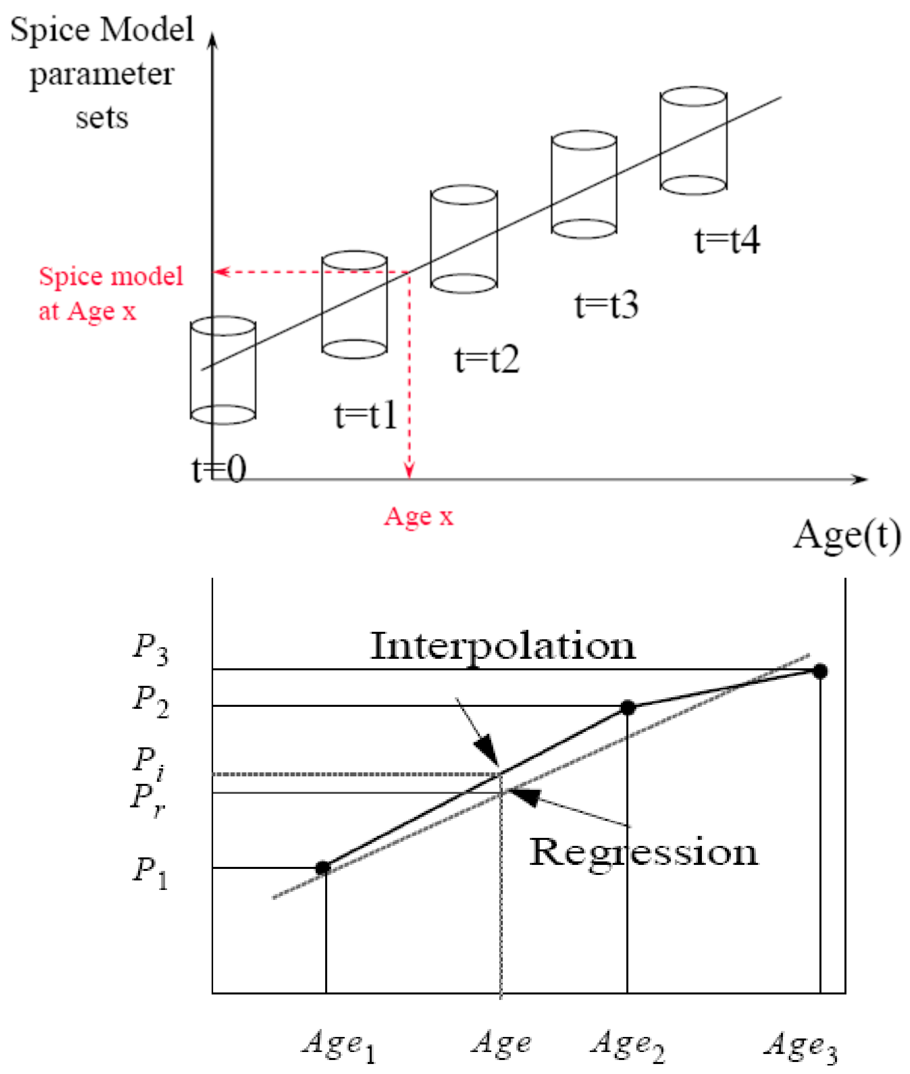
# Degraded Model Sets

- Degraded model sets represent device aging by separate model cards for each device age, time point
  - For example: separate model cards for a transistor after 0 years, 1 year, 5 year, 10 year, …
- Model parameters are interpolated to estimate the effect of degradation for device ages between the specified model ages



# AgeMOS Model

- The AgeMOS model enables reliability analysis of HCI and NBTI circuit reliability simulation
  - ΔP=f(P0,age,d1, d2, n1, n2, s )
  - Replaces degraded model sets
  - No interpolation, keeps the aged parameters monotonic

$$\Delta D(t) = f(Age)$$

$$Age = \int_0^T A dt$$

$$A = f(V_{gs}, V_{ds}, V_{bs}, W, L, V_t, \ldots)$$

$$t = D(A)^{-n}$$

- Degraded Example

```
*relxpert: +hd1_vth0 = 4.5 hd2_vth0 = 0 hn1_vth0 = 0.3 hn2_vth0 = 0.36488 hs_vth0 = 1.2777
*relxpert: +hd1_ua = 0.11812 hd2_ua = 13.12 hn1_ua = 0.2684 hn2_ua = 0.50428 hs_ua = 3
*relxpert: +hd1_ub = 372.6 hd2_ub = 1 hn1_ub = 0.44 hn2_ub = 1 hs_ub = 1
*relxpert: +hd1_a0 = 0.40162 hd2_a0 = 0 hn1_a0 = 0.08392 hn2_a0 = 1 hs_a0 = 1
*relxpert: + age = 1e-12
```

- AgeMOS Example

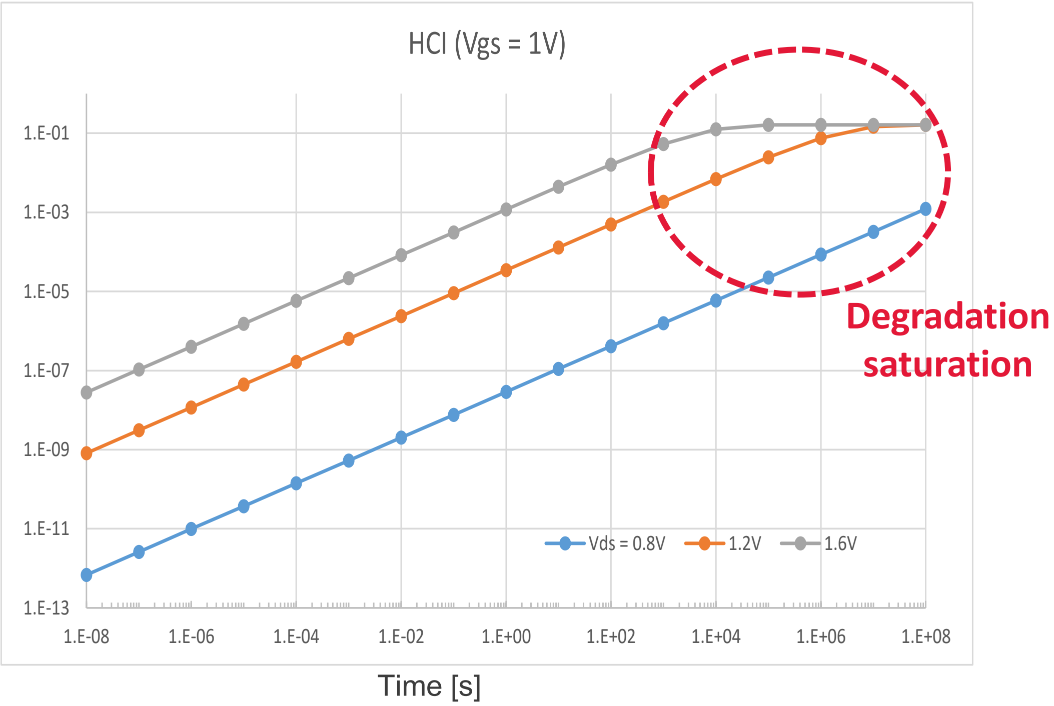
```
.MODEL nchan nmos level = 49
+ vt0 = 0.7 u0 = 450 tox = 180
* Above line specifies fresh SPICE parameters
*relxpert: + age_level = 0 <<<<HCI parametes
*relxpert: + hd1_vth0 = 4.5 hd2_vth0 = 0 hn1_vth0 = 0.3 hn2_vth0 = 0.36488
*relxpert: + age_level = 1 <<<<NBTI parameters
*relxpert: + nn1_a0 = 1.0 nn1_nfactor = 1.0 nn1_pclm = 1.0 nn1_u0 = 1.0
```

# New Generation Reliability Model

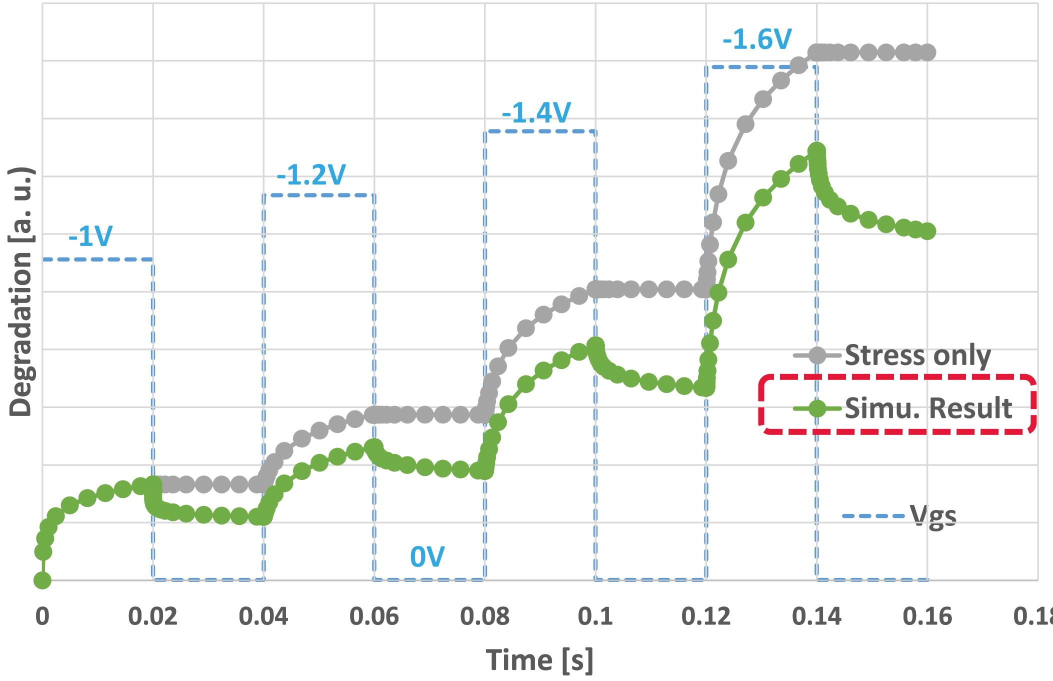
## MOS-AK December 2016 [9]

- New and improved physics-based model suitable for advanced node and legacy node modeling has been developed for better prediction of device degradation
  - Change in device parameters can be estimated from the environmental, operating conditions, and device size

HCI model with saturation effect




BTI model with recovery effect



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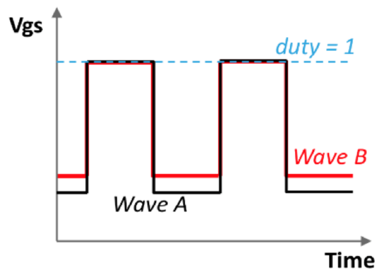
# New Generation Reliability Model

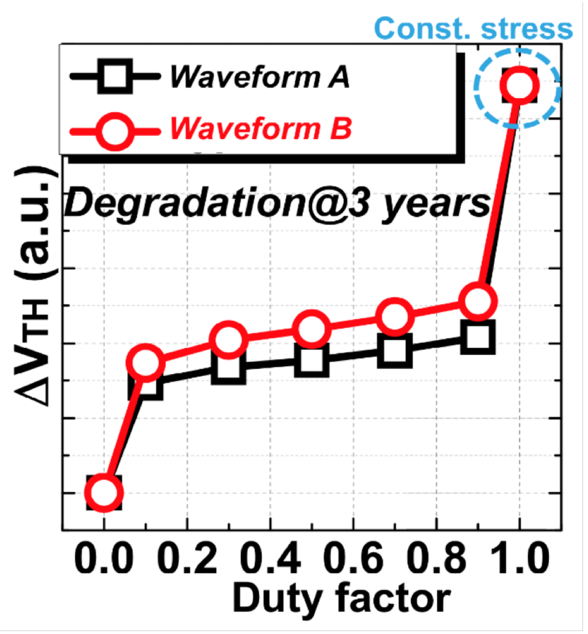
## NBTI modeling

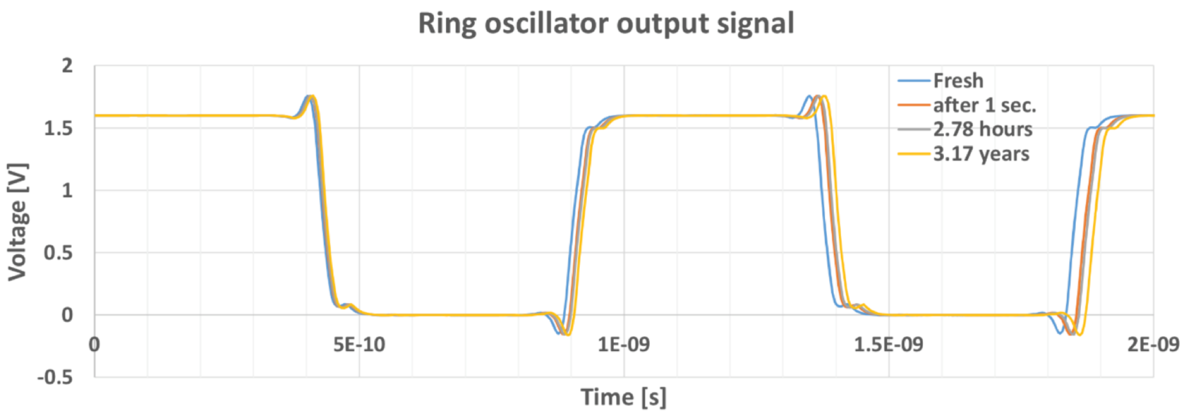
- NBTI stress-recovery dynamic processes originate from trapping and de-trapping mechanism
- Two kinds of traps - fast and slow - contribute to FinFET NBTI
- Activation energies and voltage-accelerated factors in both stress and recovery stages differ for each trap type
- Results differ for short-term and long-term NBTI behavior in FinFET




The duty cycle is varied from 0% to 100% for two gate bias waves with different recovery bias values.

When duty = 100%, a constant stress bias is applied.



# Advanced Aging Analysis

# Evolution of Aging Analysis

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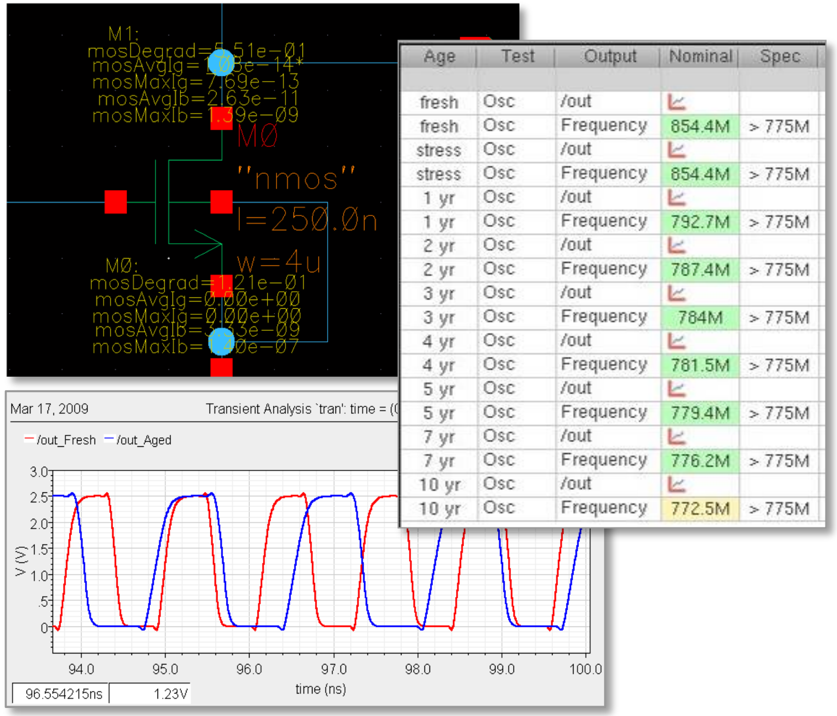


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# Simulating Aging with Device Self-Heating Effect

## Three-step aging with self-heating flow

**Calculate Power**

- Simulate the fresh performance
- Calculate power and average temperature rise for each device

**Calculate Stress with $T_{rise}$**

- Updates the temperature, $T_{rise}$, for each device
- Simulate the electrical stress

**Calculate Aging with $T_{rise}$**

- Age parameters of each device based on degradation
- Simulate including aging and self-heating

# Simulating the Effect of Self-Heating on Aging

| | | Temperature Rise | Device Degradation | | | | |
|---|---|---|---|---|---|---|---|
| Rank | Instance | $d_{temperature}$ | diVdsat(HCI+BTI, %) | diIdlin(HCI+BTI, %) | | dvtlin(HCI+BTI, V) | |
| 1 | I1.M0 | 3.532e+00 | 5.934e+00 | 4.355e+00 | 1.265e-02 | 1.852e-01 | 1.366e-01 |
| 2 | I0.M0 | 8.363e-01 | 5.803e+00 | 4.259e+00 | 1.238e-02 | 2.504e-01 | 1.847e-01 |
| 3 | I12.M0 | 7.923e-01 | 5.742e+00 | 4.214e+00 | 1.224e-02 | 2.383e-01 | 1.758e-01 |
| 4 | I9.M0 | 1.357e+00 | 5.594e+00 | 4.106e+00 | 1.193e-02 | 2.097e-01 | 1.547e-01 |
| 5 | I8.M0 | 7.633e-01 | 5.556e+00 | 4.078e+00 | 1.185e-02 | 2.029e-01 | 1.497e-01 |
| 6 | I11.M0 | 8.770e-01 | 5.495e+00 | 4.033e+00 | 1.172e-02 | 2.179e-01 | 1.608e-01 |
| 7 | I4.M0 | 1.605e+00 | 5.437e+00 | 3.990e+00 | 1.159e-02 | 1.942e-01 | 1.433e-01 |
| 8 | I6.M0 | 1.218e+00 | 5.409e+00 | 3.970e+00 | 1.153e-02 | 1.694e-01 | 1.250e-01 |




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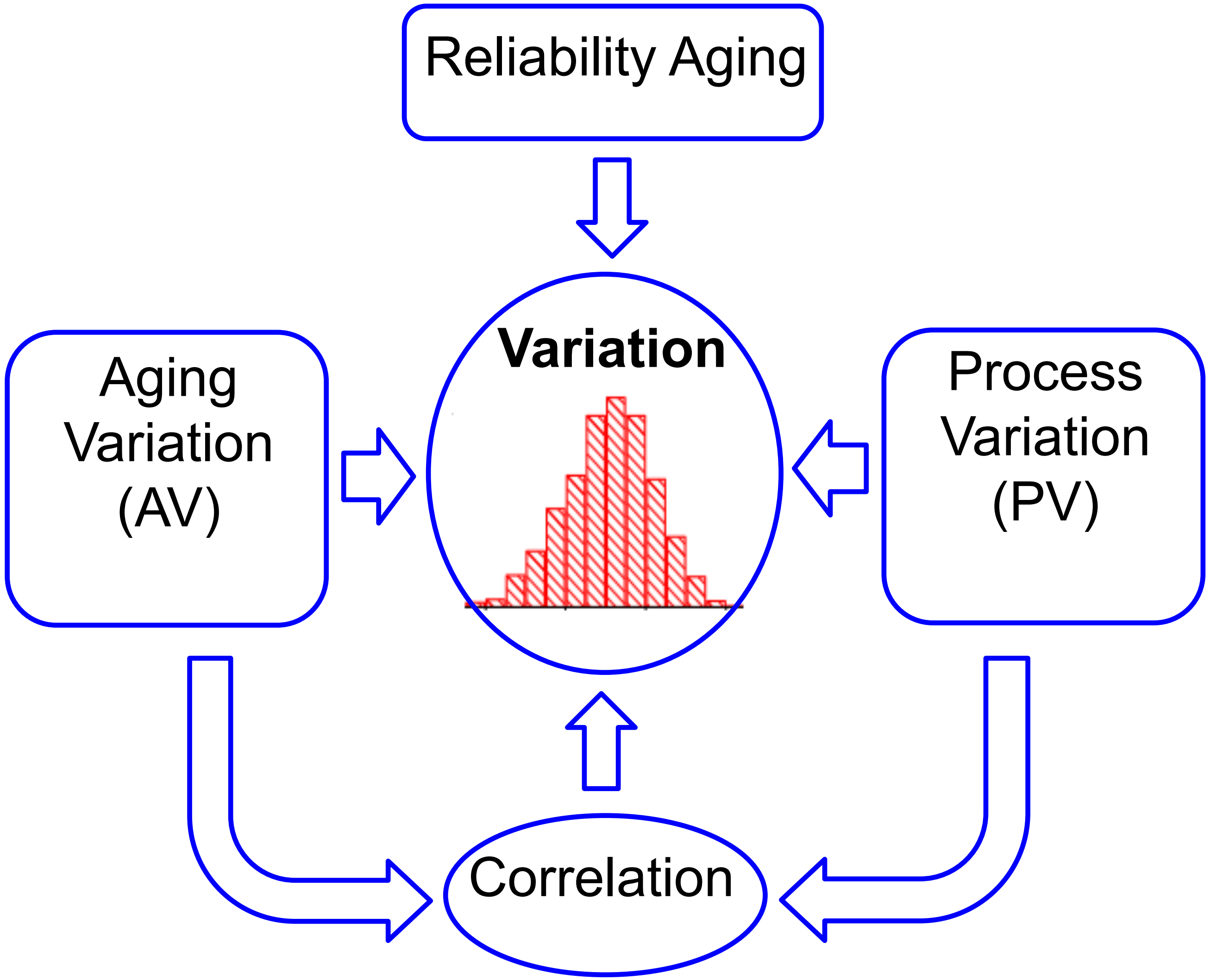
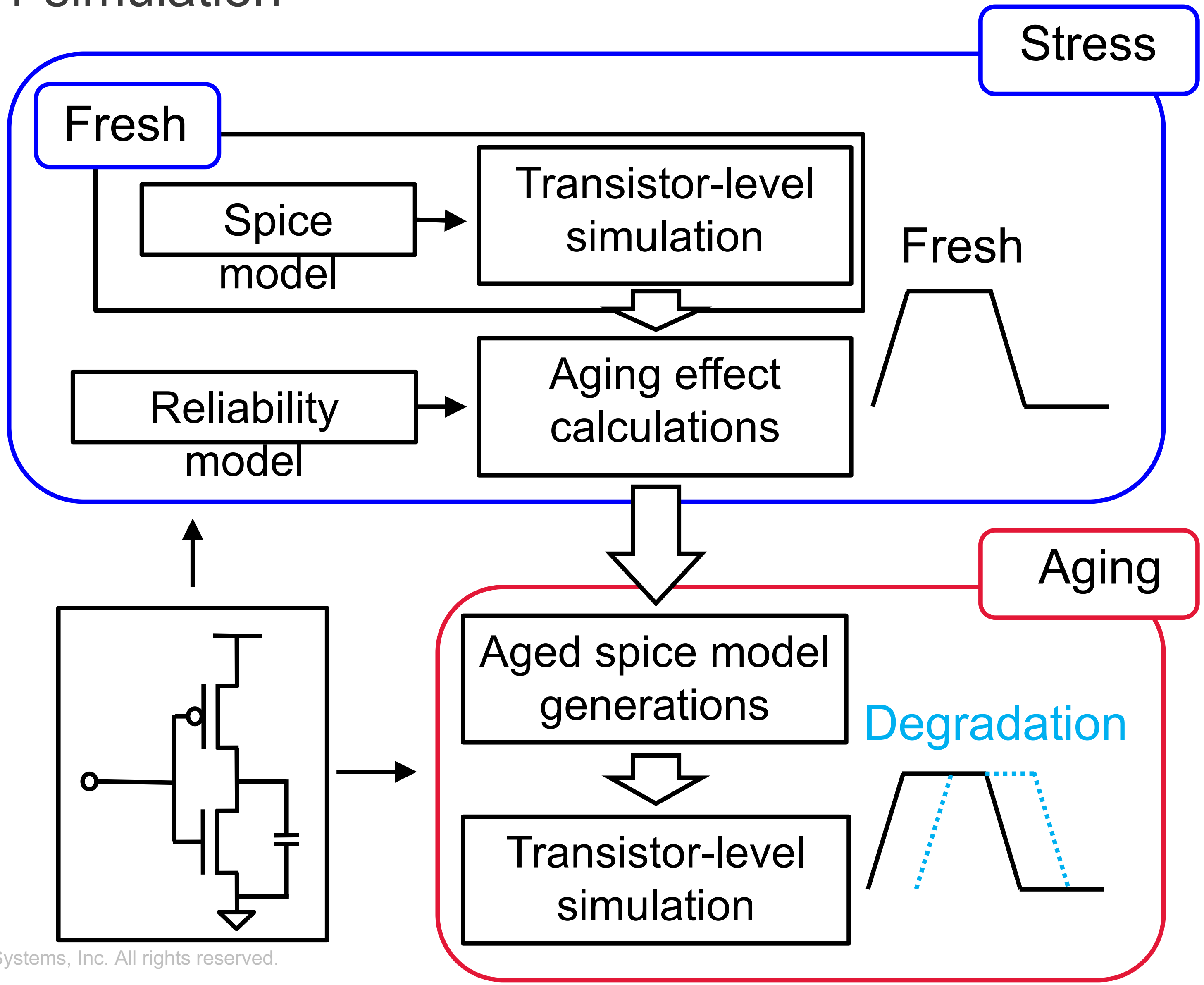
# Monte Carlo Based Reliability Variation Analysis

## IDEM 2015 [11]



# Aging Acceleration due to Process Variation

## RelXpert Flow, 1 simulation



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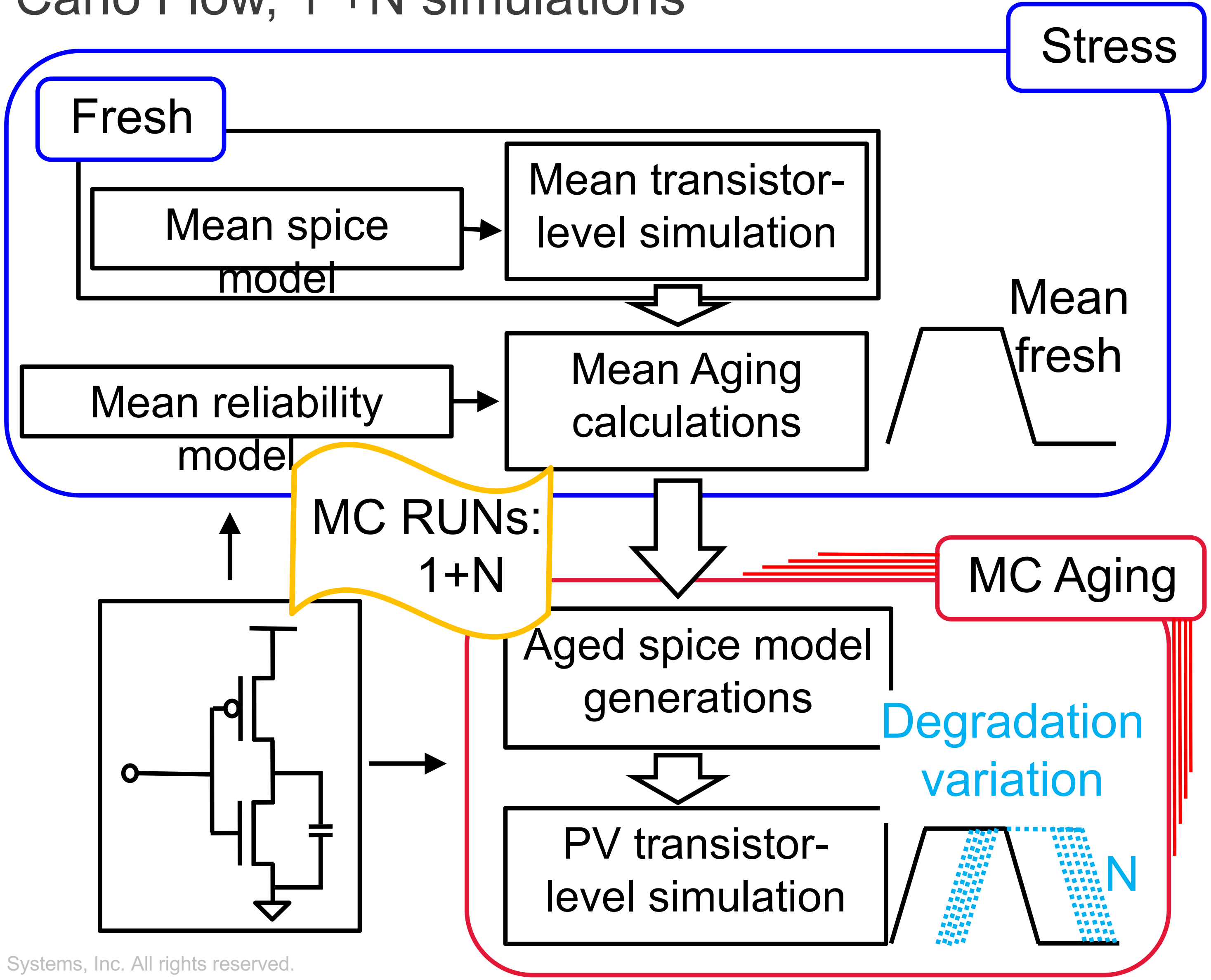
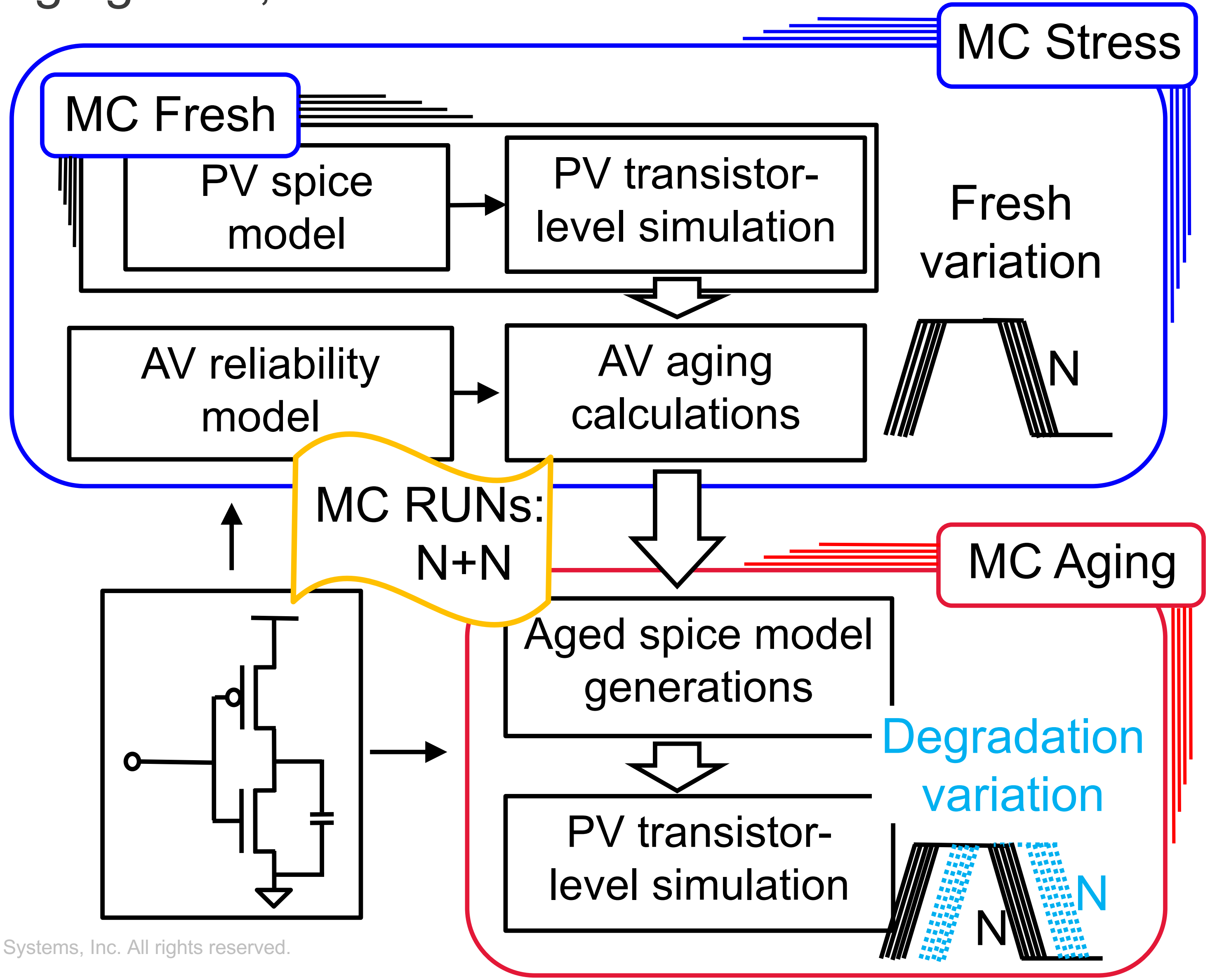
# Aging Acceleration due to Process Variation

## Aging + Monte Carlo Flow, 1 +N simulations



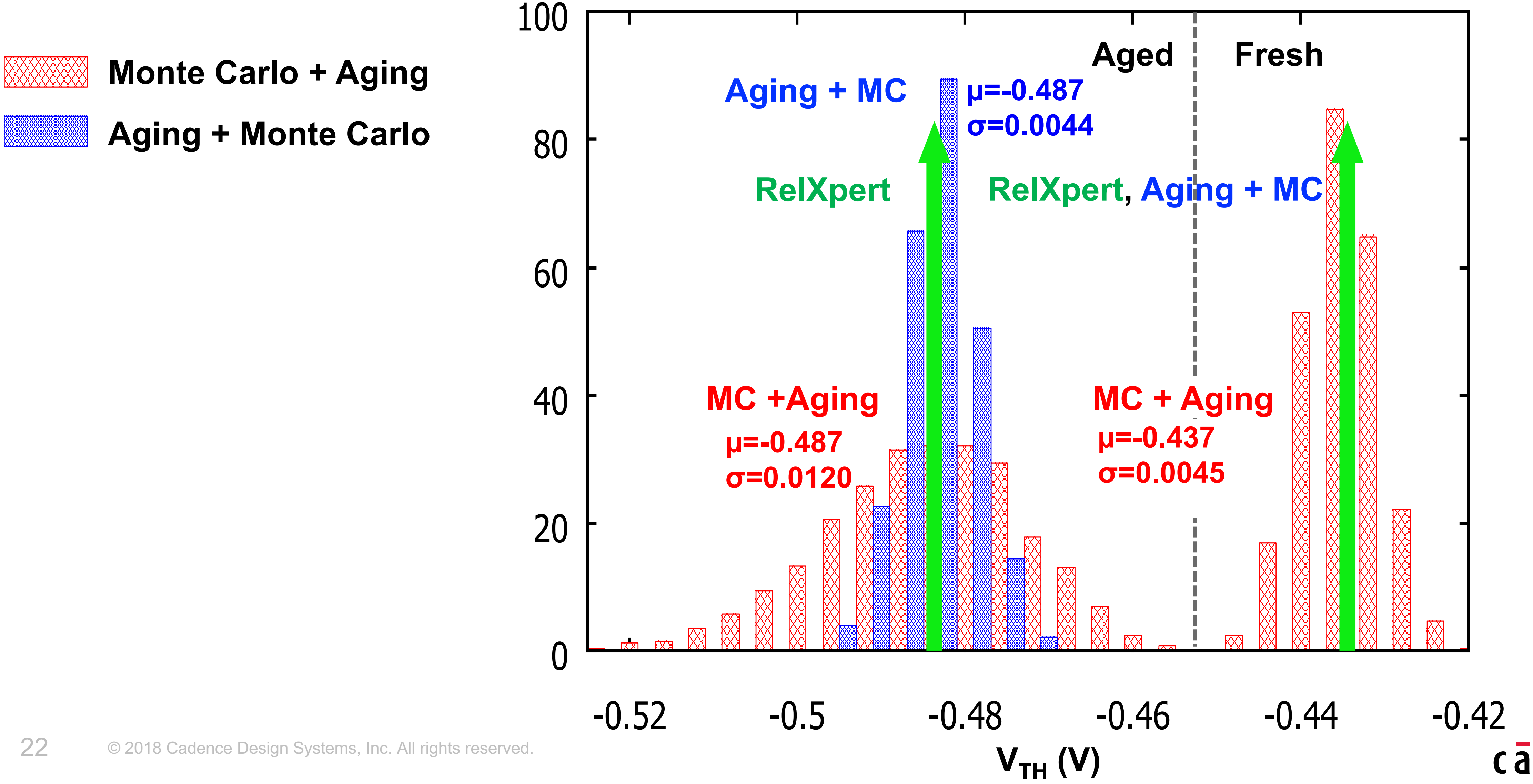
# Aging Acceleration due to Process Variation

## Monte Carlo + Aging Flow, N + N simulations



# $V_{TH}$ Comparison between Flows

## RelXpert, Aging + Monte Carlo (1+N), Monte Carlo + Aging (N+N)



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# Mission Profiles

# Evolution of Aging Analysis

## *Inputs*

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## *Analysis*

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## *Outputs*

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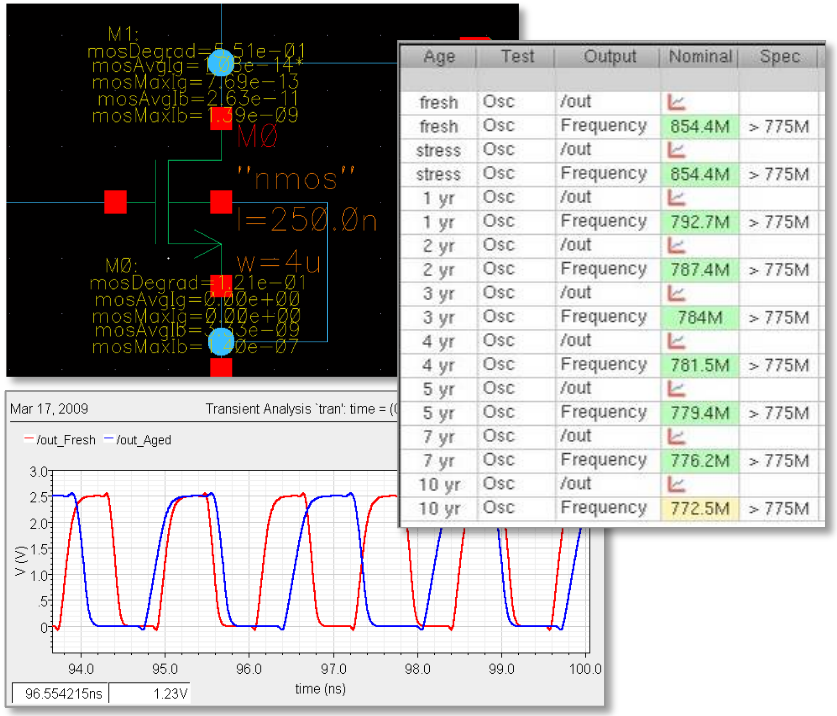


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# Gradual Aging Simulation

- Traditionally aging analysis performs a single stress simulation and extrapolated until the end of life
- Approach works well if aging does not effect circuit operating point
- Gradual Aging is an extension to aging analysis that breaks the aging period up into multiple intervals
  - More accurate
  - More expensive, requires more simulation
- Multi-stress simulation is another option
  - Simulate lifetime over burn-in + operation

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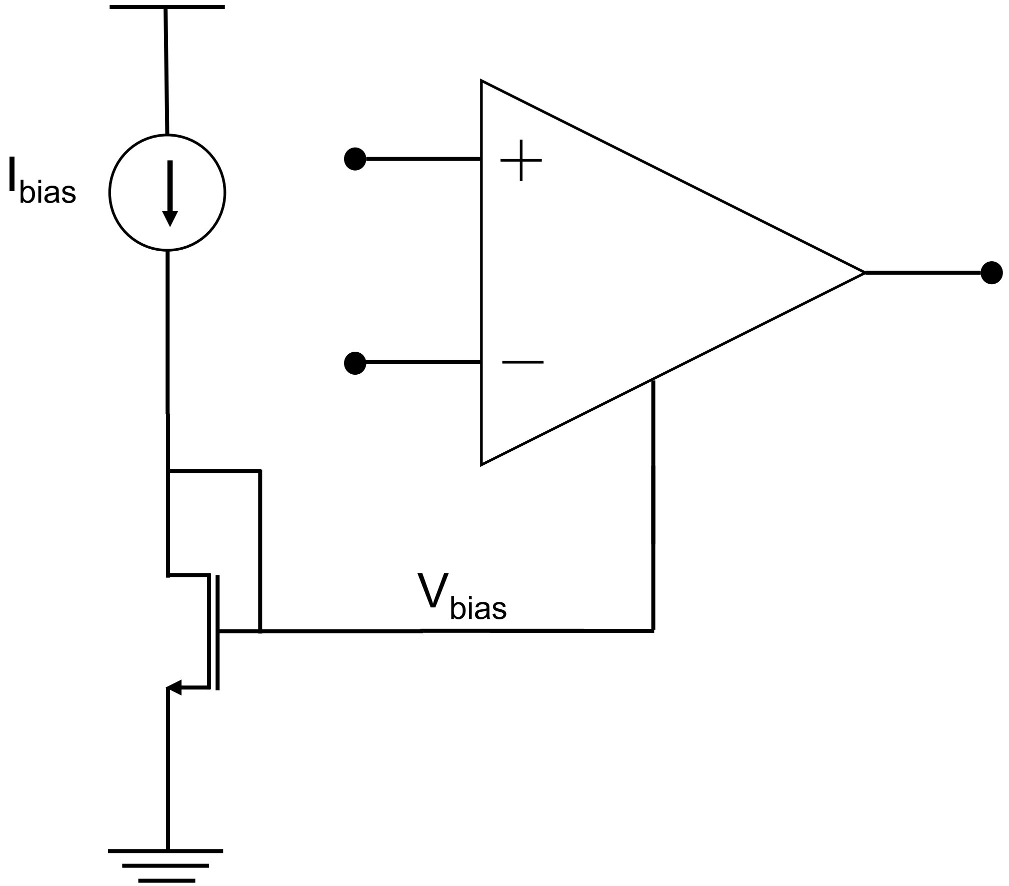
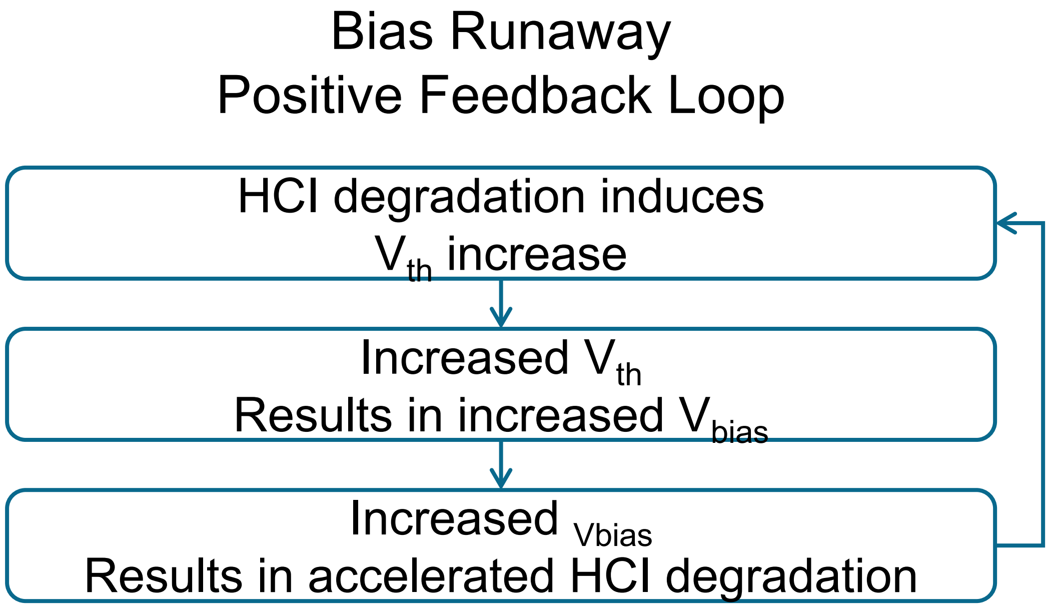
# Accelerated Aging due to Bias Runaway

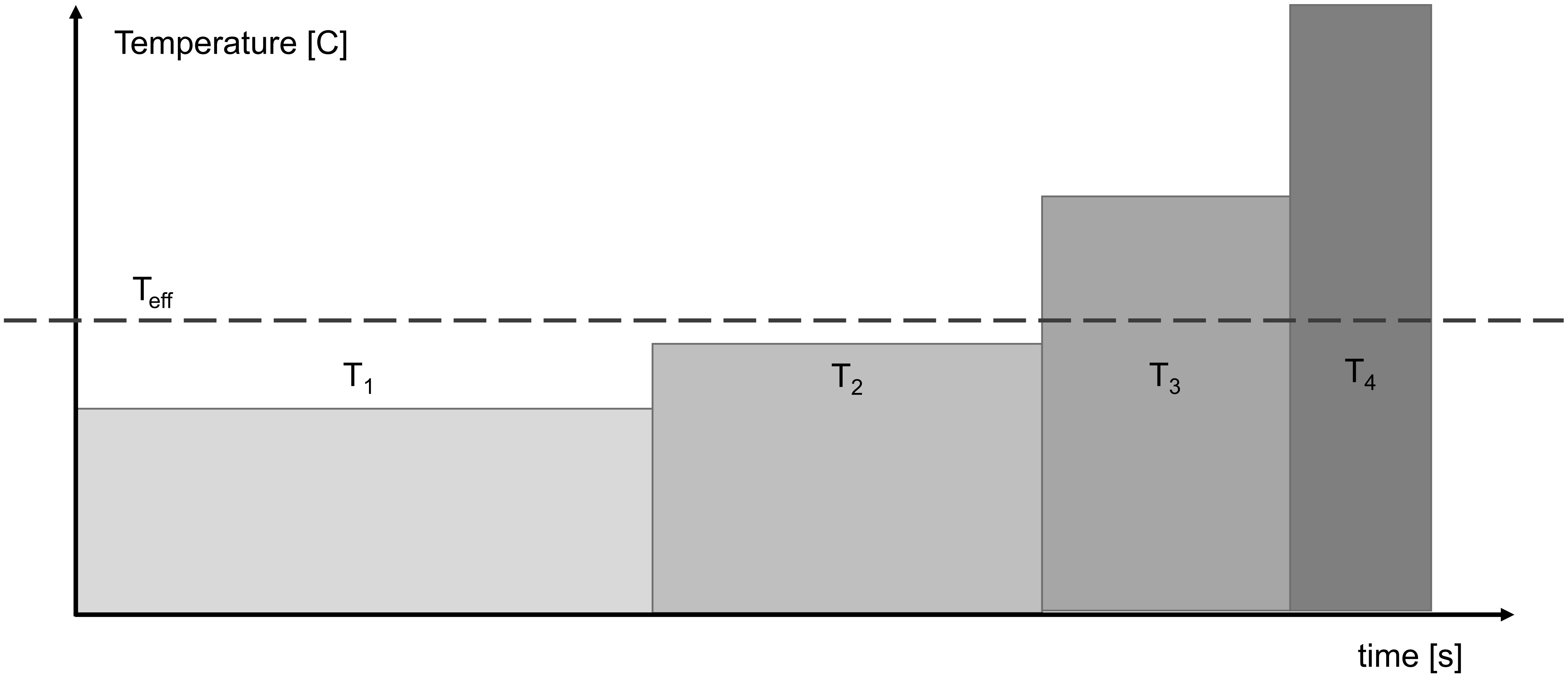
- In a circuit with feedback loop, a positive bias current and aging effect feedback can cause device degradation to rapidly increase thus causing failure



# Mission Profile Example

## Temperature vs. cumulative effective lifetime profile



# Conclusion



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# Legato™ Reliability Solution

## Industry's first complete analog IC design-for-reliability solution

**Analog Defect Analysis**: Reduces test cost and eliminates test escapes

**Electro-Thermal Analysis**: Prevents thermal overstress to avoid premature failures

**Advanced Aging Analysis**: Accurately predicts product wear-out


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