weeroc

High-end Microelectronics Design

Mixed-Signal Test Vehicle in Microchip Atmel ATMX150RHA

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AIRBUS

Presentation outlook

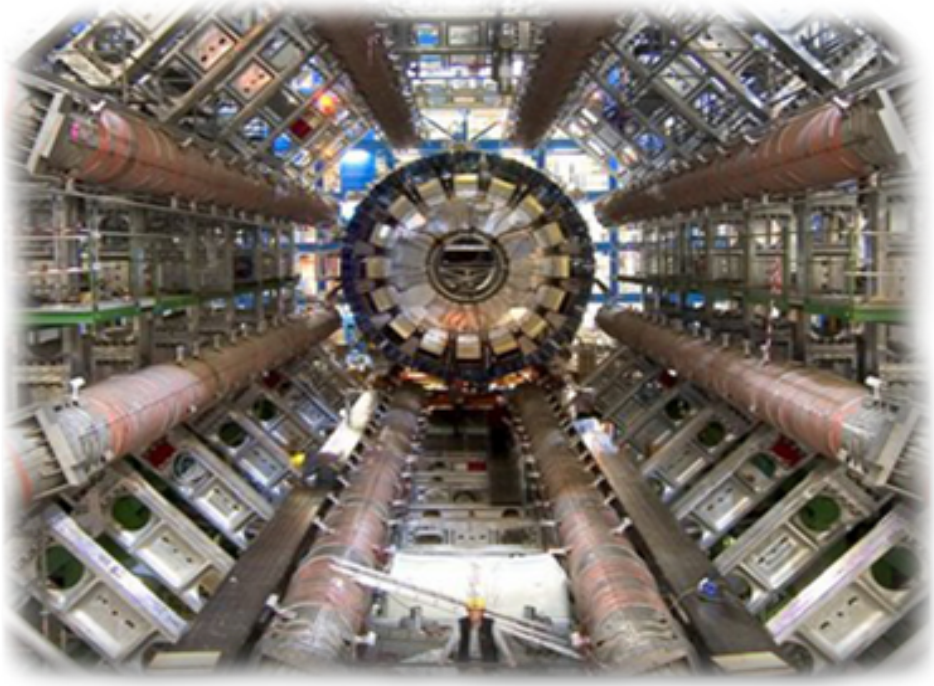
- Weeroc presentation
- Test vehicle presentation
- DAC requirement specification
- DAC design
- DAC performances
- Conclusion & next step

WEEROC PRESENTATION

Say Hi !

Weeroc story

- Founded by engineers (OMEGA) from IN2P3/CNRS
  nuclear and particle physics institute, nat. french agency for research
- Officially established in 2012
- Weeroc & OMEGA are located at Ecole Polytechnique campus



Core activities at IN2P3/CNRS:

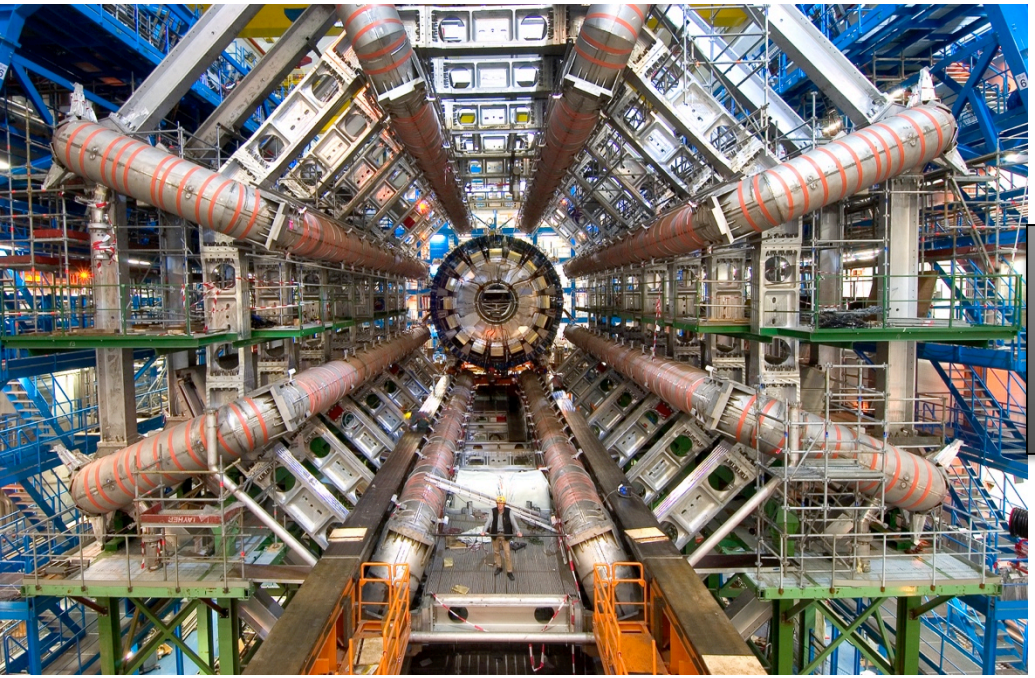
Design of front-end integrated circuits to read-out particle physics detectors

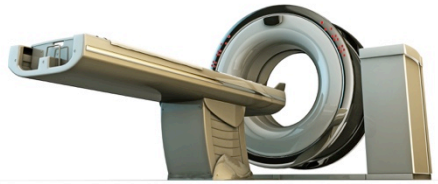
Our expertise

Radiation tolerant design

Low noise, low power analog microelectronics circuits

Technology and knowledge transfer





cnrs IN2P3 Les deux infinis

ΩMEGA Microelectronics

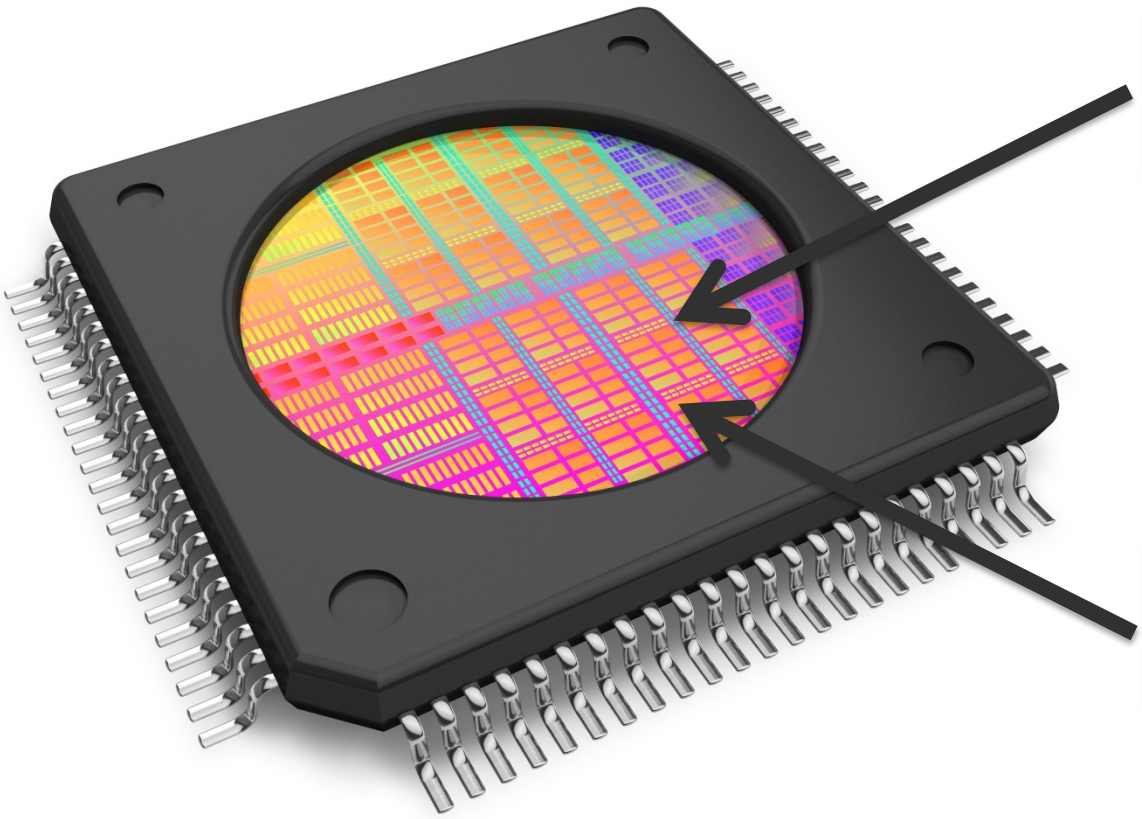
weeroc

Expertise of Weeroc

Design and marketing

Analog & mixed-signal microelectronics ICs for photodetectors read-out

and radhard application



Particle detection

Low-noise, low power, analog and mixed-signal design

Radhard design

Weeroc markets

Medical imaging

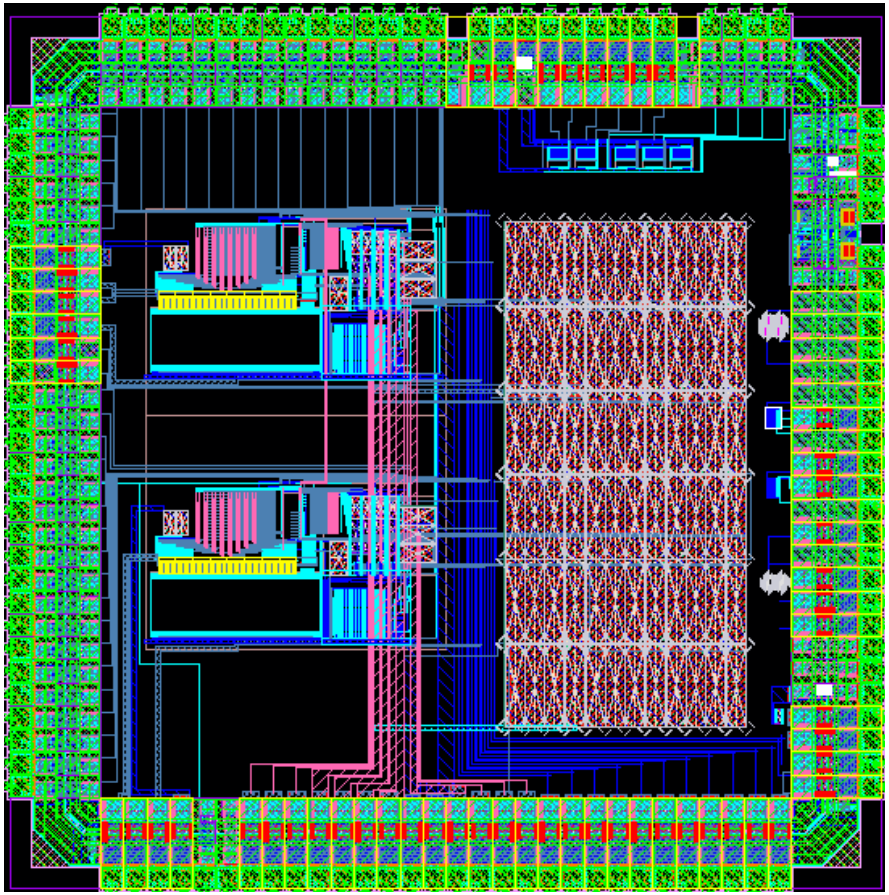
Aerospace industry

Nuclear industry

Homeland security

Scientific instrumentation

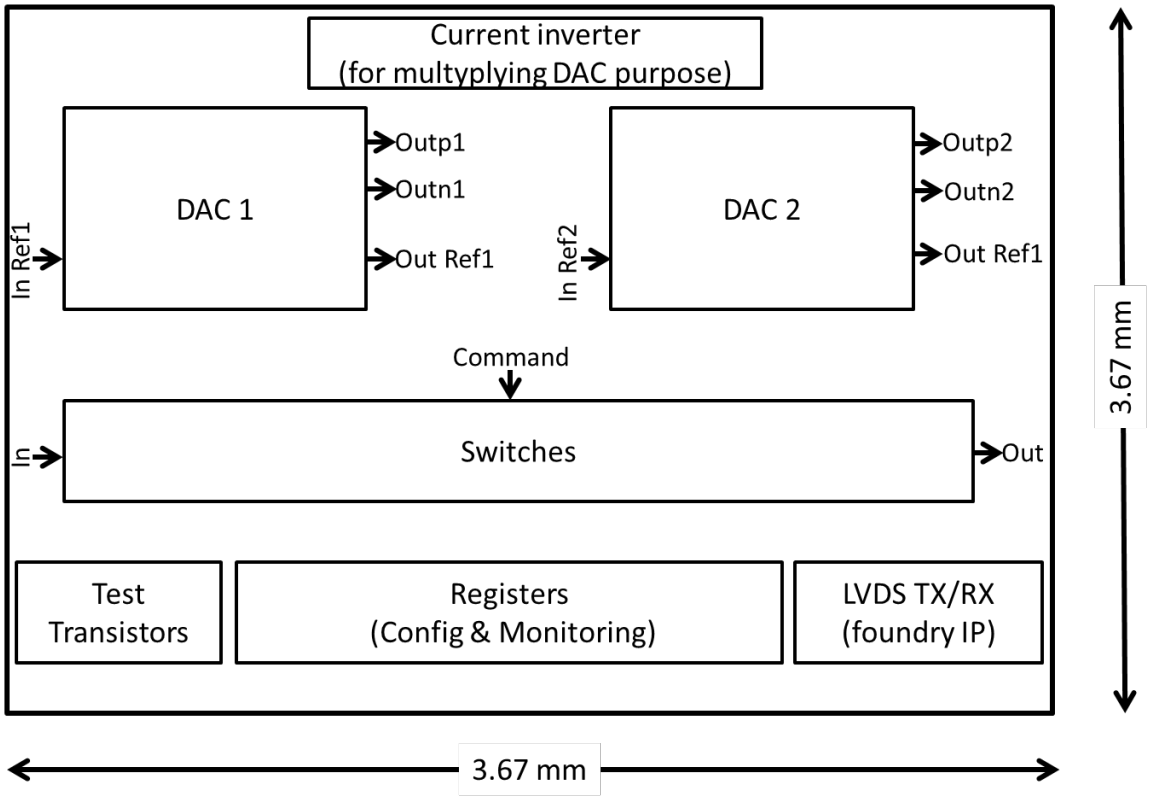
Analytical instrumentation



TEST VEHICLE PRESENTATION

The test vehicle

- 2 16b – DAC, differential
- Set of RF switches
- LVDS
- HV LDMOS HVMOS
- Programmable register
- Programmable probe



Focus on 16b-DAC in that talk

DAC 16 bit : requirement specifications

- 16 bits
- 4 MSPS min - 12MSPS typical speed
- Differential current output
- 1mA min /10mA max current output – tunable

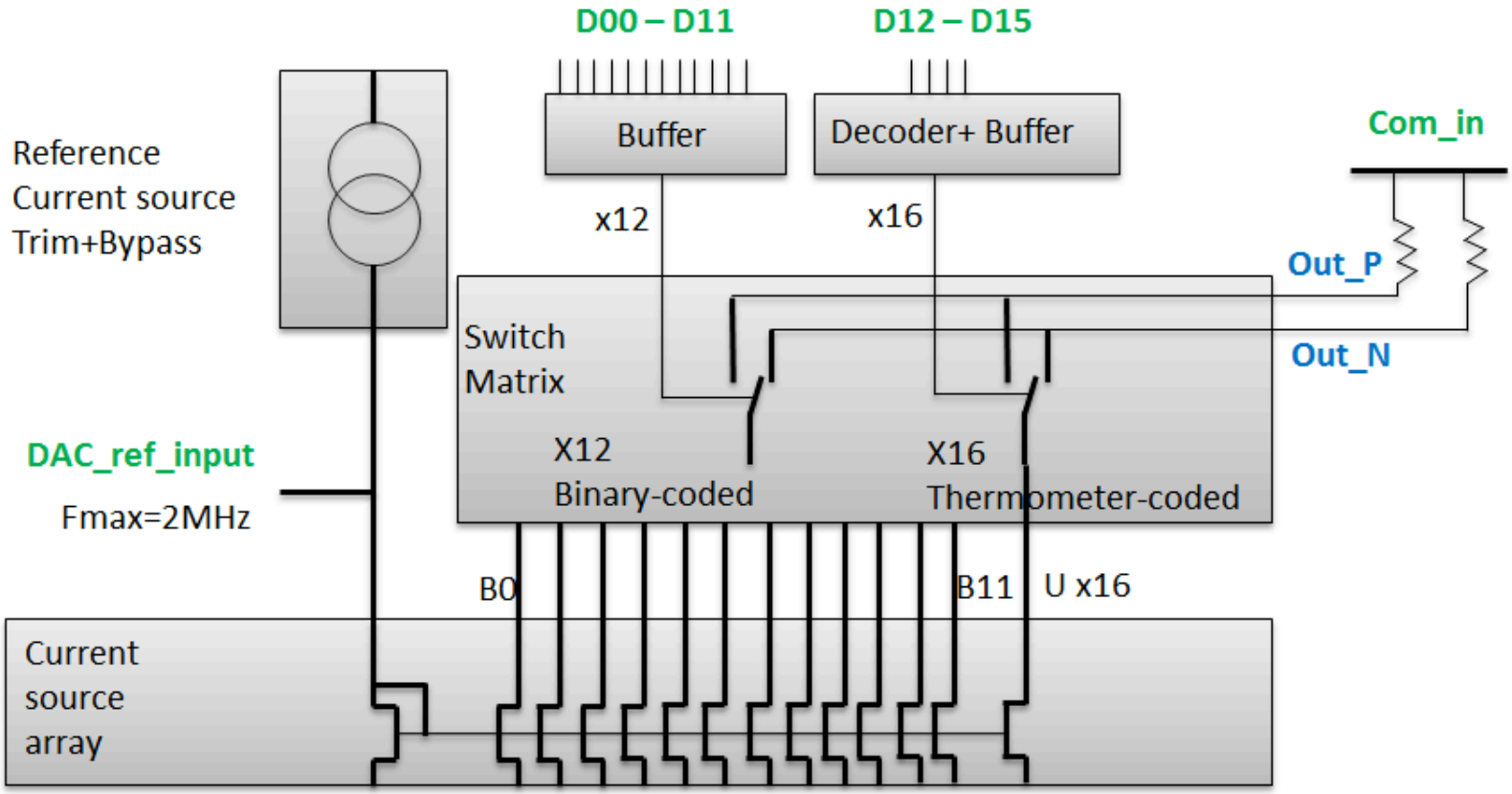
Parameter	Min.	Typ.	Max.	Units
Maximum full-scale output current	4	20		mA
Minimum output current	-	-	0	mA
Settling time to ±1/2 LSB	-	-	50	ns
Analogue output loads	-	50	-	Ω
Output loads capacitances	-	-	10	pF
Output glitch amplitude	-	-	1/2	LSB
Output glitch surface	-	-	35	pV
Maximum admissible conversion rate	4	12	-	MSps
Integral Non-Linearity (INL)	-4	-	+4	LSB
Differential Non-Linearity (DNL)	-5	-	+5	LSB
Spurious Free Dynamic Range (SFDR) @1MHz	-	80	-	dBc

State of the art

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
DC ACCURACY[1]				
Linearity Error				
T_A = +25°C	–8	±4	+8	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Differential Nonlinearity				
T_A = +25°C	–6	±2	+6	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Monotonicity (13-Bit)	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE			
ANALOG OUTPUT				
Offset Error	–0.2		+0.2	% of FSR
Gain Error	–1.0		+1.0	% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range	–1.2		+5.0	V
Output Resistance	0.8	1.0	1.2	kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	2.475	2.5	2.525	V
Reference Output Current[3]		+5.0	+15	mA
REFERENCE INPUT				
Reference Input Current	1	5	7	mA
Reference Bandwidth[4]				
Small Signal, IREF = 5 mA ± 0.1 mA		28		MHz
Large Signal, IREF = 4 mA ± 2 mA		9		MHz

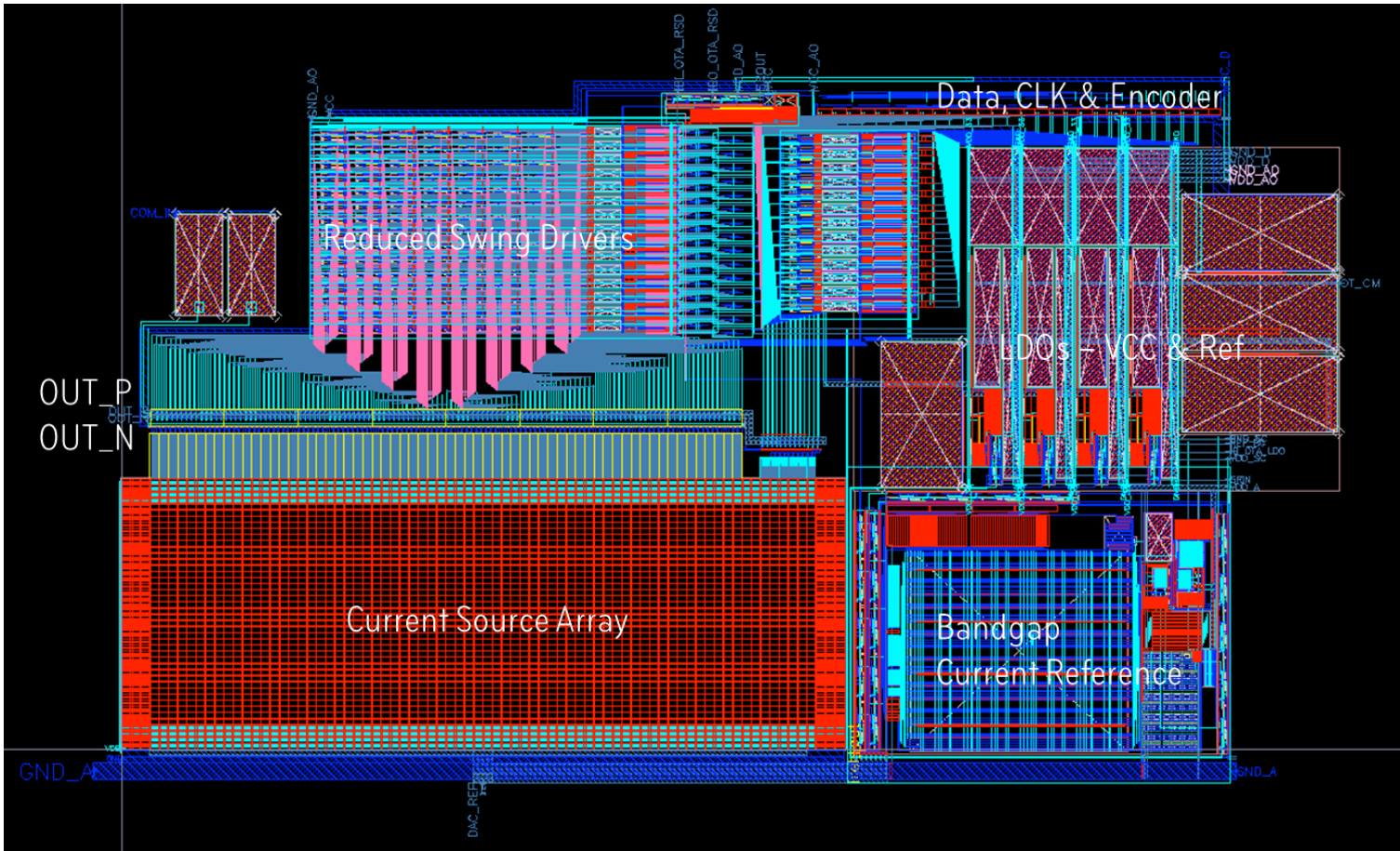
DAC 16 bit architecture

- Bibliography → see proceedings
- Current steering DAC
- 16 bit : 12 binary (LSBs)+ 4 thermometer (MSBs)



Layout

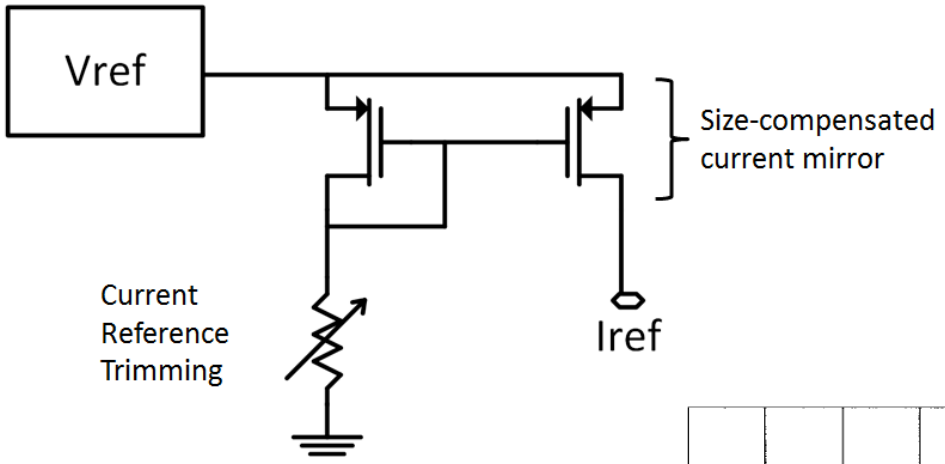
- Area : about 0.85mm2
- Include bandgap reference, 4 LDOs for intermediate voltage

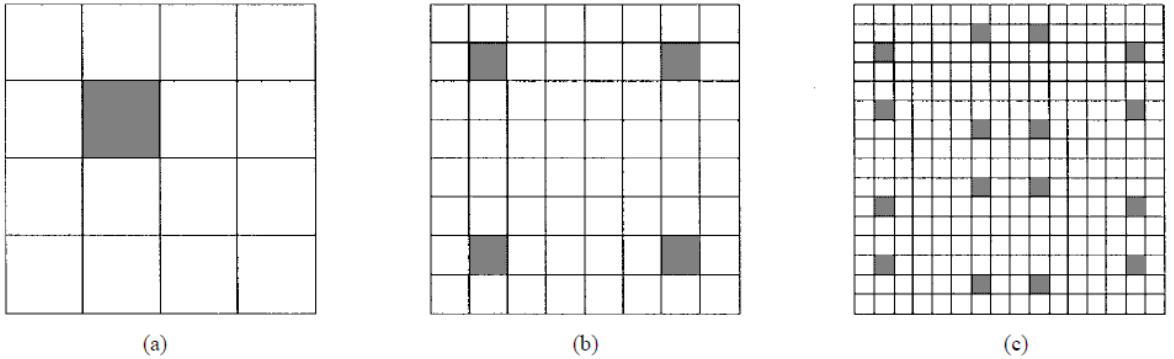


Current reference and current source array

- Current reference can be trimmed by programmation
- Current source array follow a Q2 random walk (see bibliography)

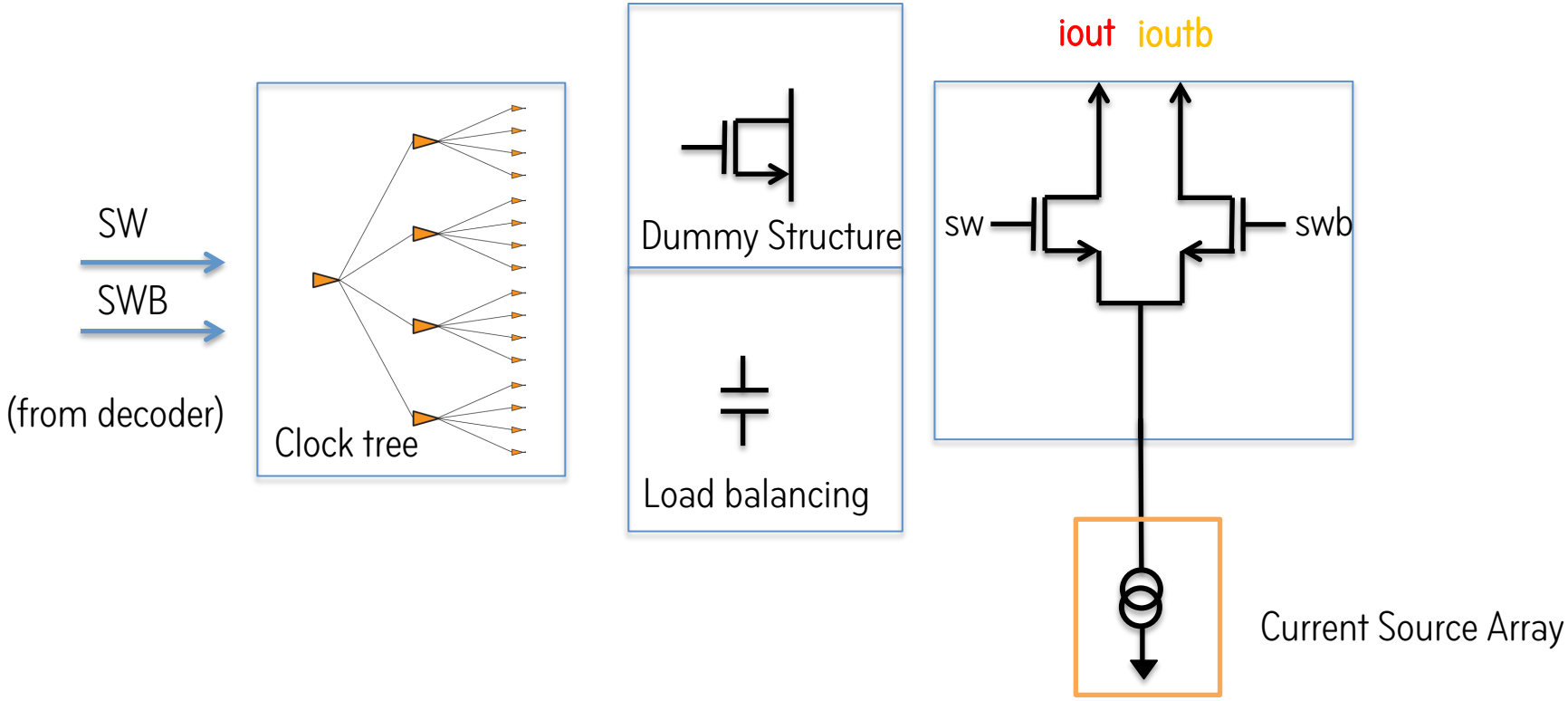
Bit #	Min INL (LSB)	Max INL (LSB)
B00_INL	0,055	0,058
B01_INL	0,111	0,115
B02_INL	0,201	0,213
B03_INL	0,316	0,343
B04_INL	0,308	0,383
B05_INL	-0,083	0,099
B06_INL	-0,147	0,156
B07_INL	-0,204	0,164
B08_INL	-0,320	0,265
B09_INL	-0,341	0,379
B10_INL	-0,528	0,436
B11_INL	-0,672	0,681
B12_INL	-1,042	0,851
B13_INL	-1,549	1,621
B14_INL	-1,756	1,701
B15_INL	-1,934	1,479





G. Van Der Plas et al. « A 14-bit Intrinsic Accuracy Q2 Random Walk CMOS DAC » IEEE Journal of Solid State Circuits, vol. 34, no. 12, December 1999, pages 1708-1718.

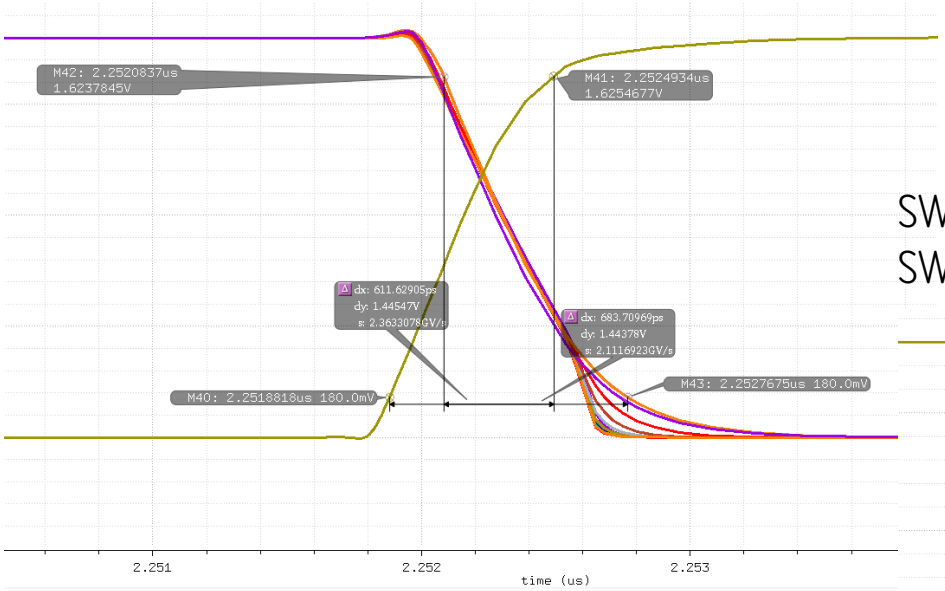
Switch array architecture



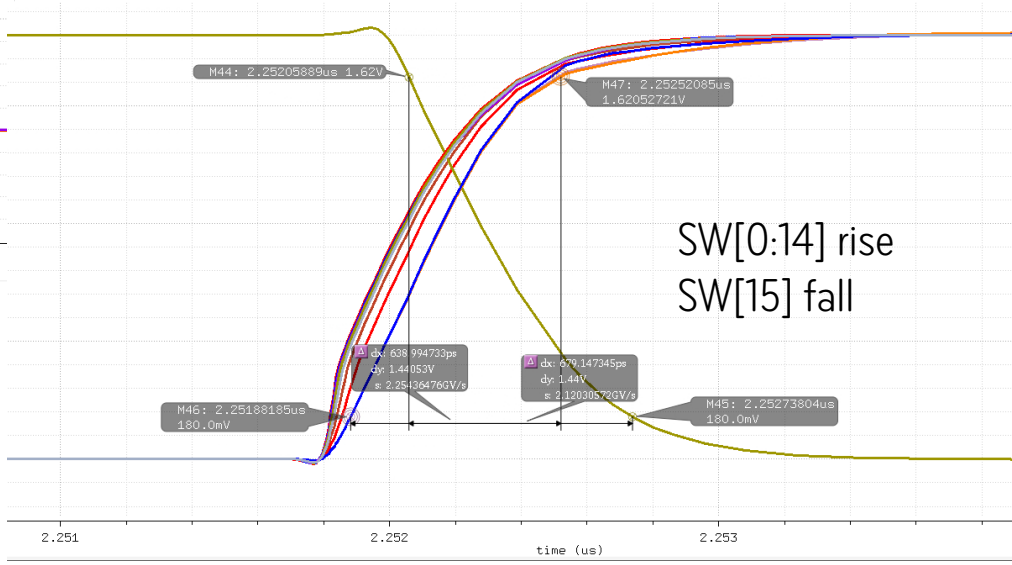
All cells designed placed and routed on full custom

Switches timing

- Load balance for every switch unit
- Rise/fall time trade-off
  - Reducing charge injection feedthrough to output
  - Avoid simultaneous switch OFF state
- Rise/fell ~ 650ps +/- 50ps



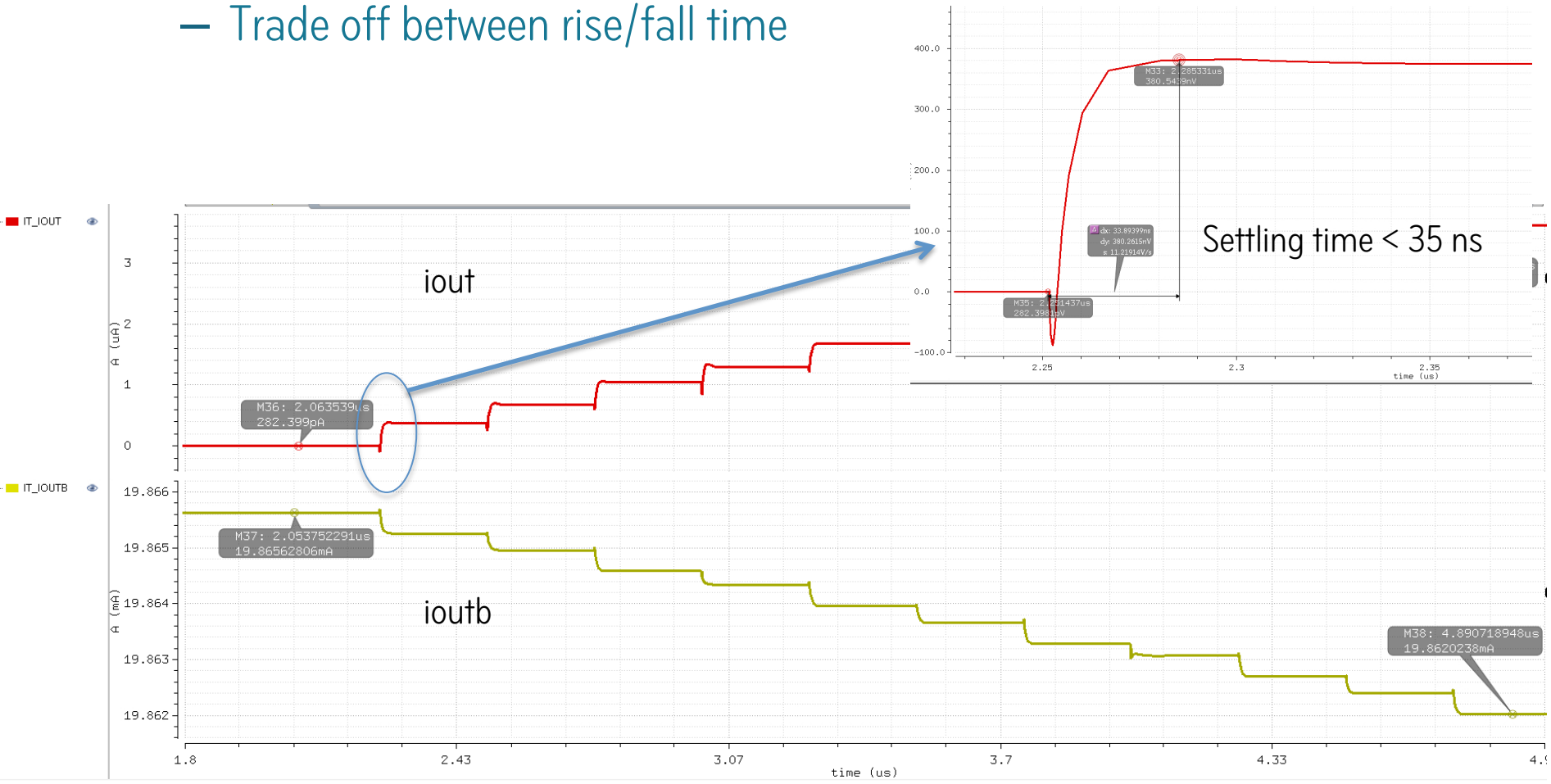
SW[0:14] fall
SW[15] rise



SW[0:14] rise
SW[15] fall

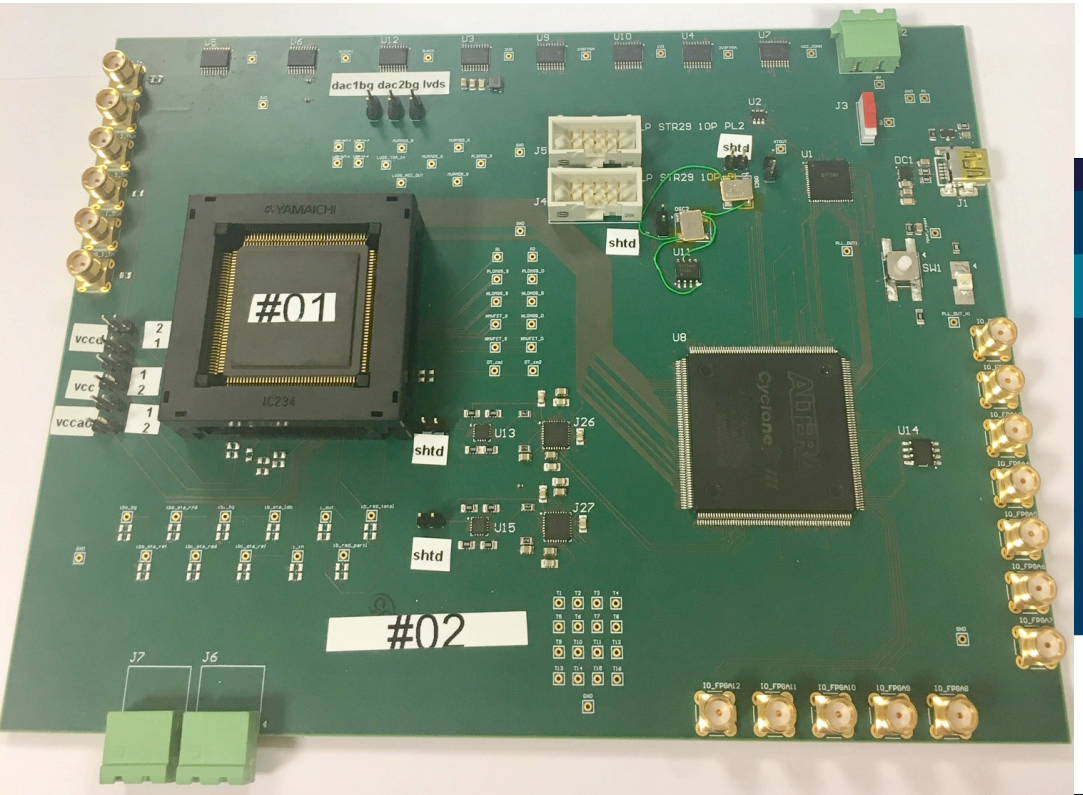
Current output

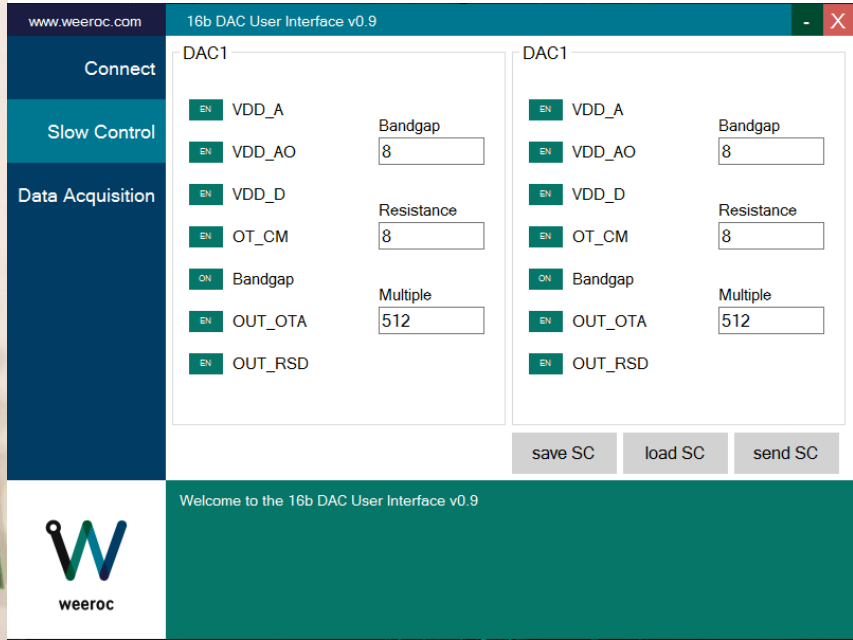
- Load balancing between switch array
  - Trade off between rise/fall time

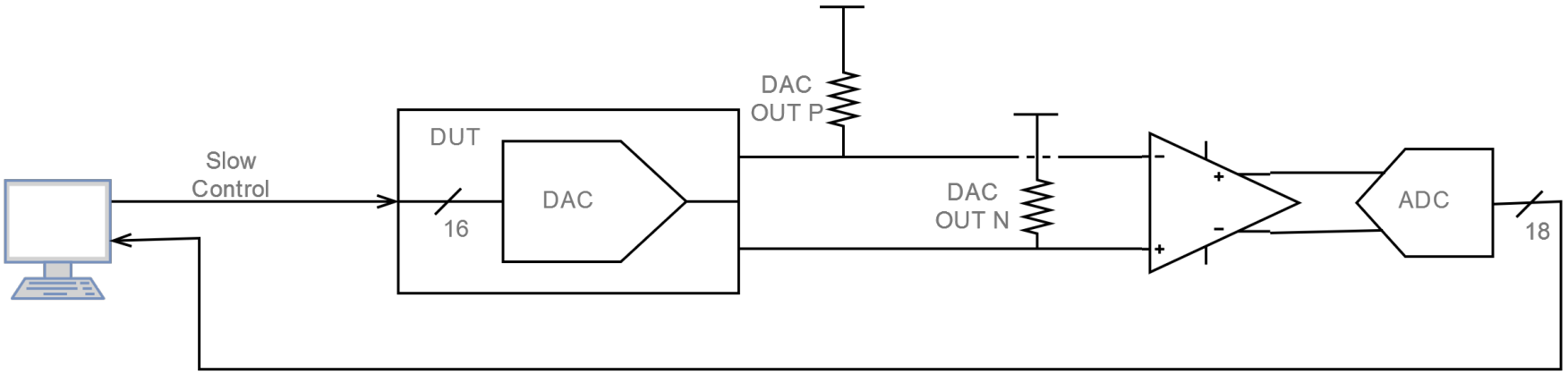


Characterization board

- A characterization board and a firmware/software have been designed to measure the 16b DAC



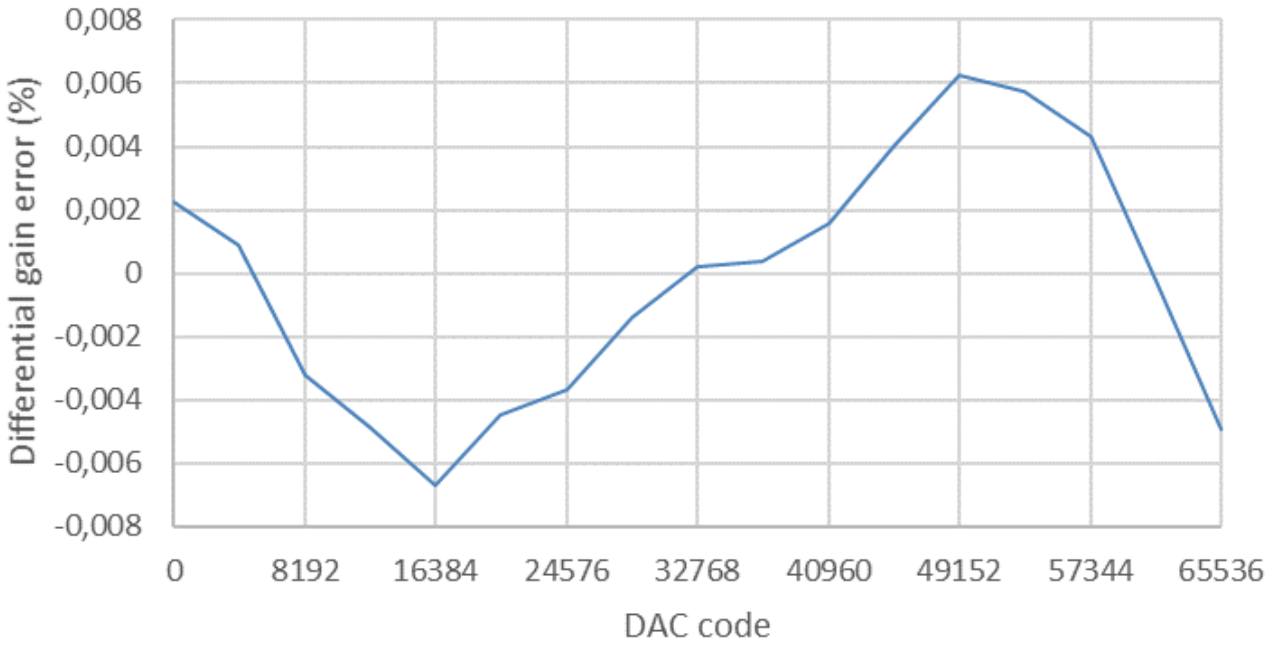




STATIC MEASUREMENT

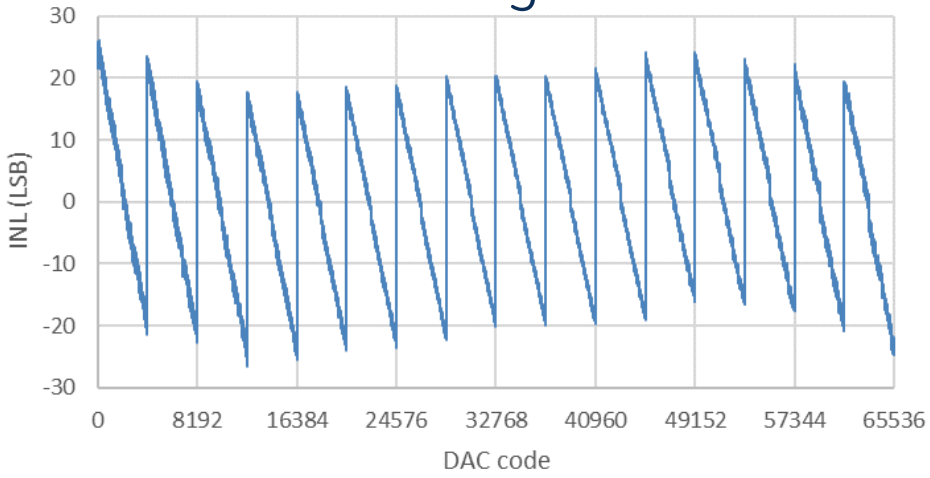
Offset and Gain Error

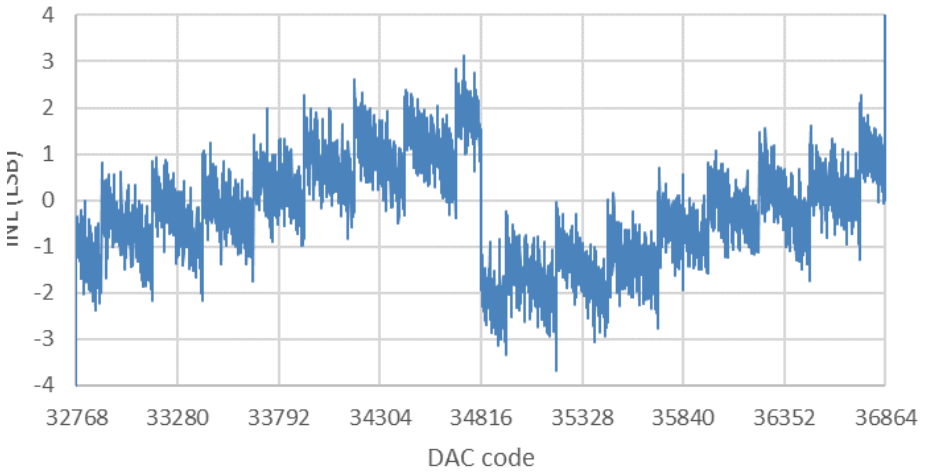
- The requirement on the gain error is ± 1 % on the full scale range. The error on this measurement is -0.0455 %. The offset error is -0.09 % FSR with a requirement of ± 0.2 % FSR.

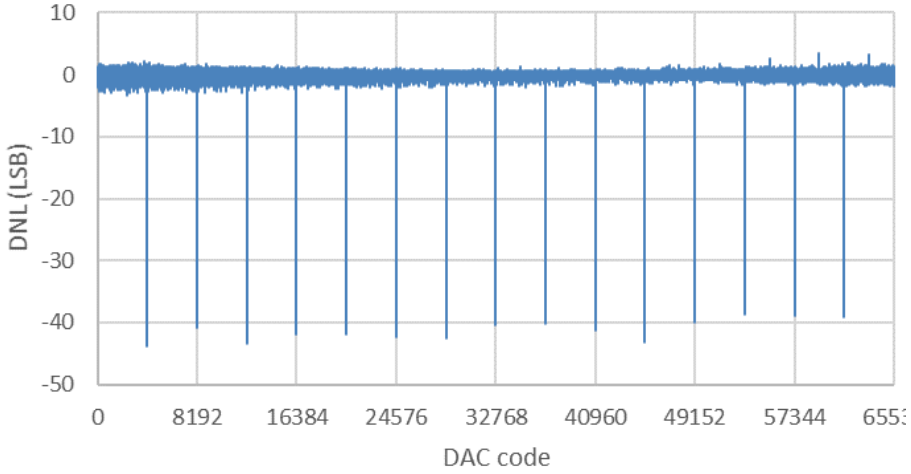


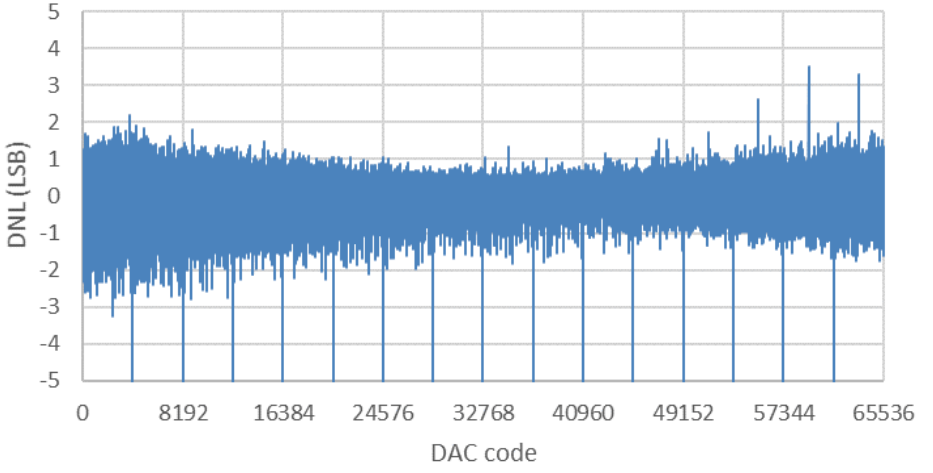
INL and DNL

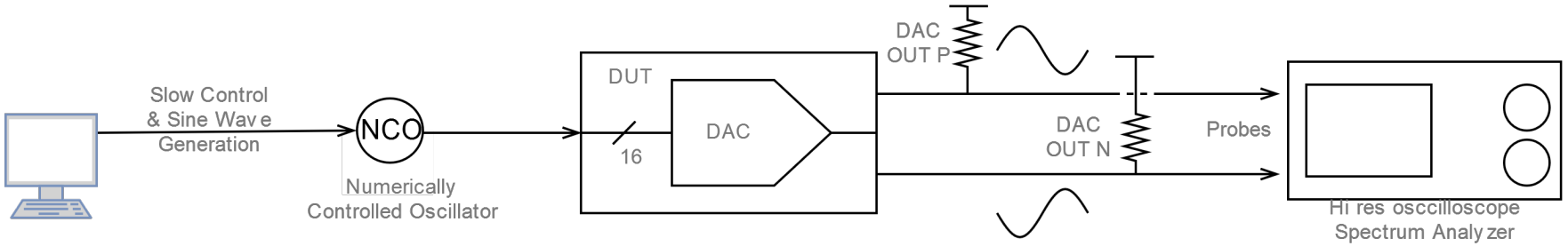
- Thermometer to binary mismatch
- Need fine tuning









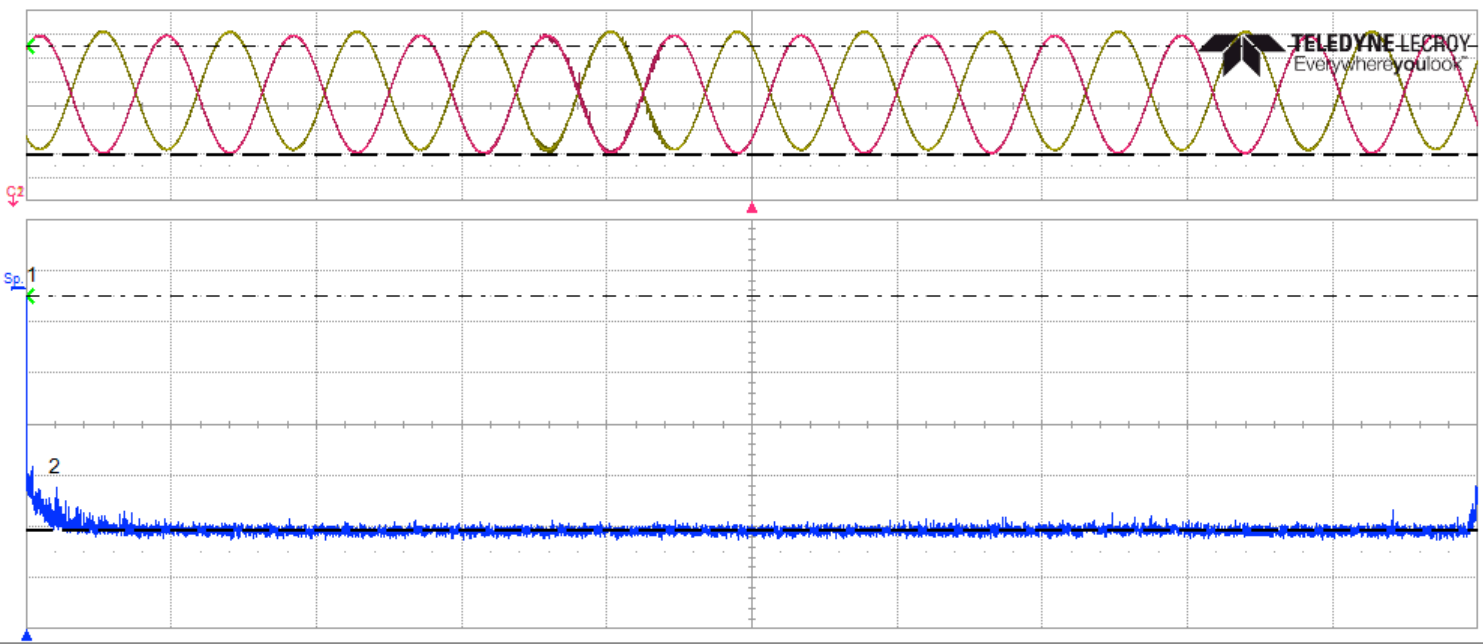


AC MEASUREMENT

Frequency domain analysis

- Numerically controlled oscillator build sine @1k, 10k, …, 1M
- DAC sampling rate is swept from 1M, 4M, 10M
- DAC output is analyzed with 12b HiRes scope

Peaks	Frequency	Amplitude
1	229 Hz	-3.16126 dBV
2	10.757 kHz	-77.8488 dBV



C1 DC1M
200 mV/div
-2.67000 V
3.168 V
2.258 V
Δy -910 mV

C2 DC1M
200 mV/div
-2.70000 V
3.198 V
2.288 V
Δy -910 mV

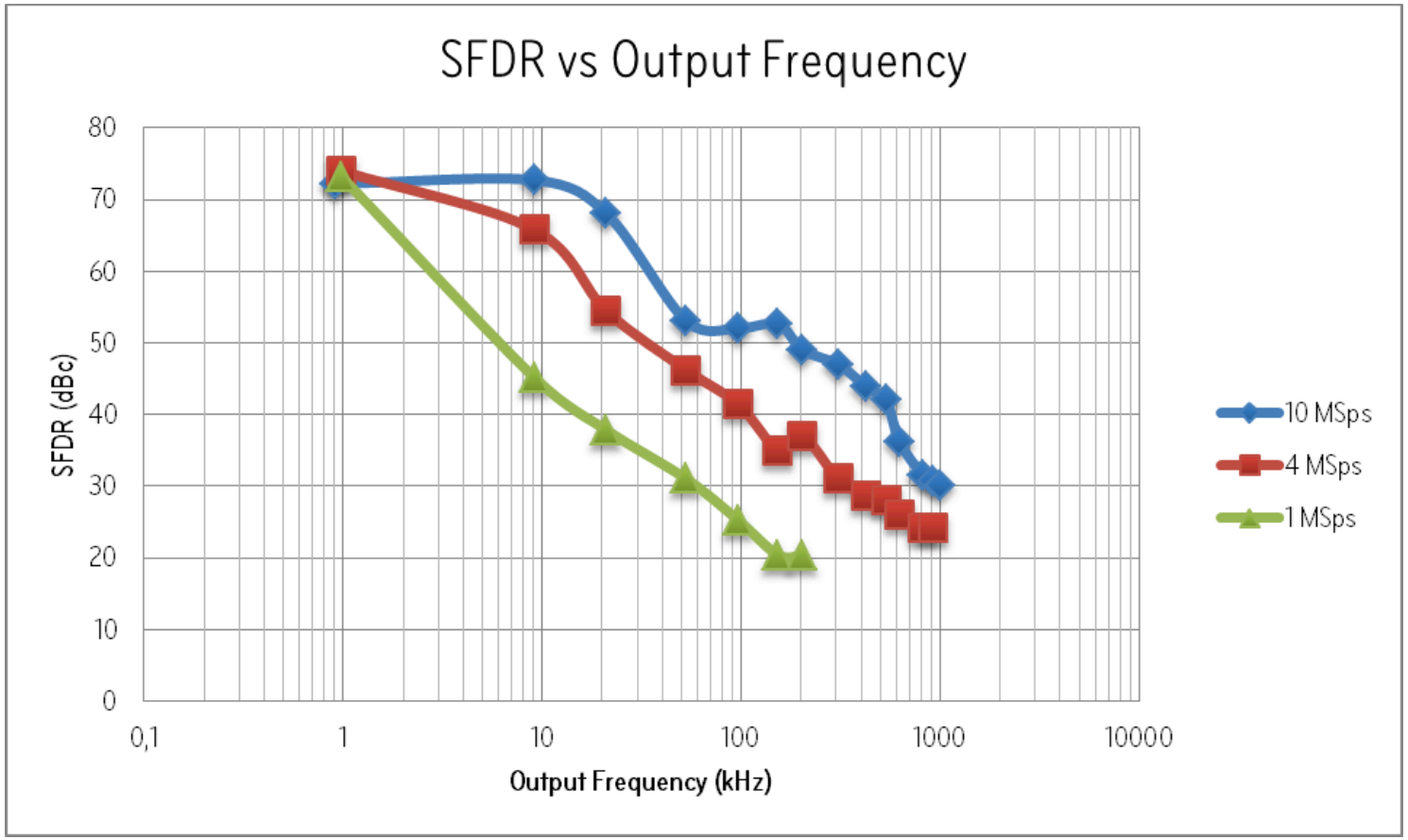
SpecAn C1-C2
20.0 dB/div
50.0 kHz/div
813 #
-3.1 dBV
-94.1 dBV
Δy -91.0 dB

Timebase 0.0 ms
5.00 ms/div
125 kS 2.5 MS/s

Trigger C4 DC
Auto 500 mV
Edge Negative

SFDR

- Almost in spec for low frequencies
- Digital picking noise issue to be corrected → padring



Conclusion & next step

- A 16bit DAC 10MSPS has been designed in ATMX150RHA
- Technology shows very good analogue performances
- 2 actions to get in specification
  - Fine tuning Thermometer to binary
  - Floorplanning modification & pinout optimization
- Test vehicle to be tested in irradiation (@TRAD)
  - CNES funding
- New iteration : as soon as $
- Thanks to Airbus and CNES for their trust and support

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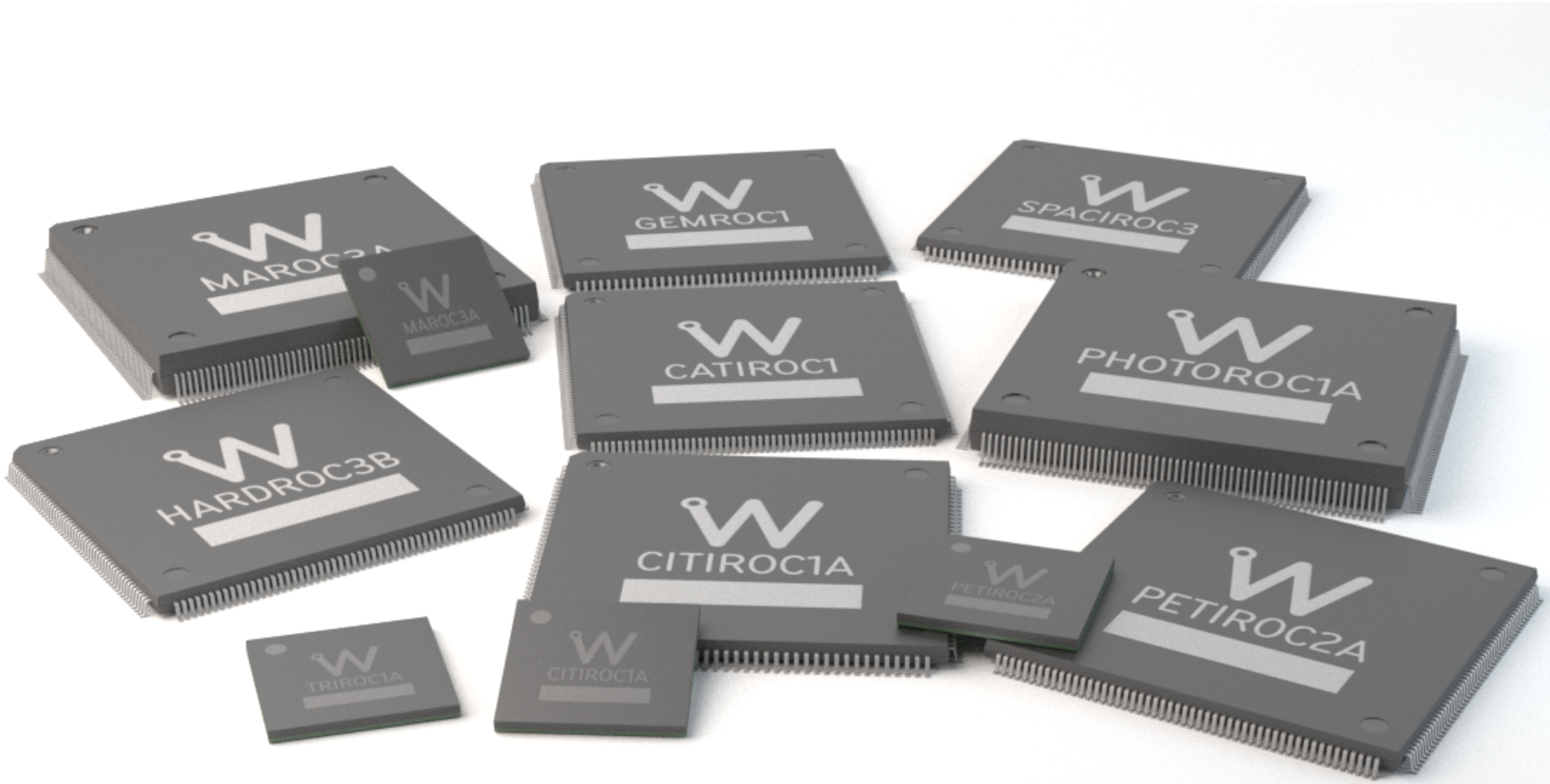
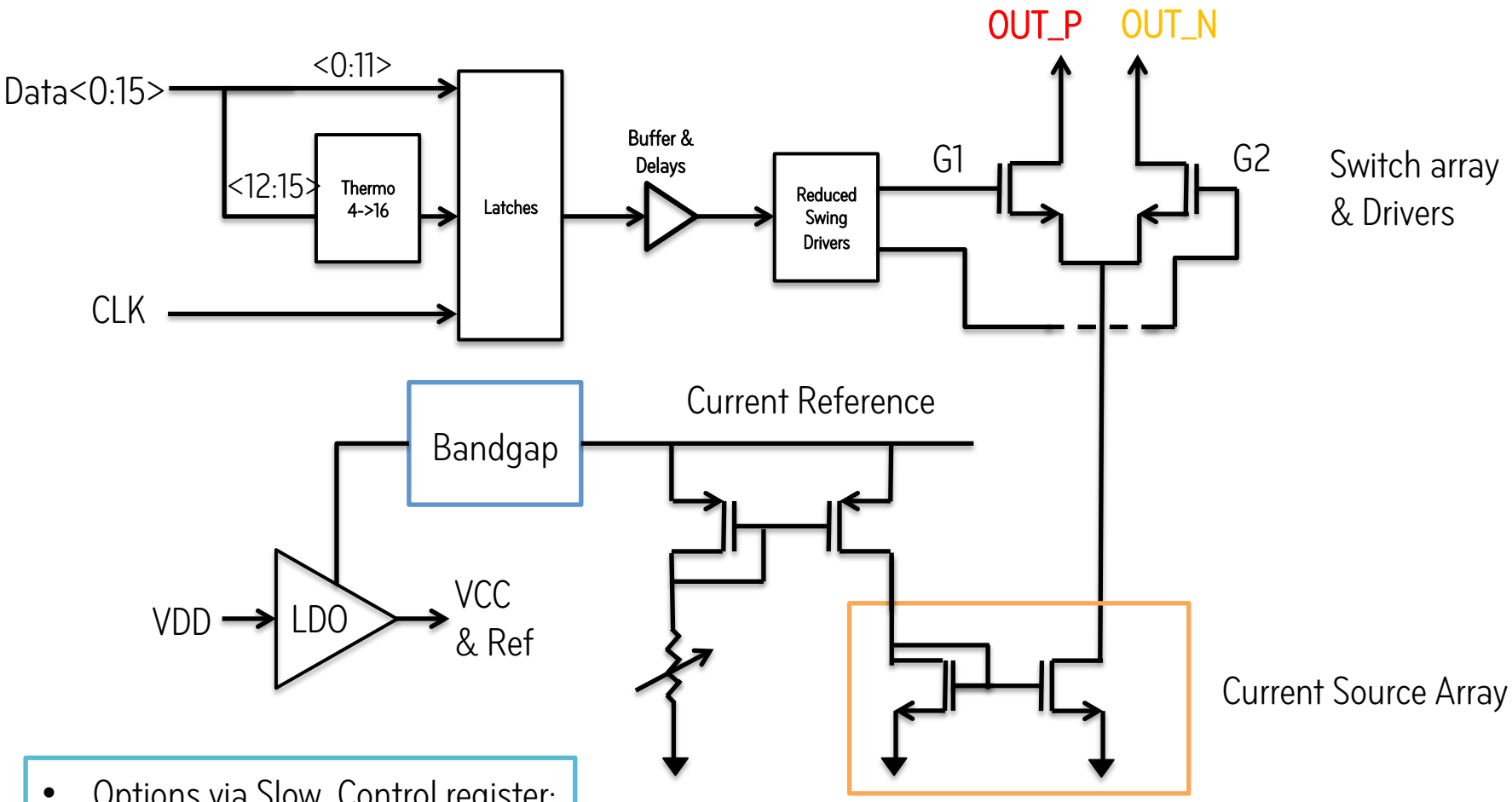
Thank you


MAROC3A
MAROC3A
GEMROC1
SPACIROC3
CATIROC1
PHOTOROC1A
HARDROC3B
CITIROC1A
PETIROC2A
PETIROC2A
TRIROC1A
CITIROC1A

Architecture

DAC segmentation : 12-bit binary & 4-bit unary



- Options via Slow Control register:
  - Current ref trimming
  - Regulator off
- Pads access for bias adjustment