STATIC LINEARITY TEST FOR RADIATION EFFECTS CHARACTERIZATION OF AN 18-BIT SAR SERIAL IO COTS ADC: ANALOG DEVICES AD7982

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OUTLINE

- INTRODUCTION
- SINEWAVE HISTOGRAM TEST METHOD
- IMPROVED ALGORITHM BASED ON AN INL MATHEMATICAL SEGMENT MODEL
- EXPERIMENTS
  - DEVICE UNDER TEST
  - SET-UP FOR MEASUREMENTS
  - RESULTS AND METHODS COMPARATION
- CONCLUSIONS

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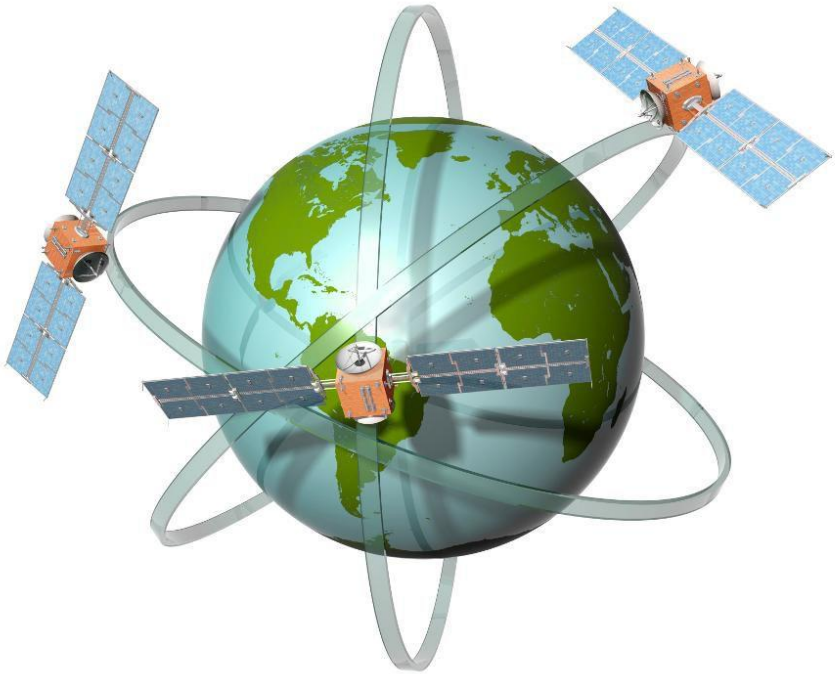
INTRODUCTION

Space Industry

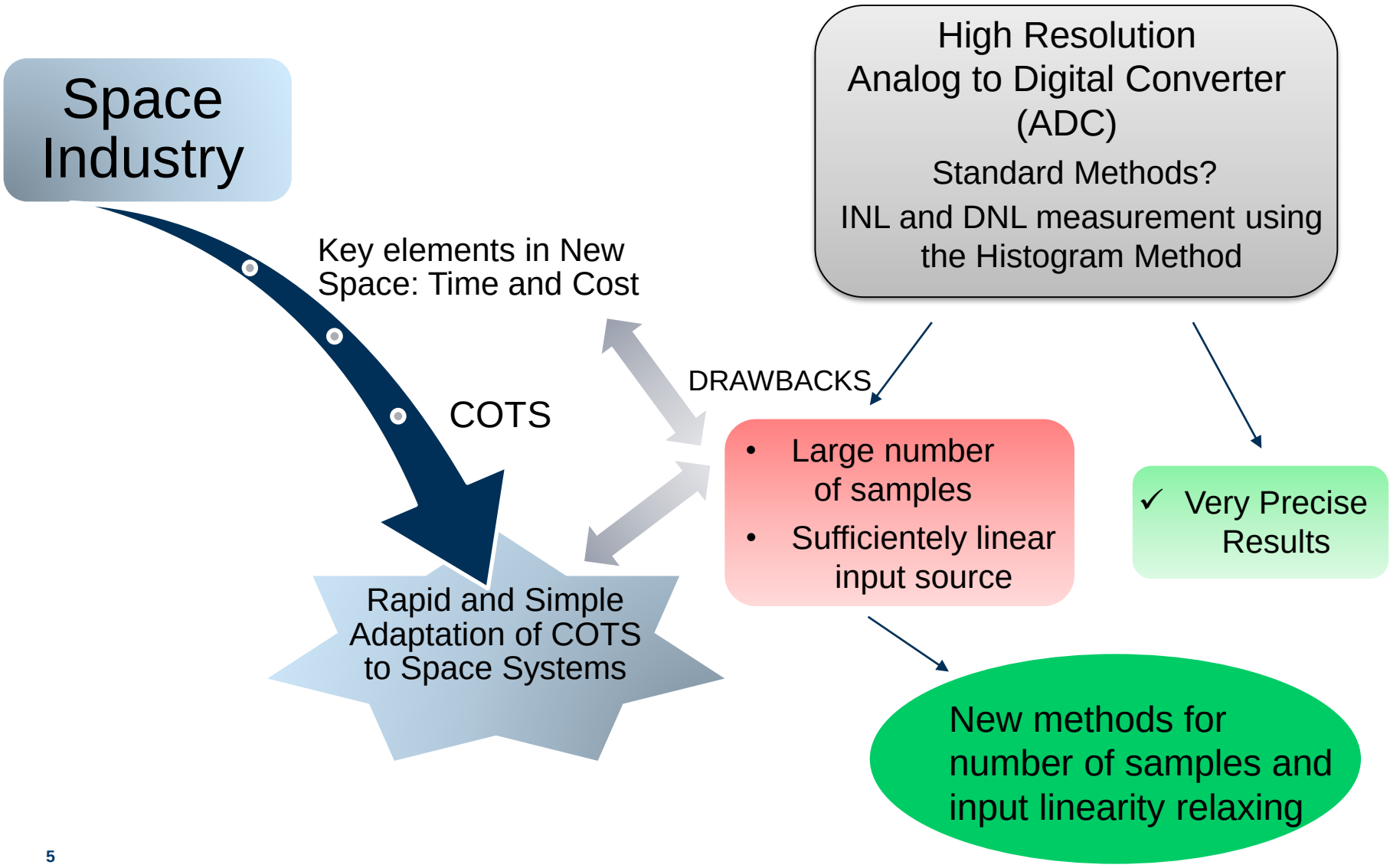
Key elements in New Space: Time and Cost

COTS

Rapid and Simple Adaptation of COTS to Space Systems



INTRODUCTION



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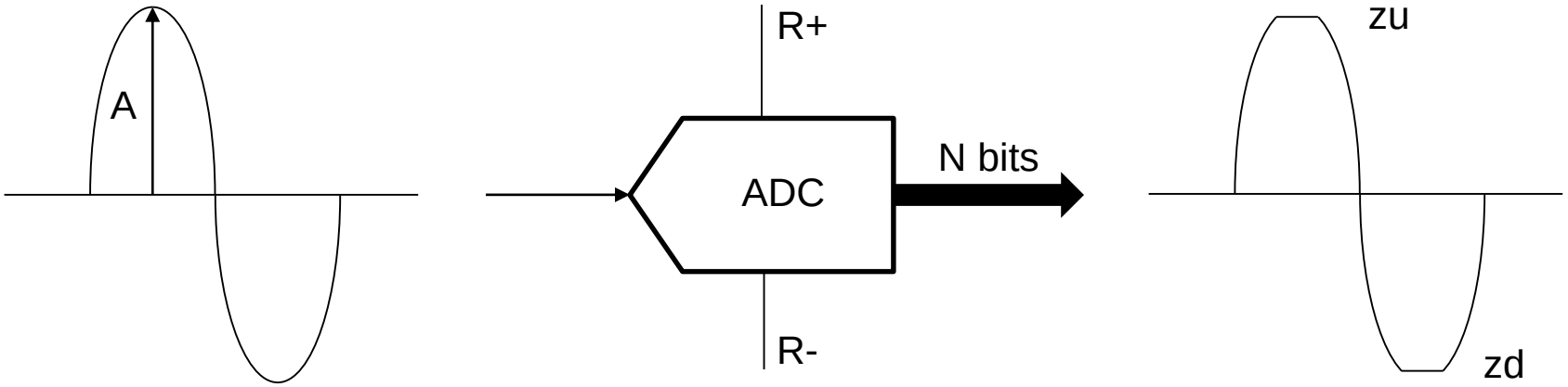
SINEWAVE HISTOGRAM TEST METHOD



$$P(k) = \frac{S(k)}{\sum_{k=zd}^{zu} S(k)},\ k \in [zd, zu]$$

$$Q(k) = P(z < k) = \sum_{z=zd}^{k-1} P(z),\quad k \in [zd+1, zu]$$

$$tk = \mathrm{C} - \mathrm{Acos}\left(\pi Q(k)\right),\quad k \in [zd+1, zu]$$

$$INL(k) = \frac{t(k) - l(k)}{LSB},\quad k \in [zd+1, zu]$$

$$DNL(k) = INL(k+1) - INL(k) = \frac{t(k+1) - t(k)}{LSB} - 1,\quad k \in [zd+1, zu-1]$$

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IMPROVED ALGORITHM BASED ON AN INL MATHEMATICAL SEGMENT MODEL

Based on **three main factors**:

- The amount of truly independent error sources contributing to linearity errors is much lower tan the number of code bins to be tested.

- All sampled codes are valid to estimate the ADC parameter, as the noise is rejected by the algorithm itself.

- INL accept a mathematical segment model: SAR, Pipeline and Cyclic ADCs present such kind of segmented non-linearity pattern error.

IMPROVED ALGORITHM BASED ON AN INL MATHEMATICAL SEGMENT MODEL

Example: ADC of N=18 bits of resolution with segmentation r_M=8, R_I=7, R_L=3 bits

Output Code Z can be written in terms of three subcodes:

$$Z \equiv \{b_{17}, b_{16}, \dots, b_1, b_0\} \equiv \{b_{17}, b_{16}, \dots, b_{11}, b_{10}\} || \{b_9, b_8, \dots, b_4, b_3\} || \{b_2, b_1, b_0\}$$

$Z_M = \{b_{17}, b_{16}, \dots, b_{11}, b_{10}\}$, as the Most significant code
$Z_I = \{b_9, b_8, \dots, b_4, b_3\}$, as the Intermediate significant code
$Z_L = \{b_2, b_1, b_0\}$, as the Least significant code

Assuming INL Segmentation Model

INL can be expressed as sum of three functions:

$$INL(Z) = f_M(Z_M) + f_I(Z_I) + f_L(Z_L), , Z \in [1, 2^N - 1]$$

$f_M(.)$= discrete function of (2^{N_M}-1) values → 255 parameters
$f_I(.)$ = discrete function of (2^{N_I}-1) values → 127 parameters
$f_L(.)$ = discrete function of (2^{N_L}-1) values → 7 parameters

INL is determined only by 255+127+7 = 389 parameters

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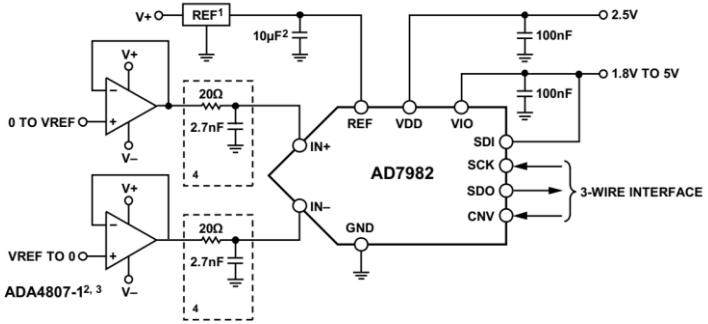
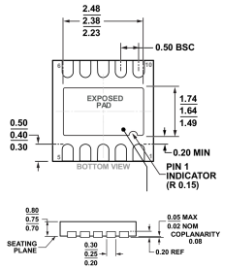
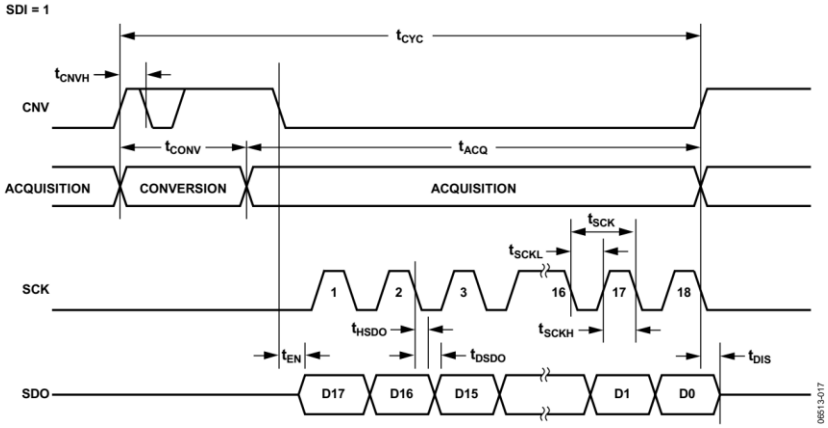
EXPERIMENTS: DEVICE UNDER TEST

AD7982 of Analog Devices → TID Radiation test under ^{60}Co till 100kRad for JUICE Mission, 5 samples biased and 5 samples unbiased

- General Characteristics:
  - 18-bit, Serial IO SAR converter
  - INL = ±2LSB, DNL = -0.85LSB to +1.5LSB (no missing codes)
  - Input range = 10Vpp differential
  - 3mmx3mm 10-Lead LFCSP
- Space trending:
  - COTS
  - Serial IO →$\overline{CS}$ mode 3-wire without busy indicator



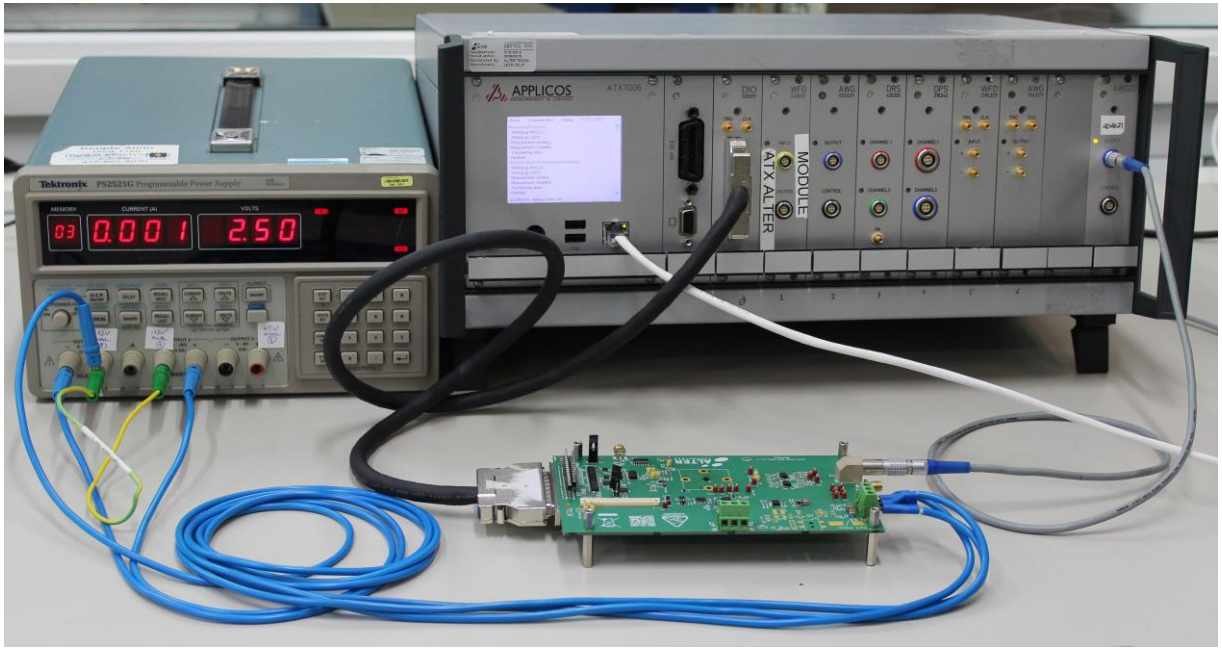




EXPERIMENTS: SETUP FOR MEASUREMENTS

Setup:

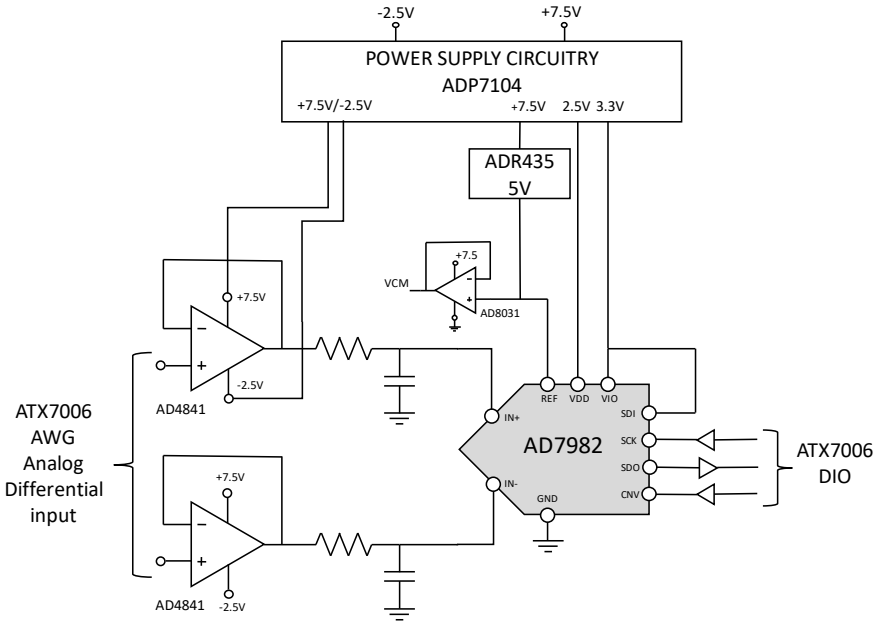
- PCB Board
- Programmable Power Supply
- Analog ATE Applicos ATX7006

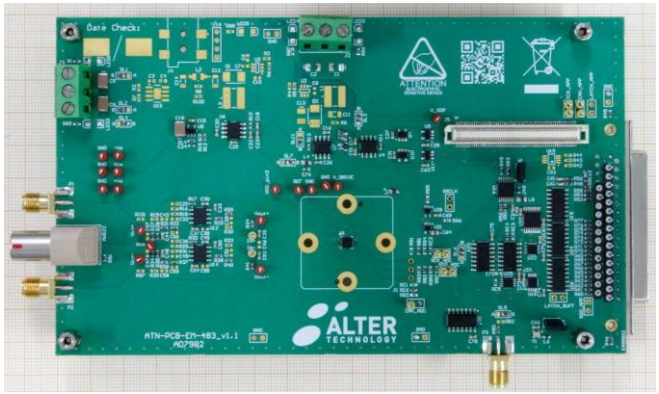


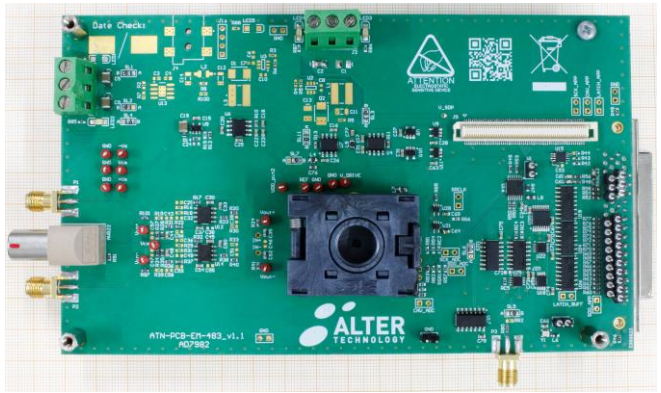
EXPERIMENTS: SETUP FOR MEASUREMENTS

PCB Board:

- XFET reference (ADR435)
- 2 low noise, low distortion and rail-to-rail op amps (AD4841)
- Set at midscale by the use of a reference voltage divider buffered by a rail-to-rail, high speed and fast settling amplifier (AD8031)







EXPERIMENTS: SETUP FOR MEASUREMENTS

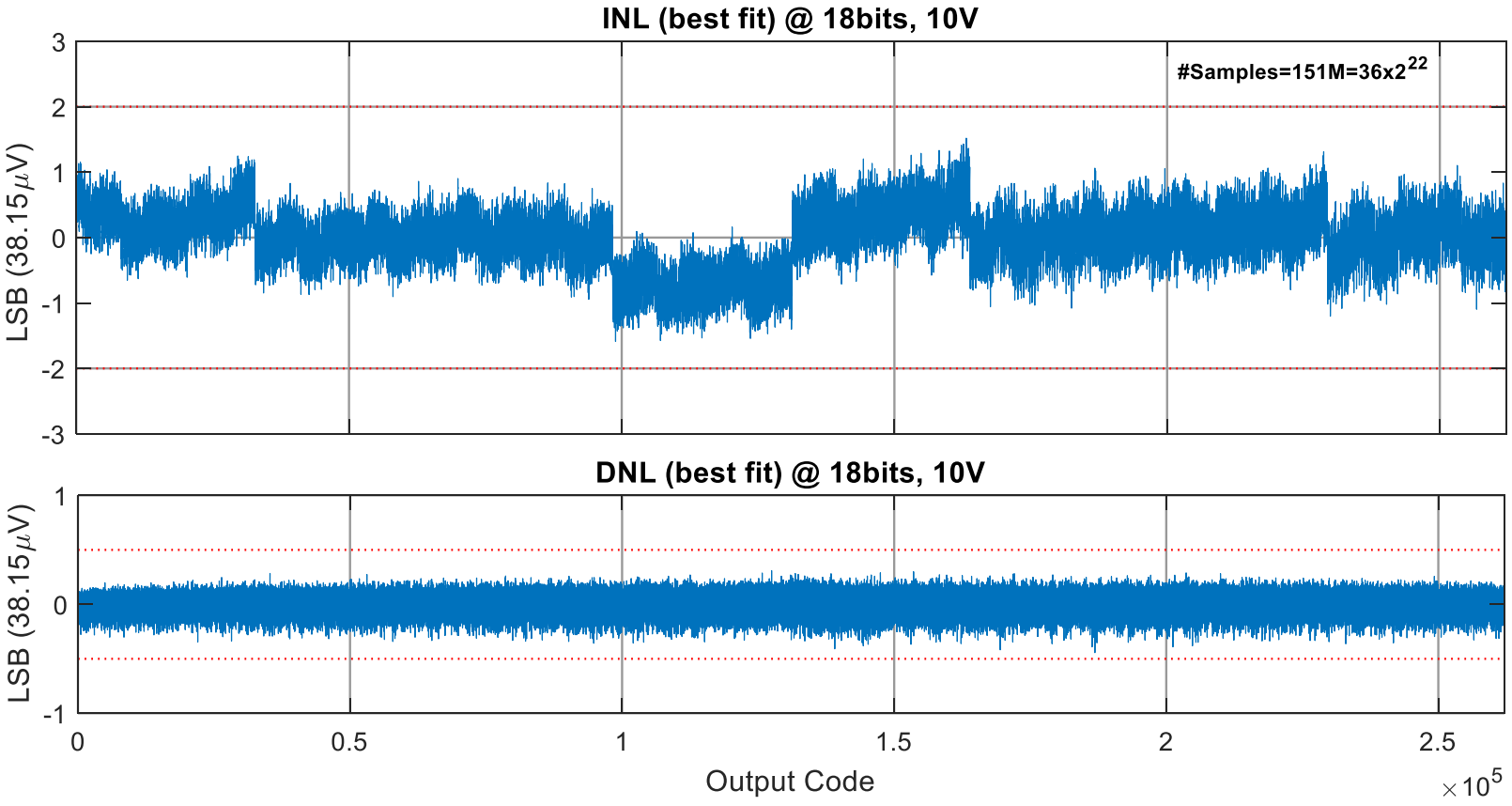
Analog ATE: Applicos ATX7006

- Fully integrated data converter test solution with very high accuracy, low noise and fast sampling features for low speed high accuracy testing to high speed medium accuracy testing.
- Fully synchronization exists between wave generators and the digital capture module.
- The analog test signal was generated using the AWG22 module which is a 22-bit Arbitrary Waveform Generator (AWG). The update rate is DC-2Msps with a bandwidth of DC-500kHz. Analog signal of 1kHz comes out filtered by a 4-pole 12-kHz Butterworth LP filter integrated in AWG.
- Digital module DIO captures with a depth of 4Mx24-bits serial words. The data capture rate is DC-50MHz.

EXPERIMENTS: RESULTS AND METHODS COMPARATION

Histogram test

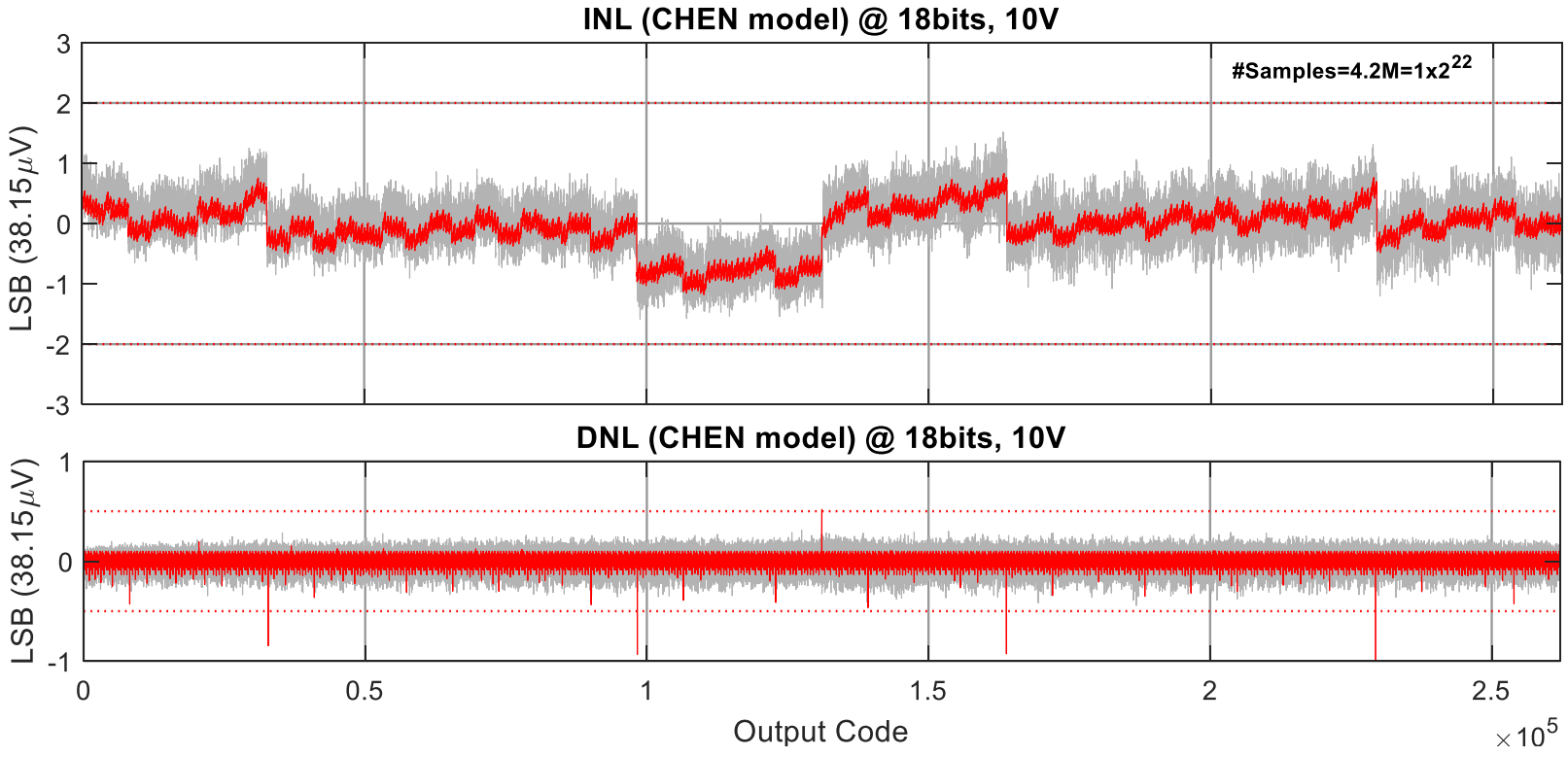
36 x 2^22=151 millions samples, no socket



EXPERIMENTS: RESULTS AND METHODS COMPARATION

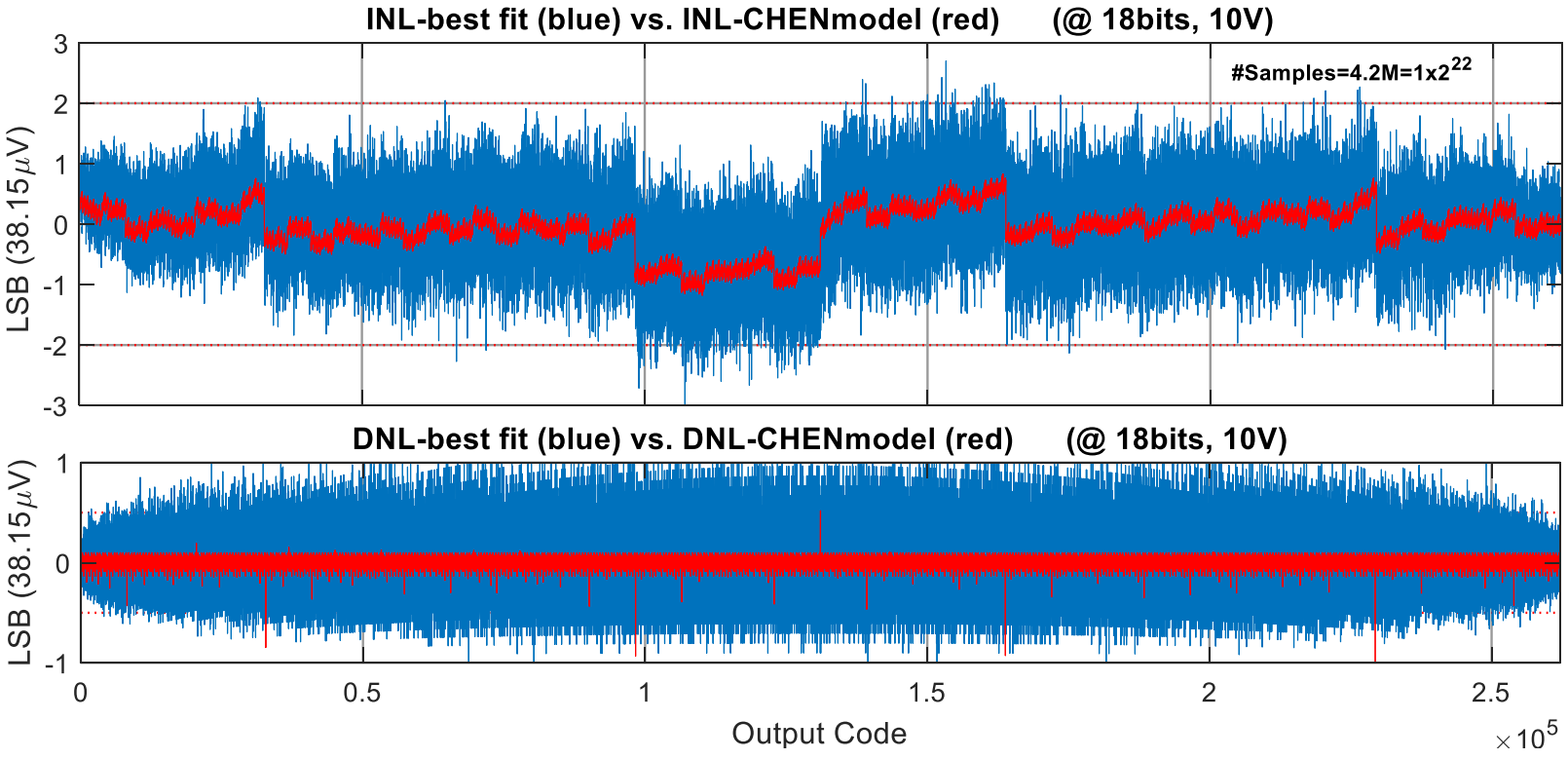
Improved method test based in Chen model

1 x 2^22=4.2 millions samples, no socket



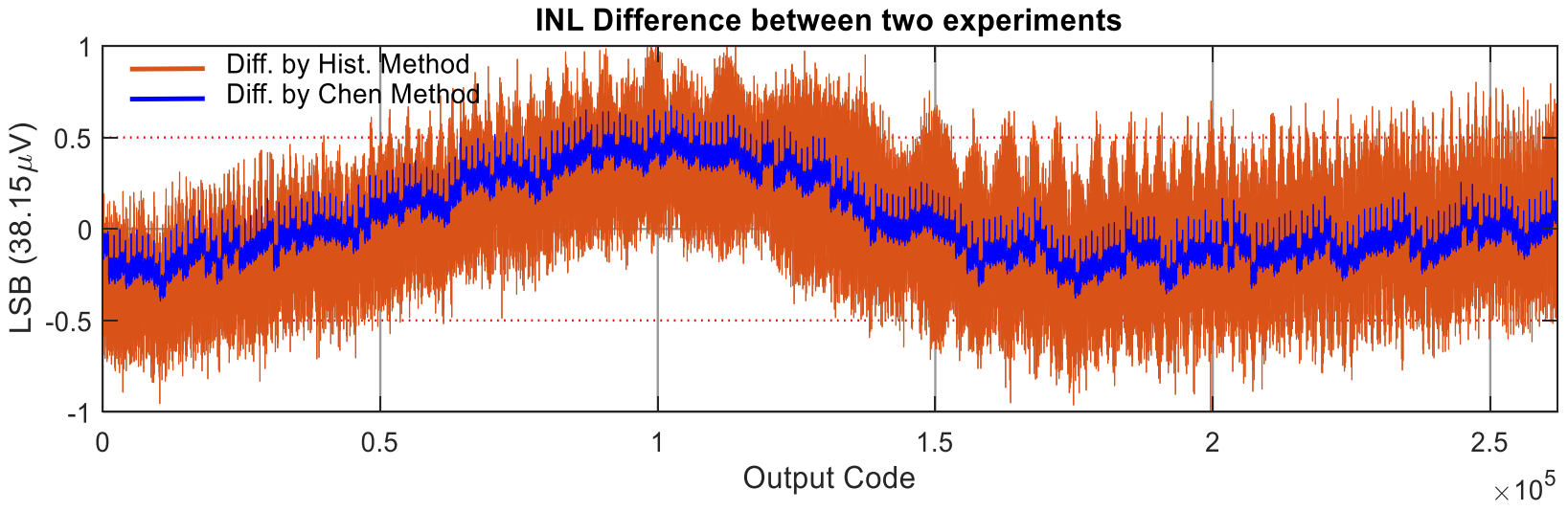
EXPERIMENTS: RESULTS AND METHODS COMPARATION

Comparison between methods when using the same amount of samples, no socket



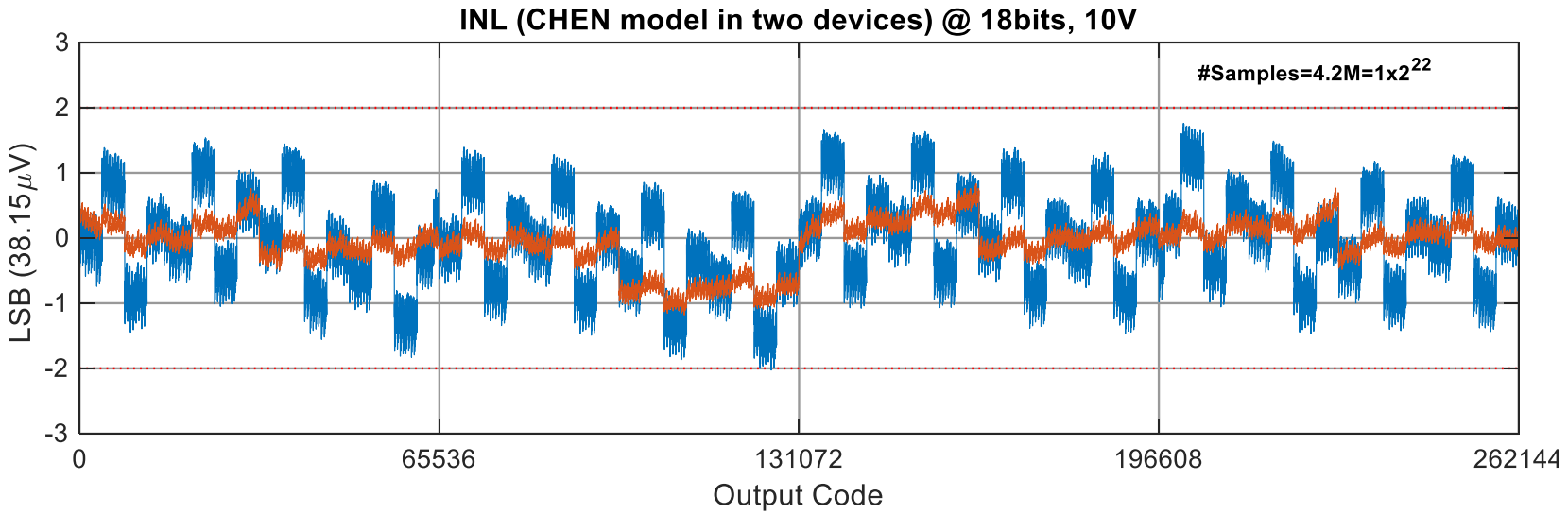
EXPERIMENTS: RESULTS AND METHODS COMPARATION

Comparison between methods against PCB configuration changes (digital supply filtering), no socket



EXPERIMENTS: RESULTS AND METHODS COMPARATION

Comparison between results of the improved method with and without using socket



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CONCLUSIONS

1. In high resolution ADCs, performing linearity test using the standard histogram method implies obtaining a large number of samples per code in order to average the measurement noise.
2. This leads to long test time which involve high test costs. Space applications nowadays are trending to the use of COTS devices for cost saving purposes. This is aligned with a reduction in the cost of testing such COTS components.
3. The present work has shown that it is possible to reduce the cost of the linearity test reducing the number of necessary samples. This is done by improving the noise averaging efficiency by using the very accurate input signal information dismissed in the accumulation of the histogram, redistribute the contribution of noise average to all samples and taking care of the high dependence behavior of segmented architectures of some types of high resolution ADCs.

THANK YOU!