Static Linearity Test for Radiation Effects Characterization of an 18-bit SAR Serial IO COTS ADC: Analog Devices AD7982

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Abstract

This paper reports the testing results of a Successive-Approximation-Register (SAR) ADC of 18-bits with Serial Input/Output digital interface. We compare the results of using a standard approach with a new test methodology for SAR static linearity testing. The available test time in between radiation steps is limited in order to avoid annealing. The presented method strongly reduces the amount of output code samples, which implies not only higher test speed but also lower test cost.

I. Introduction

The Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL) are both some of the most important static parameters that must be known to insure the correct operation of an ADC in a certain application. The Histogram Method [1] is one of the standardized method to obtain the static performance of the ADC, achieving a very precise result independently of the type of its transfer function. But the high cost of its application, due to large number of samples that must be acquired (that increases, in general, in an exponential way with the converter resolution) and the requirement of a sufficiently linear input source, makes the Histogram Method expensive and time-consuming for the test of high-resolution ADCs, especially in the Space Industry area where today time and cost are key elements that demand for solutions that allow rapid and simple adaptation of commercial components to be used in space systems, the Commercial Off-The Shelf (COTS) components.

Many works have been proposed to solve the mentioned histogram test drawbacks. Some works are based on the use of spectral processing [2]-[6], where the number of samples to be taken, and the test time, is drastically reduced, but they require a high purity sinusoidal input. Other works [7]-[10] suggest methods for relaxing the input signal generator linearity, using two related nonlinear stimuli. In [7] the non-linearity inserted by the stimulus is identified and removed (SEIR) exciting the ADC with two identical non-linear ramps with a voltage offset between them. [8] includes modifications for a test environment where time drifts are not negligible. In [10] the authors introduce a simple and general algorithm based on SEIR but independent of the test signal waveform and adapted to a non-stationary test set-up.

This paper shows the non-linearity results obtained by the application of a modified test methodology based on [11] to the commercial 18-bit SAR AD7982 converter of Analog Devices [12]. It uses a segmented non-parametric integral non-linearity model that dramatically reduces test data and achieves better precision than the standard histogram test.

Section II presents the used algorithm. Section III describes de ADC DUT to be tested. Section IV depicts the measurement setup. Section V displays the experiments results and comparison with a standard method. Section VI provides the conclusions. Finally, section VII expresses the acknowledgements.

II. Test Methodologies

A. Sinewave Histogram Test

The sinusoidal Histogram Method [1] consists in stimulating the ADC with a pure sinusoidal signal that slightly saturate the output. The digital output codes are then accumulated in code bins forming a histogram, each bin corresponding with an output code. The accumulation in the code bins are then compared with the expected occurrences of an ideal ADC of the same resolution when excited with a sinusoidal. The difference indicates the non-linearities of the converter.

B. Improved Efficiency Algorithm

The improved algorithm [11] exploits three main factors: 1) the amount of truly independent error sources contributing to linearity errors is much lower than the number of code bins to be tested; 2) all sampled codes are valid to estimate the ADC parameters. Noise is rejected by the algorithm itself; 3) Integral Non-Linearity accept a mathematical segment model, i.e. INL curve is a collection more or less complex of rectilinear segments without continuity restrictions between them. This way, DNL is a discrete collection of positive and negative spikes corresponding to the discontinuity jumps between segments.

The methodology is especially appropriate for high resolution high linearity ADCs as SAR, Pipeline and Cyclic ADCs, which present such a kind of segmented non-linearity error. In actual high-resolution ADCs, segmentation pattern of INL can be practically described using a few (2 to 5) levels of

segmentation model. Algorithm [11] used here, only apply a three level model.

Consider the *r*-bit binary word of output code, *Z*, of our ADC under test is written as:

$$\begin{aligned} Z &\equiv \{b_{17}, b_{16}, ..., b_3, b_2, b_1, b_0\} \\ &\equiv \underbrace{\{b_{17}, b_{16}, ..., b_{11}, b_{10}\}}_{Z_M} \| \underbrace{\{b_9, b_8, ..., b_4, b_3\}}_{Z_I} \| \underbrace{\{b_2, b_1, b_0\}}_{Z_L} \end{aligned} \quad (1)$$

where a resolution of r=18 bits is used to exemplify the model, and the symbol '||' represents the bit-word concatenation operation.

Code Z is expressed in terms of three subcodes. A Most significant code, Z_M, an Intermediate significant code, Z_I, and a Least significative code, Z_L, with respectively resolution of r_M=8, r_I=7, r_L=3 bits $(r = r_M + r_I + r_L)$.

Segmentation model of INL assumes that the curve $INL(Z)$ has the following functional form:

$$INL(Z) = f_M(Z_M) + f_I(Z_I) + f_L(Z_L), \quad Z \in [1, 2^r - 1] \quad (2)$$

i.e. the INL is the sum of three functions which depend each one on one subcode of partition in (1).

This model implies that:

- $f_M(.)$ is a discrete function of $(2^{r_M} - 1)$ values, corresponding to all different values of Z_M excepting 0 (INL(0) is undefined);
- $f_I(.)$ is a discrete function of $(2^{r_I} - 1)$ values, and
- $f_L(.)$ is a discrete function of $(2^{r_L} - 1)$ values.

Therefore, in the case of (1), INL results in a discrete function of $(2^r - 1) = 262143$ values but determined only by 255+127+7=389 parameters, those that define the sub-functions in (2).

Algorithm in [11] provides an identification method to extract the values of sub-functions in (2). In this work, we use the same procedure but extended to take into account all levels of signal up to ADC saturation.

III. Device Under Test

The Device Under Test (DUT) is a commercial 18-bit Serial IO Analog to Digital Converter AD7982 of Analog Devices [12]. This converter is a Successive Approximation Register (SAR) type with no missing codes, maximum |INL| = 2.0LSB and DNL=-0.85LSB to +1.5LSB. It has a differential input range of 10Vpp and no pipeline delay. This device uses a serial peripheral interface which is SPI/QSPI/MICROWIRE/DSP compatible. The chosen package to be tested is the 3mmx3mm 10-Lead LFCSP.

This component in particular is to be qualified for its use in the Juice Icy Moons Explorer (JUICE) mission of the ESA. This kind of high resolution ADCs with serial interface is considered to be in line with the future trend of mixed-signal philosophy for space [13]. Not only by the reduction of cost implied by the use of COTS components, but also because the serial IO allows for simply swapping pin-to-pin compatible ADCs of different characteristics such as resolution, linearity, etc.

IV. Measurements Setup

The setup consists on a PCB board, a programmable power supply, an Applicos ATX7006 Analog ATE [14] and a PC, see Fig. 1.

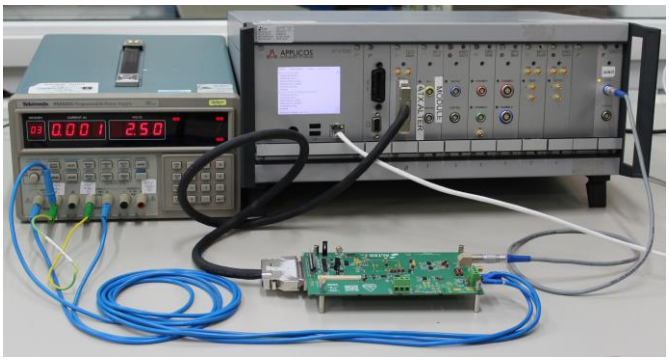

Fig. 1. Setup photograph

A. Hardware

The precision analog signal generation and digital codes capture are performed via an analog ATE which is connected to the DUT through a PCB board.

1) PCB Board

The board has been developed custom made for this application. It includes a reference, a signal conditioning circuit and power supply circuitry, see Fig 2.

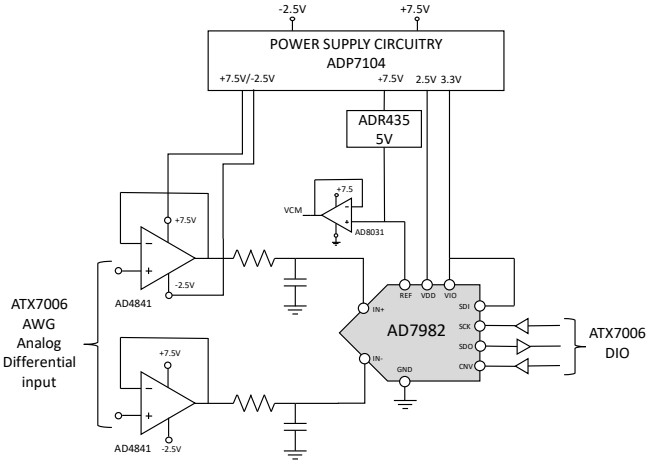

Fig. 2. Simplified Board Block Diagram

The configuration for the DUT is fully differential, and it can be inserted by soldering or with a socket in order to make comparative analysis, see Fig. 3 and 4.

The reference of the ADC is provided by a high precision ultralow noise with temperature drift curvature correction and extra implanted FET (XFET) 5.0V reference (ADR435B). Additionally, the reference source is capable of sourcing up to 30mA and sinking -20mA.

The signal conditioning circuit includes two unity gain stable, low noise (2.1nV/$\sqrt{\text{Hz}}$), low distortion and rail-to-rail output op amps (ADA4841). Both amplifiers are set at midscale

by the use of a reference voltage divider (590Ω) buffered by a rail-to-rail, high speed and fast settling amplifier (AD8031).

The power supplies are decoupled at the insertion in the test board and at each device. A single ground plane is applied to minimize the effect of high frequency noise interference.

The analog signal source is provided via a LEMO serie B connector to interface with the connection cable coming from ATX7006 Arbitrary Wave Generator (AWG).

The digital input/output is connected using a 68 SCSI connector with the Digital Input/Ouput (DIO) module of the analog ATE. The connection is made in single-ended low speed mode.

The DUT is not capable of driving the load implied by the SCSI connector and cable of the ATE digital interface. Therefore, the serial communication from the ADC to the digital capture circuitry of the ATE is performed via a digital buffer (SN74LVC126).

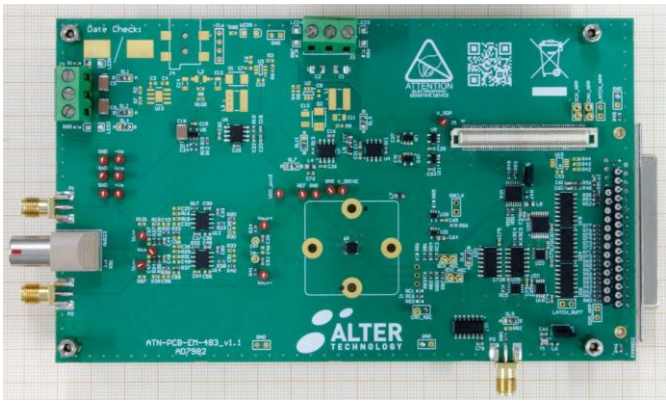

Fig. 3. PCB Board photograph with solded DUT

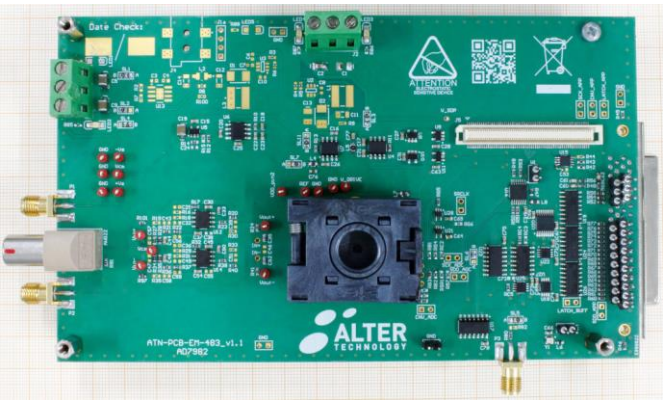

Fig. 4. PCB Board photograph with socket

2) Analog Generator and Digital Capture: ATE Applicos ATX7006

As already mentioned, the test setup included in this work contains as the input analog generator and digital signal capture the Applicos ATX7006 ATE test system, see Fig. 5, a fully integrated data converter test solution with very high accuracy, low noise and fast sampling features.

Generator and digitizer modules cover the range from low speed high accuracy testing to high speed medium accuracy testing. Auxiliary modules also provide linear reference and supply voltages, low jitter clocks and digital IO.

The ATX-series chassis use a well-considered grounding scheme that includes isolating noise on the backplane ground from the analog hardware.

A fully synchronization exists between wave generators and the digital capture module. The test signal was generated using the AWG22 module which is a 22-bit Arbitrary Waveform Generator (AWG), which includes output impedance lower than 1Ω and non-linearity of maximum ±3ppm of range. The update rate is DC-2Msps with a bandwidth of DC-500kHz. Analog signal of 1kHz comes out filtered by a 4-pole 12-kHz Butterworth LP filter integrated in AWG.

The capture of the digital data is performed by the digital module DIO with a depth of 4Mx24-bits serial words. The data capture rate is DC-50MHz. The capture of the digital data is fully synchronized with the analog source via pattern generator that controls both the analog generation and digital capture timings.

Fig. 5. Applicos ATX7006 front view

B. Software

The software has been developed in Visual Studio C#. The software communicates with the driver via Ethernet to obtain custom made behavior from a set of optional commands.

In this case, the software indicates the ATE to generate slightly saturated sinusoid excitations. The ATE has a limitation of 4Mwords to be capture in every register. To overcome this, the capture process is repeated to obtain a longer data set. However, these excitations are changed in phase, which is not directly allowed by the provided software. This avoid obtaining the same points of the equivalent sinusoid but repeated due to the full synchronization analog-to-digital of the system and coherent sampling. After the measurements have been run, the digital captured data of 4M words each register are retrieved and stored in a PC. Later, these results have been mathematically processed with Matlab.

V. EXPERIMENTS

In the experiments, a set of 36 registers of 4MSamples has been taken. The sinusoidal histogram test has been computed using all the registers, which implies an amount of 151 million of samples. In comparison, in the improved model it has only been used 1 register, which implies 4 million of samples. We can observe in Fig. 6 and 7 that despite of using a much lower number of samples, the improved model results are more adjusted and contain a less noisy behavior.

Fig. 8 shows a comparative of the methods under the same conditions, both using a single register of 4 million of samples.

It is noticeable that the noise averaging of the non-parametric segmented model is superior.

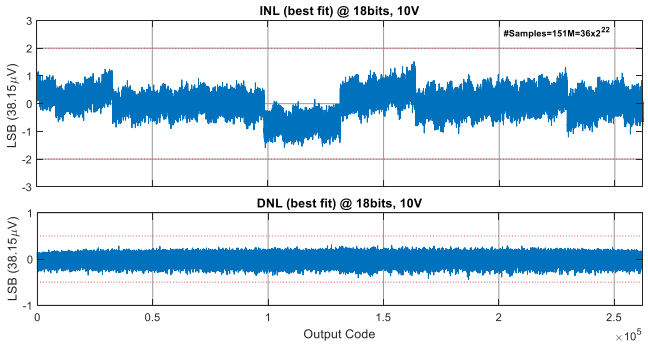

Fig. 6. Linearity test results of histogram method using 151MSamples

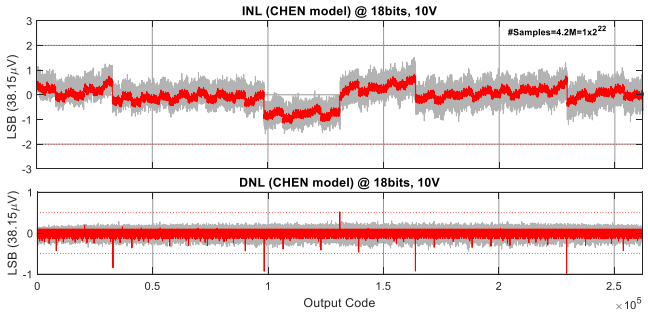

Fig. 7. Linearity test results of improved method using 4.2MSamples

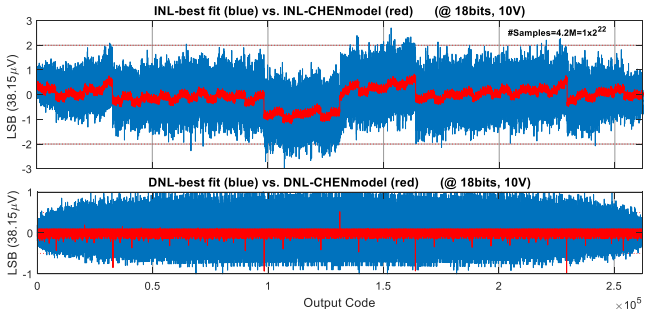

Fig. 8. Comparative of linearity test methods using 4.2MSamples

In Fig. 9 is shown the difference between different INLs when obtained with the two methods. The subtracted INLs has been obtained with two different configurations when filtering the digital power supply. We can observe that the stability against slight experiment conditions changes is better in the improved model than in the standard histogram method, as the difference between the INLs is more defined.

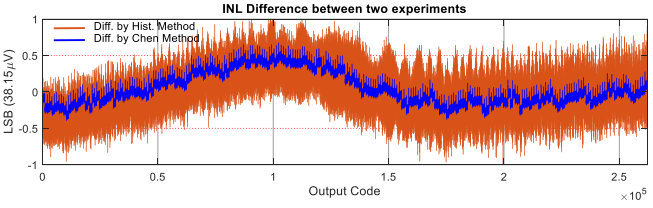

Fig. 9. Comparative of results difference using two different configurations

Fig. 10 shows the obtained INLs with both a solded DUT (orange line) and the use of a socket (blue line). It is noticeable that the improved algorithm is not fixed and can detect strong changes in the circuitry as a change in its linearity. The use of sockets can imply a great impact when testing this kind of components due to the support circuitry needed [15].

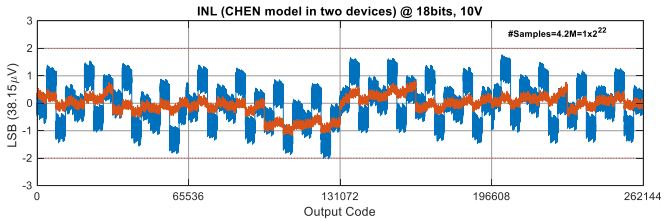

Fig. 10. Comparative of INL results of improved method with a without socket

VI. Conclusions

In high resolution ADCs, performing linearity test using the standard histogram method implies obtaining a large number of samples per code in order to average the measurement noise. This leads to long test time which involve high test costs. Space applications nowadays are trending to the use of COTS devices for cost saving purposes. This is aligned with a reduction in the cost of testing such COTS components. The present work has shown that it is possible to reduce the cost of the linearity test reducing the number of necessary samples. This is done by improving the noise averaging efficiency by using the very accurate input signal information dismissed in the accumulation of the histogram, redistribute the contribution of noise average to all samples and taking care of the high dependence behavior of segmented architectures of some types of high resolution ADCs.

VII. Acknowledgements

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References

[1] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," in IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000) , vol., no., pp.1-139, Jan. 14 2011. doi: 10.1109/IEEESTD.2011.5692956. URL:http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5692956&isnumber=5692955

[2] F. Attivissimo, N. Giaquinto, I. Kale; "INL reconstruction of A/D converters via parametric spectral estimation"; *IEEE Transactions on Instrumentation and Measurement*, Vol. 53, Issue 4, Aug. 2004, pp940-946.

[3] F. Adamo, F. Attivissimo, N. Giaquinto, M. Savino; "Measuring the static characteristic of dithered A/D converters"; *Measurement* 32 (2002) Elsevier, pp.231-239.

[4] V. Kerzerho, S. Bernard, J.M. Janik, P.Cauvet; "Comparison between Spectral-Based Methods for INL estimation and feasibility of their implementation". *IEEE International Mixed-Signal Testing Workshop*, June 2005, pp.270-275.

[5] A. C. Serra, M. F. Silva, P. M. Ramos, R. C. Martins, L. Michaeli, and J. Saliga; "Combined Spectral and Histogram Analysis for Fast ADC Testing"; *IEEE Trans. Instrument. and Measurement*, Vol.54, No. 4, August 2005, pp. 1617-1623.

[6] E. J. Peralías, M.A. Jalón, A. Rueda; “Simple Evaluation of the Non-Linearity signature of an ADC using a Spectral Approach”; *VLSI Design*, Volume 2008, Article ID657207.

[7] Le Jin, Kumar Parthasarathy, Turker Kuyel, Degang Chen, Randall L. Geiger; “Accurate Testing of Analog-to Digital Converters using Low Linearity Signals with Stimulus Error Identification and Removal”; *IEEE Trans. and on Instrum. And Meas*., Vol.54, No.3, June 2005, pp.1188-1199.

[8] Le Jin, Kumar Parthasarathy, Turker Kuyel, Degang Chen, Randall L. Geiger; “High-Performance ADC Linearity test Using Low-Precision Signals in Non-Stationary Enviroments”; *IEEE International Test Conference Proceedings*, Nov. 2005.

[9] E. Korhonen and J.Kostamovaara; “An improved algorithm to identify the stimulus in histogram-based A/D converting testing*”; Proc 2008 13th European Test Symp*. May 2008, pp.149-154.

[10] M.A. Jalón, E. Peralías; “ADC Non-Linearity Low-Cost Test through a Simplified Double-Histogram Method”; *Journal of Electronic Testing, February 2010, Vol. 26, Issue 1, pp. 47-58*

[11] Z. Yu and D. Chen, "Algorithm for dramatically improved efficiency in ADC linearity test," 2012 IEEE International Test Conference, Anaheim, CA, 2012, pp. 1-10. doi: 10.1109/TEST.2012.6401561. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6401561&isnumber=6401510

[12] Analog Devices AD7982 Datasheet URL: http://www.analog.com/media/en/technical-documentation/data-sheets/AD7982.pdf

[13] R. Bedi, “Serial I/O ADCs/DACs: The Next Giant Leap in Mixed-Signal for Space”, 6th International Workshop and Mixed-Signal Integrated Circuits for Space Applications (ESA’s AMICSA 2016).

[14] Applicos ATX7006 ATE URL: http://www.atx7006.com/

[15] M. Murnane, C. Augusta, “Understanding PulSAR Support Circuitry”, URL:http://www.analog.com/media/en/technical-documentation/application-notes/AN-931.pdf.