Prototype of a Multi-Mode C-Band Capable 12-bit 1.5/3/6 GSps Quad ADC in Flip-Chip Non-Hermetic Technology

R. Pilard, M. Martin, B. Dervaux, K. Salmi, G. Wagner, J.-P. Peltier, D. Bellin, V. Monier, N. Chantier

Teledyne e2v, 4 rue de Rochepleine, 38120 Saint-Egrève, France

romain.pilard@teledyne-e2v.com

Abstract

Teledyne e2v has developed a new 12-bit 1.5/3/6 GSps quad ADC on STMicroelectronics BiCMOS9 technology, and assembled in Flip-Chip non-hermetic technology.

This device is C-band capable embedding a cross point switch for flexibility and chaining capabilities for multi-component synchronization and clocking.

The BiCMOS technology used features 130nm CMOS and SiGeC NPN HBT bipolar technology (Ft/Fmax = 166/175 GHz).

The device is assembled in a non-hermetic flip-chip CBGA package using HiTCE glass ceramic material in order to reach optimized RF performance and higher pin density.

I. Context

Satellite-based applications like telecommunication, earth observation and navigation increasingly demand more flexibility [1] in terms of utilized capacity, performance and mobile usage. At the same time satellite constellations are getting more complex in order to meet these flexibility demands [2]. Emerging satellite systems therefore use intelligent communication payloads based on capable on-board signal processors. These should be able to interface effectively to complex antennas, flexibly generating hundreds of traffic beams or inter-satellite connections and handling multi-GHz processed bandwidth per port.

Payload systems performance is directly linked to the performance of components used at every stage of the signal chain within the satellite payload: starting from the reception antenna followed by low-noise amplifiers to the final transmission antenna, through the analogue-to-digital conversion, digital processing and the digital-to-analogue transfer stages. Two components are of key importance here because they have a direct effect on signal quality at receive (Rx) and transmit (Tx) side and therefore are key enablers of the global system performance: the analogue-to-digital and digital-to-analogue data converters (ADC and DAC). Within this context, Teledyne e2v has developed a new quad 12-bit 6GSps ADC in the frame of a European H2020 program. This ADC is capable to reach a high integration level with more channels on a board, low power consumption, large bandwidth and high dynamic performance.

This paper is composed of six parts. A first section will present the market trends in which the ADC has been developed for. Then an overview of the product is proposed and details of the multiple-component chaining features are presented. The fourth section is dedicated to the packaging technology used for the ADC. Then radiation hardening techniques employed are revealed. In the last section, first measurement results are shown.

II. Market Trends

The space market evolves with a growing variety of reliability requirements and an increasing variety of system architectures as the usage of digital signal processing techniques on microwave signals continuously expands its range of applications in space systems [3].

Consequently, the prototype ADC is built to be delivered in several reliability grades. And from the onset, this new ADC has been defined to be a multi-purpose device designed and architected to digitize broadband microwave signals in a broad variety of system implementations. Its unique Cross Point Switch in the input stage is a fundamental part of its multi-purpose nature.

Additionally, the C-Band capability of the ADC supports the market trend to simplify RF receiver signal chains with direct digitization of signals in P-, L-, S- and C-band, and high IF implementations for system operating in higher bands.

As a result, the engineering efforts needed to adopt a new ADC can then be leveraged on a broad variety of system architectures, including in telecommunications payloads, UWB or multi-band SAR [4], broadband uplink modems, altimeters, high accuracy Lidar systems, GNSS systems and other space payload instruments.

This also contributes to address the growing expectations of short time to market in the space industry.

III. Product Overview

The prototype called EV12AQ600 presented in this paper is a quad channels 12-bit 1.5 Gsps ADC. It is based on STMicroelectronics BiCMOS9 technology featuring 130nm CMOS and SiGeC NPN HBT Bipolar technology (Ft/Fmax = 166/175 GHz) [5]. The built-in Cross-Point-Switch (CPS) allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates. In 4-channel operating mode, the four cores can sample, in phase, four independent inputs at 1.5 Gsps. In 2-channel

operating mode, the cores are interleaved by 2 in order to reach 3 Gsps sampling rate on each of two inputs. In 1-channel operating mode, a single input is propagated to each of the four cores which are interleaved by 4 in order to reach a sampling rate of 6 Gsps. Figure 1 shows the CPS configuration: the ADC inputs (from IN0 to IN3) to the ADC cores (from core A to core D). This high flexibility enables digitization of IF and RF signals with up to 3 GHz of instantaneous bandwidth, up to 6 GHz.

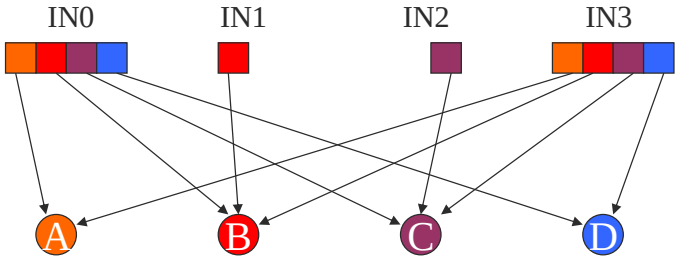

Figure 1: CPS Configuration

Each channel is composed of a single core 4 stages folding interpolation ADC sampling at up to 1.5GSps. Based on an innovative architecture without interleaving, it provides high spectral purity. It offers an analog input bandwidth (-3 dB) of up to 6 GHz with two selectable configurations to optimize SNR performance when working in lower Nyquist zones or linearity performance in higher Nyquist zones. With an extended input bandwidth above 6 GHz the EV12AQ600 allows sampling of signals directly in the C-band (4-8 GHz) without the need to translate the signal to baseband through a down-conversion stage. Figure 2 shows the block diagram of the ADC.

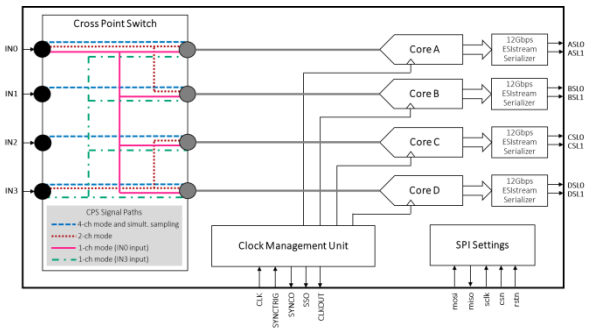

Figure 2: Block diagram

The ADC uses 8 low latency serial lanes at 12 Gbps with ESIstream protocol [6]. Serial lane rate is linked to sampling clock frequency by a ratio of 2, allowing no need of extra PLL, avoiding extra overhead with fractional ratio and being more robust against radiation. The ESIstream protocol is a 14b/16b encoding based on 14 scrambled bits along with 2 overhead bits: clock bit and disparity bit. Applied to the EV12AQ600, the 16 bits frames are as follows (cf. Figure 3):

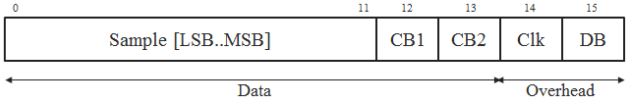

Figure 3: ESIstream frame with EV12AQ600

DB is the disparity bit, CLK the clock bit, CB1 and CB2 are control bits of the ADC and bits 11 to 0 contain the ADC sample. Bits 13 to 0 are scrambled using an LSFR (Linear Feedback Shift Register) that generates the PRBS (Pseudo-Random Binary Sequence).

It also features a novel synchronization method to ease the synchronization of a large number of ADCs. The device is controlled through an SPI interface. All sensitive areas of the device have been triplicated to increase robustness. This includes, but is not limited to, clock circuitry and SPI registers.

IV. Multiple-Component Chaining Features

A method for synchronizing multiple data converters is embedded, already deployed on EV12AD550 [7]. It is based on a daisy chain approach between data converters and one or multiple processing units, i.e. Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). A synchronization pulse is propagated between data converters. The Figure 4 shows a diagram of the interface between multiple data converters and a processing unit.

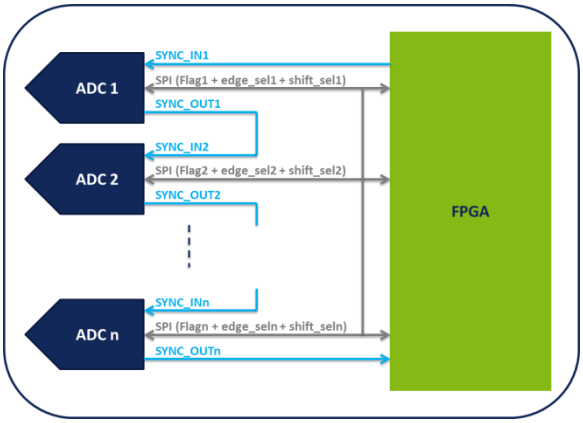

Figure 4: Multiple-device synchronization system overview

Three settings are necessary to manage or configure each ADC:

- Flagx: this signal indicates whether the synchronization pulse is in a meta-stability zone in regards to the clock of the data converter;
- Edge_selx: this signal is configured to choose which edges of the clock of the data converter is used to recover the synchronization pulse;
- Shift_selx: this signal is configured to add a certain number of clock cycle delays to the synchronization of the device after the pulse has been recovered by the data converter

The SYNC_OUT is a copy of the SYNC_IN that is sampled on the reference clock common to all data converters to ensure repeatability of the timings between power-ups and each time the synchronization process is started. Using the three settings, and a training of the system, the different data converters can be synchronized.

Calibration procedure is described in [8].

This synchronization process brings multiple advantages to systems having large count of channels:

- The parameters are accurate between power-ups, synchronization process and printed circuit board based on the same design. This is useful to develop industrial scale system, as the determination of the parameters can be done during prototyping only;
- This method relaxes all layout constraints on the SYNC signal. This means that it can be propagated on one board, or between multiple boards through a backplane which is unavoidable when systems have hundreds of channels to synchronize;
- This method is also compatible with different implementation. The daisy chain shown in Figure 4 is one of them but a tree configuration is possible as well as any hybrid between the two. This brings flexibility to the system;
- Finally, this method does not impact the sampling clock performance. This is essential as some synchronization method adding delays on the sampling clock can degrade its jitter and thus degrade the SNR (Signal to Noise Ratio) performance of the data converters. Communication and wideband radar are two applications which performances are limited by SNR.

In terms of limitations, there are still layout constraints on the reference clock that needs to be time aligned at the input of all the data converters. However, method exists to help either through digital processing or using a slow reference and PLLs to generate the fast clock fed to the high-speed data converters.

Speed wise, this method is limited by the setup and hold time and jitter achievable compared to the reference clock.

The ADC has also an output clock signal provided by the circuit as a clock reference to other ADCs or DACs. This signal is the image of ADC input clock through a buffer, adding some jitter (less than 60 fs rms) to the reference clock. It can be used for ADC chaining (up to 4 components) or clocking a DAC on a same PCB, without significant impact on total converter clock jitter. Clock chaining with multiple ADCs or a DAC is illustrated on Figure **5**.

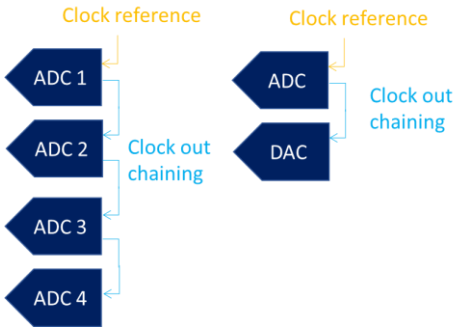

Figure 5: Clock chaining scheme

V. Packaging Technology

For the EV12AQ600 ADC, the choice of FlipChip technology appeared naturally because it is an efficient, effective and reliable device packaging solution.

Indeed, one of the inevitable side-effects of the increased maximum sampling rates and input bandwidth is that the classic configuration of an edge wire-bonded die attached within a package cavity and enclosed by a hermetically sealed lid is no longer feasible, due mainly to the inherent losses and inductances of the bond-wires and their limited distribution to the die.

EV12AQ600 is realised on flip-chip bumped die featuring area-attach. The intermediate multi-layer substrate which accepts the die on one surface and hosts solder balls on the other is fabricated using Low-Temperature Co-fired Ceramic (LTCC) permitting the use of noble metal conductors (Copper instead of Tungsten). Use of conductors made of Copper for example means that the losses at microwave frequencies are minimised and more accurate ultra-broadband impedance matching is possible where required. LTCC also features a high coefficient of thermal expansion which allows the accommodation between the expansion rates of the die and that of the PCB. This condition is a prerequisite for a highly reliable solder joint capable of surviving many hundreds of thermal cycles.

On the bottom side of LTCC substrate, 323 lands allow for solder ball attach. Thus a CBGA323 BGA package is achieved.

A copper heatspreader (Nickel finished) is attached on top with thermal interface material glued to die backside. Walls of the heatspreader are also glued to substrate with venting holes.

Package dimension is 16x16 mm and the ball pitch is 0.80 mm. Pictures of top and bottom views of the packaged device are shown on Figure **6**.

Figure 6: Top and bottom views of packaged device

Package configuration is shown on Figure 7.

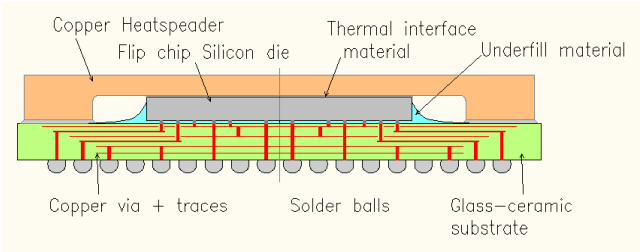

Figure 7: Cross section view of packaged device

Extensive 3D electromagnetic (EM) simulations have been performed using full-wave simulator ANSYS HFSS [9]. These EM simulations enable to predict radio-frequency effects and to assess the target specifications, such as insertion loss from the solder balls to the die bumps, return loss at the

input of the package, crosstalk between inputs, between outputs and between clock input and output. On Figure 8 is shown the 3D view of a part of the package modeled (analog inputs).

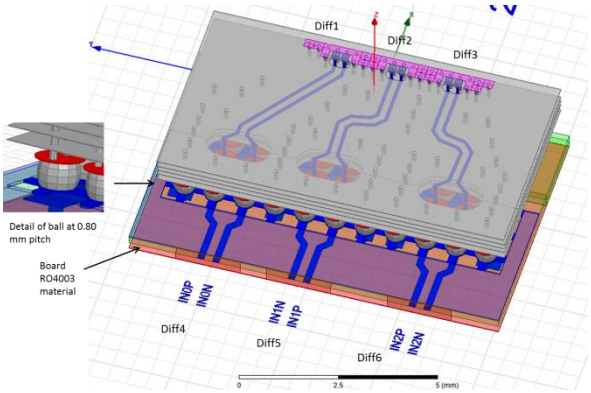

Figure 8: 3D view of a simulated analog inputs

As compared to classic package configuration (ie. wire bonded, hermetic), the EV12AQ600 comes with 2 new features:

- Flip chip
- Non-hermetic

Whereas this type of configuration has been used for many years in other applications, its adoption is quite new for space ones. Apart from technical challenges [10], an important concern was that, a few years ago, Space Standardization did not bring provisions for flip chip devices. Non hermetic flip chip has been introduced in US standards (MIL-STD-883 & MIL-PRF-38535) at the end of 2013 by the addition of the now famous class Y. At the same time, a Working Group (WG) was set up by ESA in order to introduce non hermetic flip chip in ESCC standards (ESCC 9000 & ESCC 2269000). This WG gathered attendees from Agencies, component manufacturers & end users. Those entities were represented by Quality Assurance and / or packaging experts, in order to address both standardization and technical concerns.

Teledyne e2v was granted the leadership of the WG. The group quickly agreed the following guidelines:

- Inclusion of non-hermetic / flip chip in existing ESCC standards (vs inception of fully new standards)
- When possible, consistency with European hybrids & US microcircuits standards, in order to avoid duplication of similar tests
- Addition of requirements for passive add-ons, which are very often associated with flip chip devices

The WG started its work mid 2014 & submitted a proposal to ESCC during fall 2015. Beginning of 2016, this resulted in the publication of ESCC 9000 issue 8 [11] & ESCC 2269000 issue 5 [12].

This achievement has played an important part in the adoption of flip chip for space, through a common reference and language, between agencies, component manufacturers & end users.

VI. Radiation Hardening

ST BiCMOS9 technology does not propose rad hard library. However, first radiation hardened protection assessment has been obtained on EV12AD550 using the same technology and a similar architecture.

Designing a rad hard component requires special cares both in product architecture definition, cells designs, layout implementation in order to either limit the impact of radiation event and/or decrease the event occurrence by increasing the required critical charge threshold to produce an event [13].

A. Layout for radiation considerations

Specific implementation rules have been defined and adapted case to case to limit ionization leakage current propagation into parasitic path.

Some examples of adopted rules:

- NMOS transistor isolation with a P+ guard ring.
- Bulk tie have largely been implanted in order to limit leakage current between transistors.
- Minimization of bulk resistance by placing bulk tie as close as the active device.

For the prevention of latchup, the following rules have been used:

- A deep NWELL NISO is used to isolate the digital blocks and extra substrate ties are added to standard cells to collect radiated charges (cf Figure 9).

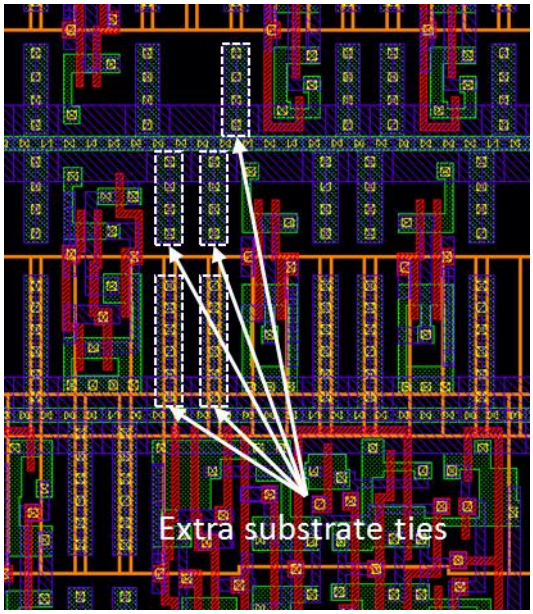

Figure 9: Detail of digital block circuit

- Enlarging minimum space between p and n zones in all analog part and adding deep NISO isolation to reduce radiated charge accumulation, isolating bulk including rail power supplies (cf. Figure 10).

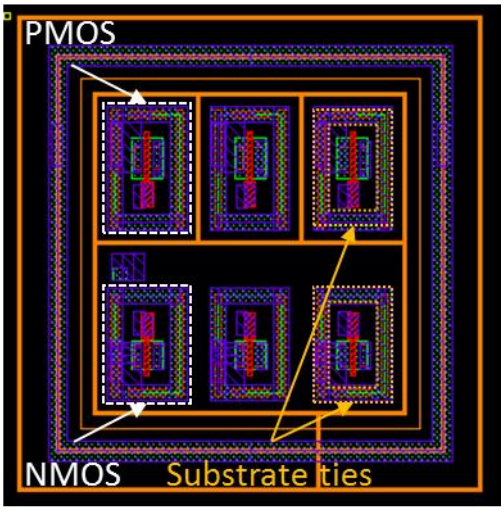

Figure 10: Detail of analog block circuit

- Reduce the serial resistance of the parasite thyristor to prevent from activation.
- Multiply the number of bulks and substrates ties
- Larger of guard ring should not be too much resistive i.e. it is mandatory to not open them.
- Increase minimum distance between guard rings.
- Between NWELL and PWELL it is necessary to put a double guard ring connected to VDD/VSS.

A specific Design Rules Check tool has been developed by Teledyne e2v for superior automation.

B. Design protection approaches

Design protection techniques to prevent occurrence of events include: large drive current of transistors, large transistors, large capacitance.

1) Analog architecture

When possible, analog redundancy has been used. That consists of parallelizing "n" times a circuit and connecting replicated nodes through a resistance to a common node, so that the perturbation effect is divided by "n".

In order to increase node time constant and then increase the parasitic critical charge required to produce a SET, Miller capacitance and/or resistance have been used.

Analog RC filtering is implemented to reduce SET.

2) Digital architecture

The protection of digital blocks is one of the most challenging topics as no rad hard libraries are available. In addition to the layout protection listed above, architecture is optimized by implementing:

- TMV (triple redundancy voting)
- Anti-glitch structure.
- A special mode (SE Protect) has been implemented to strengthen the radiation immunity to Single Event Functional Interrupt (SEFI).

However the drawback of all those protections is that they constrain the performances in terms of power consumption, speed, and size. That is why a specific study has been done on each block in order to protect the most critical nodes.

EV12AQ600 robustness to radiation will be shortly tested with two test campaigns:

- Total Ionizing Dose (TID): due to a BiCMOS process and to test the Enhanced Low Dose Rate Sensitivity (ELDRS), the ADC will be tested at a Low Dose Rate (LDR) of 36 Rad/h, up to 150Krad(Si)
- Single Events (SE): the Texas A&M University (TAMU) facility will be used to evaluate the Single Event Effects (SEE). The Single Event Latch-up (SEL) will be tested up to 80 MeV.cm²/mg without tilt. The Single Event Transient (SET), the Single Event Upset (SEU) and the Single Event Functional Interrupt (SEFI) will be tested up to 92 MeV.cm²/mg (80MeV.cm²/mg with a tilt of 30°).

VII. MEASUREMENT RESULTS

Figure 11 to Figure 13 show typical FFT spectra at frequencies varying from 100 MHz to 2980 MHz. SFDR performance as high as 75 dBFS is obtained at full power in the first Nyquist zone. Lowering input power allow reaching more than 70 dBFS SFDR performance from DC to 6 GHz frequencies.

The EV12AQ600 ADC shows an extremely good spectral purity. As can be seen on Figure 13, the harmonic tail of a 749.9 MHz signal decreases to noise floor very rapidly and no spurs remain in the spectrum.

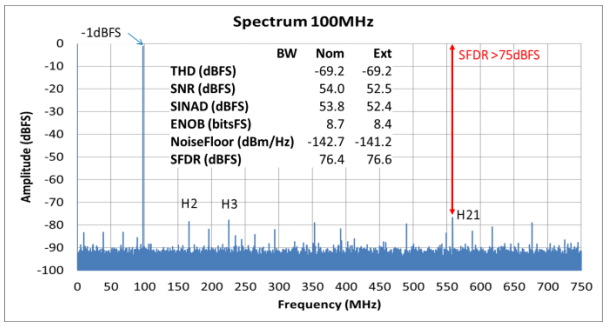

Figure 11: Typical -1dBFS spectrum and FFT computation results @ Fin=100 MHz.

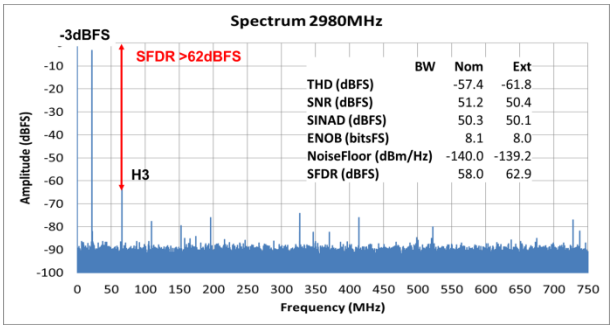

Figure 12: Typical -1dBFS spectrum and FFT computation results @ Fin=2980 MHz.

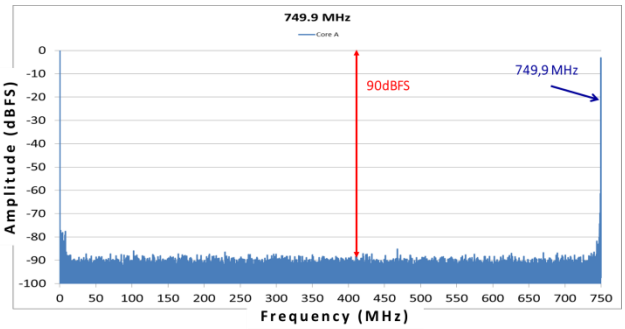

Figure 13: Spectral purity ≥ 90 dB

Figure 14 to Figure 19 show SFDR, SNR & ENOB performance for both -1dBFS and -12dBFS input powers over the full bandwidth (DC to 6 GHz).

The two bandwidth modes available in EV12AQ600 allow adjusting the performance depending of the result sought.

On the one hand, Extended Bandwidth allows for better linearity SFDR for large signals (cf. Figure 14). On the other hand, Nominal Bandwidth, by reducing jitter effect will strongly improve SNR and ENOB for small signal amplitudes (Figure 17 and Figure 19).

The spectrum and performance of a 100 MHz sine wave signal digitized in interleaved mode are shown on Figure 20.

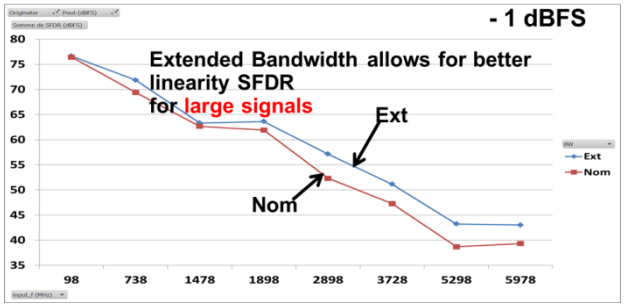

Figure 14: SFDR performance vs frequency @-1dBFS

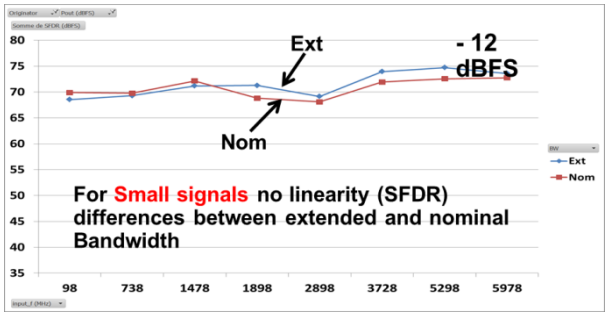

Figure 15: SFDR (dBFS) performance vs frequency @-12dBFS

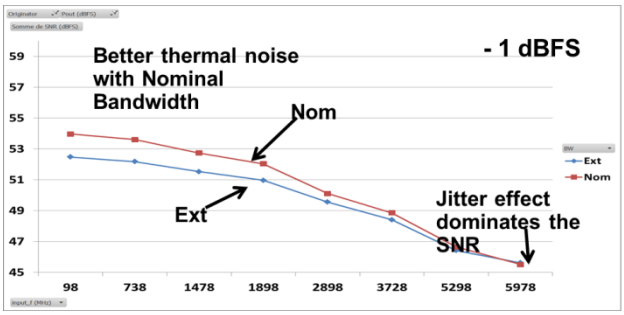

Figure 16: SNR (dBFS) performance vs frequency @-1dBFS

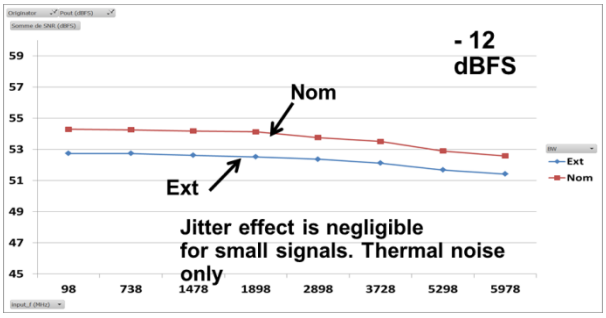

Figure 17: SNR (dBFS) performance vs frequency @-12dBFS

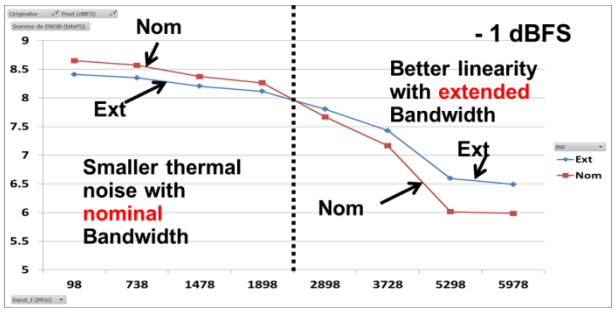

Figure 18: ENOB performance vs frequency @-1dBFS

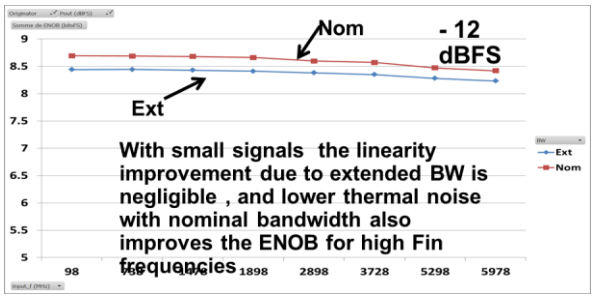

Figure 19: ENOB (Bit_FS) performance vs frequency @-12dBFS

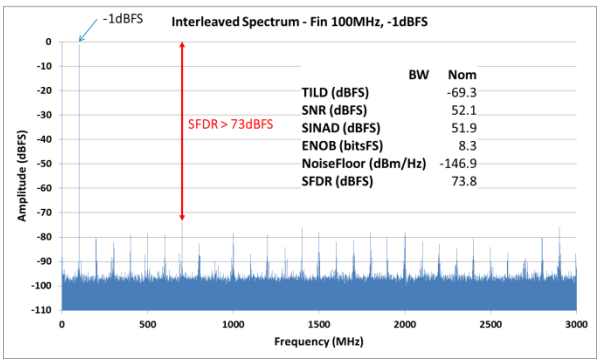

Figure 20: Spectrum and performance in interleaved mode

VIII. Conclusion and Perspectives

A prototype of a quad channels 12-bit 1.5 Gsps ADC has been presented. The ADC is a multi-purpose device designed and architected to digitize broadband microwave signals in a broad variety of system implementations. Its unique Cross Point Switch in the input stage is a fundamental part of its multi-purpose nature to address the growing flexibility demand of next generation satellite systems.

First measurement results have been presented. Further results will come in the near future to cover the entire characterization plan.

In addition, the ADC can be accompanied by a custom interleaving error correction IP provided by Teledyne SP Devices team. It will enhance the performance of the ADC in 1-channel mode (4 cores interleaved) in order to reach unprecedented performance for such a multi-purpose ADC.

IX. Acknowledgments

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This INTERSTELLAR collaborative project led by Teledyne e2v sees a fruitful partnership with Airbus Defense and Space ADS (UK), Fraunhofer IIS (D) and Thales Alenia Space TAS (FR).

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