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AIRBUS

Rad-Hard Telemetry and Telecommand IC suitable for RIU, RTU and ICU Satellite Subsystems

18/06/2018 (11:20 – 11:45)

7th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2018)

17th - 20th June 2018

Agenda

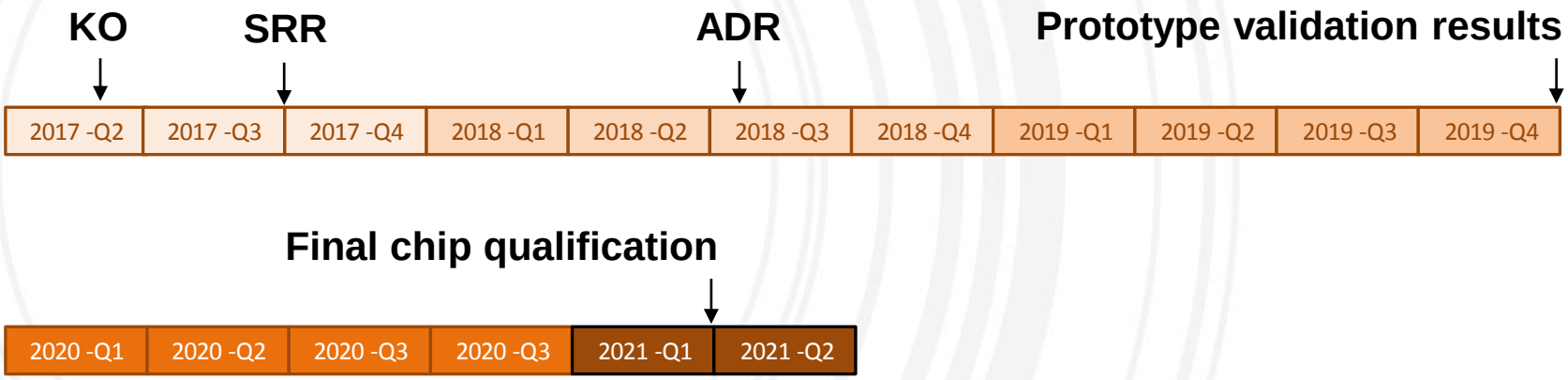
- Introduction
  - Project Overview
  - TM/TC RHIC in a Satellite Spacecraft
  - RIU / RTU and their Modules
- Design Considerations
  - Functionality
  - Challenges
- Architecture Analysis
  - Block Diagram
  - Reused IPs
- Conclusions

Introduction – Project Overview

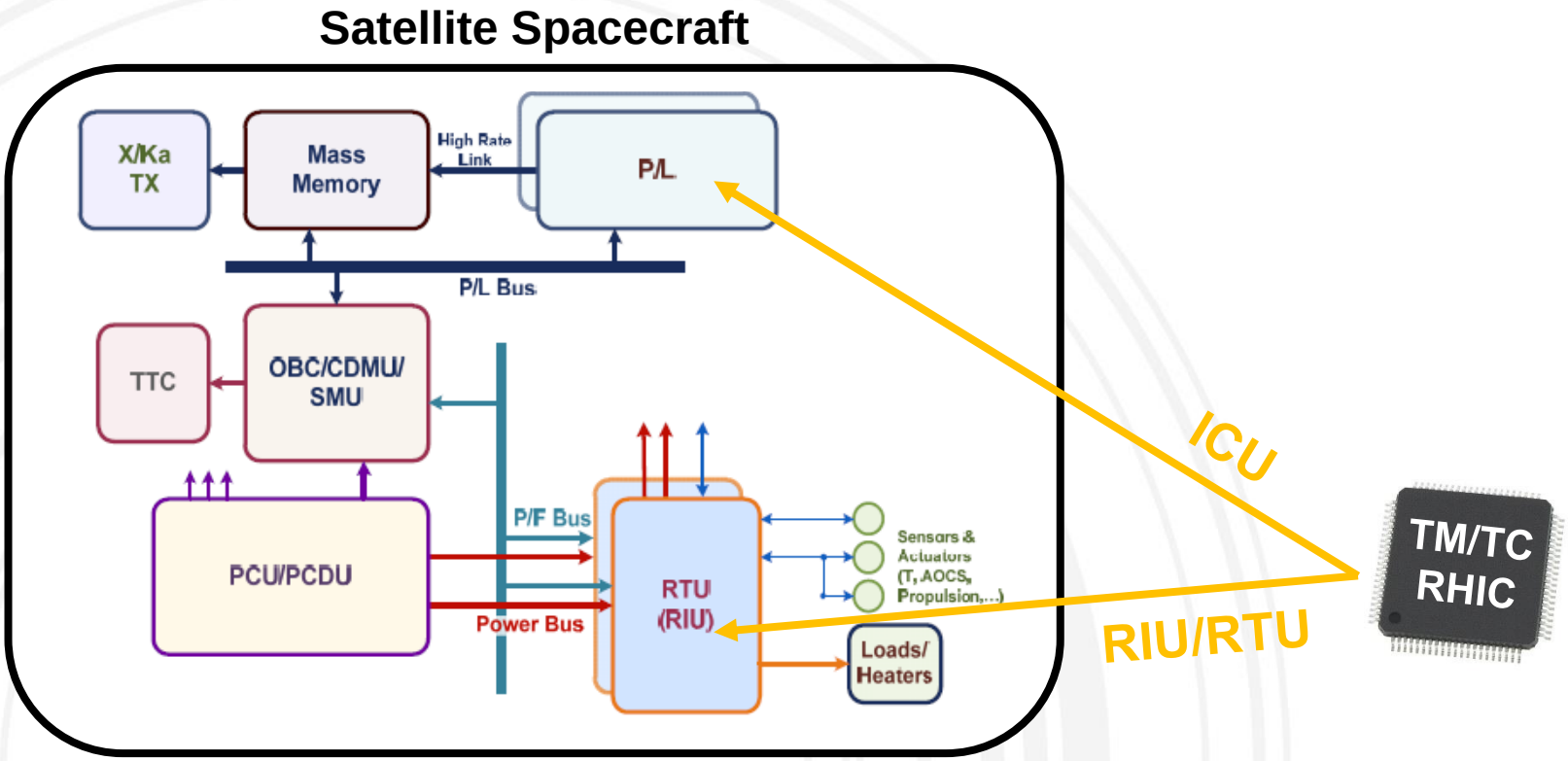
ESA project (GSTP) to achieve a TRL5 design

- Two manufacturing runs
- **AIRBUS** (main final user) in charge of the digital design
- **ARQUIMEA** in charge of the AMS design, overall integration and tests

Project Timeline



Introduction – TM/TC RHIC in a Satellite Spacecraft

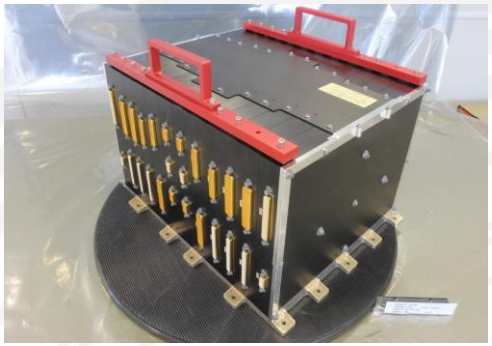


AOCS: Altitude and Orbital Control System
CDMU: Command and Data Management Unit
OBC: On-Board Computer
PCDU/PCU: Power Control (and Distribution) Unit
P/L: Payload

P/F: Peripheral
SMU: System Management Unit
TTC: Telemetry Traffic Control
X/Ka TX: X or Ka band Transceiver

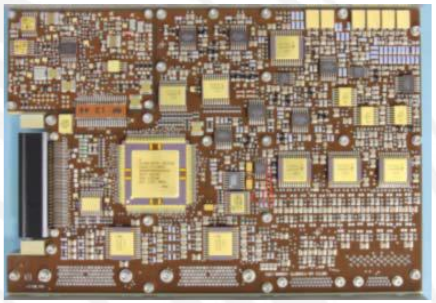
Introduction – RIU / RTU and Modules

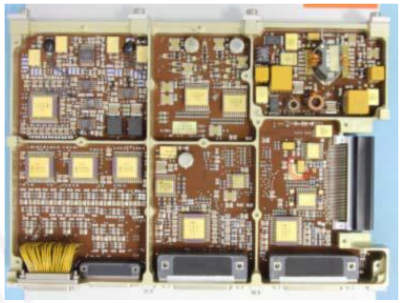
AS1000 RIU



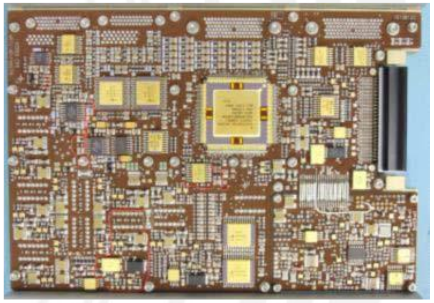
Modular-RTU

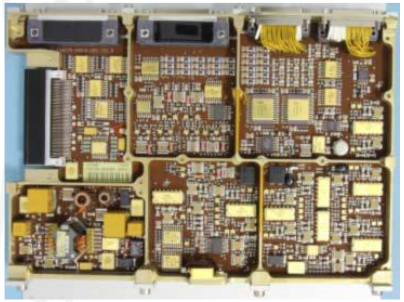
M-RTU Analogue Housekeeping Modules





M-RTU Digital IO Modules





Design Considerations – Functionality (1/3)

Telemetries

- 27/54 differential /single-ended analogue telemetries (limited in band up to 50 kHz) converted to the digital domain.
- Their acquisition sequence is configured on-chip through the SPI.
- Acquired telemetries are stored in a double depth table (consulted through SPI) that collects first and current acquisition.
- Single-ended channels can be biased by means of an on-chip programmable current source (thermistor acquisition).
- Telemetries shall be acquired with a maximum absolute error of 1% in [-55; 125] ºC and 11 ENOB.

Design Considerations – Functionality (2/3)

Telecommands

- 4 telecommands independent between each other
- 3 functions: 1) bi-level, 2) single pulse, and 3) PWM
- 2 bi-level options: 1) independent, and 2) programmed as voltage supervisor
- 2 single pulse configurations: 1) phase and 2) width
- 3 PWM configurations: 1) phase, 2) period and 3) duty cycle

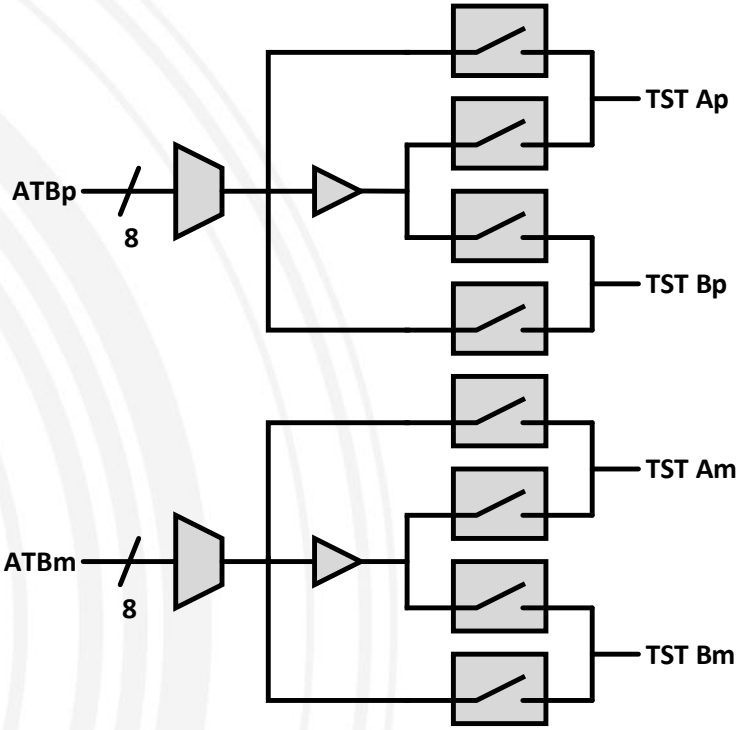
Communication Interface

- Redudant SPI
- Multiple devices sharing the same SPI bus
- Used either for internal configuration and information extraction
- Frequency range: [10 ; 20] MHz

Design Considerations – Functionality (3/3)

Testability

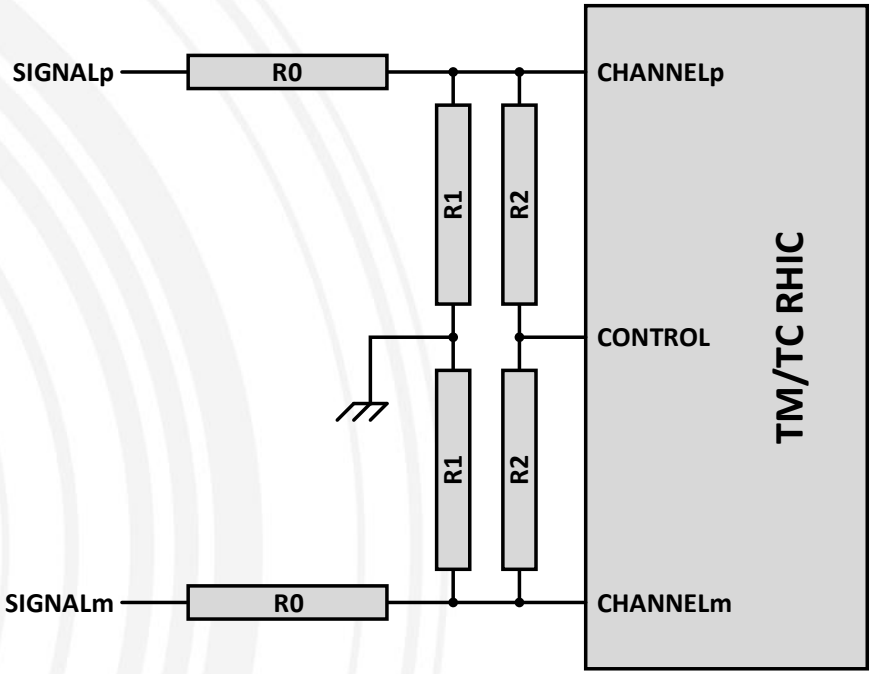
- Required to optimize the development time of a successful design
- Observability of key internal nets and registers is required to confirm the expected design behavior or for debugging it.
- An Analogue Test Bus (ATB) configured through SPI, brings access to differential signal path nets, voltage references, bias voltages and regulated supplies.
- ATB can work in single-ended or differential mode, depending on the nature of the internal net required to be monitored.
- In single-ended mode, ATB allows monitoring two different single-ended nets at once (useful to identify cross-talk or net dependency).
- ATB has two access options by sharing four IO ports with telemetry channels. This implementation allows testing all the telemetry channels without sacrificing any during ATB usage.
- ATB allows disabling and bypassing the analogue voltage buffer at its output, which gives direct access to the selected internal net(s).
- Digital Scan Chain brings access to the internal registers of the digital core through the four IO ports reserved for telecommands (no JTAG interface).



Design Considerations – Challenges (1/2)

Signal ranges above maximum ratings of IO cells library

- Signal ranges at system level exceed the absolute maximum rating of DARE180U IO cells.
- Single-ended signals can be up to the [0; 10] V range.
- Differential signals up to the [-10; 10] V range with a common-mode in the [-1.5 ; 1.5] V range.
- Differential measurements are optimized by means of an internal a common-mode control loop.



Design Considerations – Challenges (2/2)

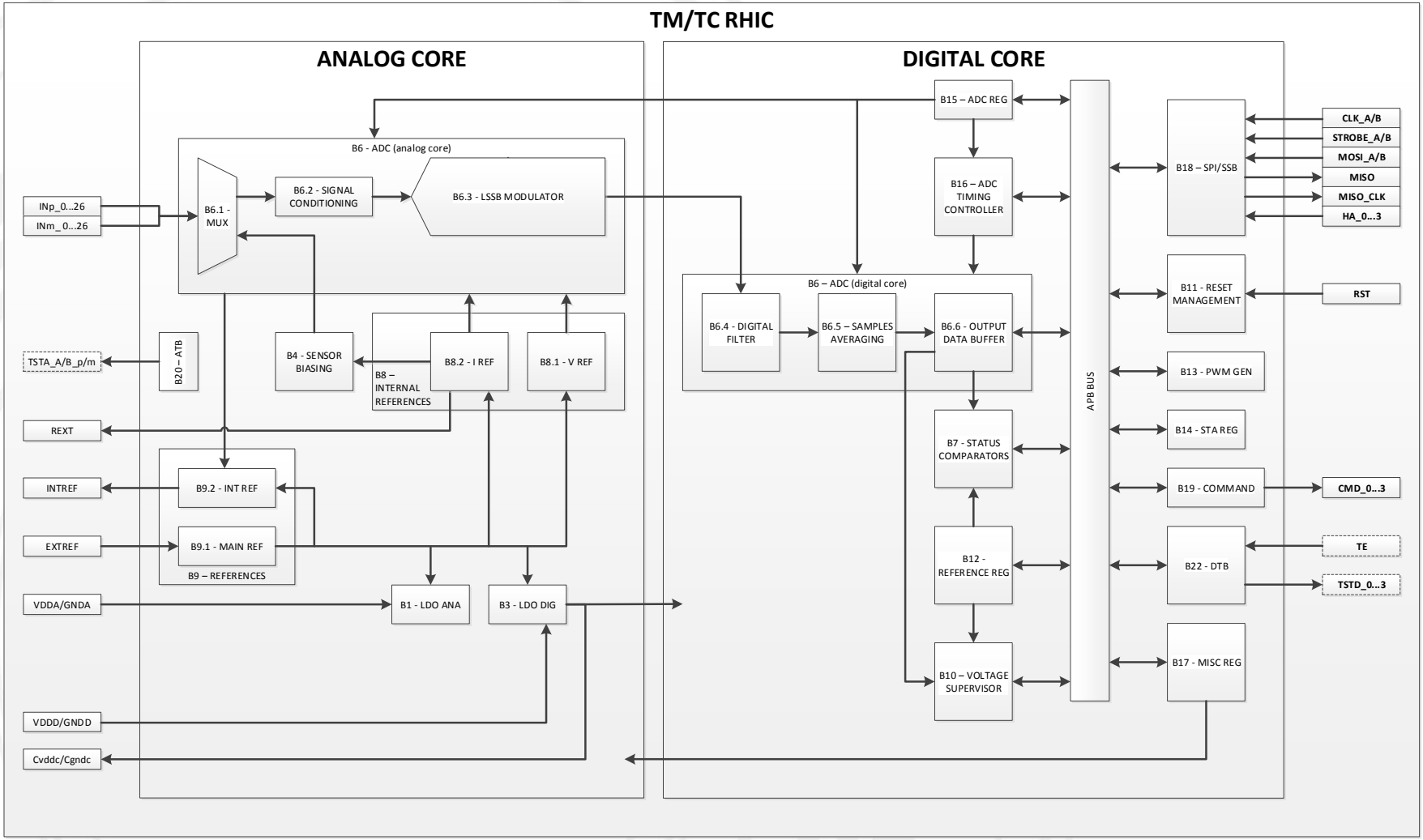
Minimum telemetry latency

- The different nature of the possible telemetries (single ended / differential, biased or not, different voltage ranges, etc.) entails a stabilization period after channel switching.
- Maximum latency of a trustworthy telemetry acquisition shall be quantified and minimized.
- The target fastest acquisition rate is one telemetry acquisition each 10 µs.

Reduced number of IO ports

- Port sharing for testability.
- 84 IO ports (telemetry channel inputs, telecommands, communications ports, analogue references and power supplies)
- 2 pairs of IO ports for the analog supply
- 2 pairs for the digital supply
- 1 pair to provide additional decoupling for the core supply LDO regulator integrated on-chip)

Architecture Analysis – Block Diagram (1/2)



Architecture Analysis – Block Diagram (2/2)

Analogue Core blocks:

B1 – LDO ANA generates the 1.8V analogue core supply from the 3.3V external supply.
B3 – LDO DIG generates the 1.8V digital core supply from the 3.3V external supply.
B4 – SENSOR BIASING provides the bias capability of the telemetry channels.
B6.1 – MUX selects the telemetry channels to be acquired.
B6.2 – SIGNAL CONDITIONNING fits the signal coming from the telemetry channels for the ΔΣ modulator input.
B6.3 – LSSB (ΔΣ modulator) is the first stage of the digital conversion of the acquired telemetry.
B8.1 – V REF generates the internal voltage references for the ΔΣ modulator.
B8.2 – I REF generates the internal current references for the rest of the analogue core blocks.
B9.1 – MAIN REF provides a stable voltage reference for other blocks of the analogue core. This reference can be provided either by the internal bandgap reference or externally.
B9.2 – INT REF generates the bias voltage for external attenuators based on resistive networks.
B20 – ATB collects critical signals from the analog core for external monitoring.

Digital Core blocks:

B6.4 – DIGITAL FILTER filters and decimates the 1-bit output of the ΔΣ modulator to obtain the final resolution.
B6.5 – SAMPLES AVERAGING
B6.6 – OUTPUT DATA BUFFER records the acquired telemetries
B7 – STATUS COMPARATOR compares the acquired telemetries with a registered threshold level.
B10 – V SUPERVISOR is a window comparator (acquired telemetry versus registered threshold levels) implemented digitally.
B11 – RESET MANAGEMENT generates the internal reset signal for TM/TC RHIC.
B12 – REFERENCE REG is a register bank. It records the threshold levels.
B13 – PWM GEN implement the PWM functionality of telecommands.
B14 – STA REG is a register bank. It stores the status of TM/TC RHIC.
B15 – ADC REG is a register bank. It stores the configurations for the digital conversions of the telemetries.
B16 – ADC TIMING CONTROLLER manages the timing configurations of the digital conversions of the telemetries.
B17 – MISC REG is a register bank. It stores additional registers not considered in the other register banks.
B18 – SPI/SSB implements the communication interfaces.
B19 – COMMAND drives the telecommands using the information stored in other blocks.
B22 – DTB is the digital test bus.

Architecture Analysis – Reused IPs (1/8)

Analogue Core blocks:

B1 – LDO ANA generates the 1.8V analogue core supply from the 3.3V external supply.
B3 – LDO DIG generates the 1.8V digital core supply from the 3.3V external supply.
B4 – SENSOR BIASING provides the bias capability of the telemetry channels.
B6.1 – MUX selects the telemetry channels to be acquired.
B6.2 – SIGNAL CONDITIONNING fits the signal coming from the telemetry channels for the ΔΣ modulator input.
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Colour code:
Reused IP
Based on available IP
Created from scratch

Digital Core blocks:

B6.4 – DIGITAL FILTER filters and decimates the 1-bit output of the ΔΣ modulator to obtain the final resolution.
B6.5 – SAMPLES AVERAGING
B6.5 – OUTPUT DATA BUFFER records the acquired telemetries
B7 – STATUS COMPARATOR compares the acquired telemetries with a registered threshold level.
B10 – V SUPERVISOR is a window comparator (acquired telemetry versus registered threshold levels) implemented digitally.
B11 – RESET MANAGEMENT generates the internal reset signal for TM/TC RHIC.
B12 – REFERENCE REG is a register bank. It records the threshold levels.
B13 – PWM GEN implement the PWM functionality of telecommands.
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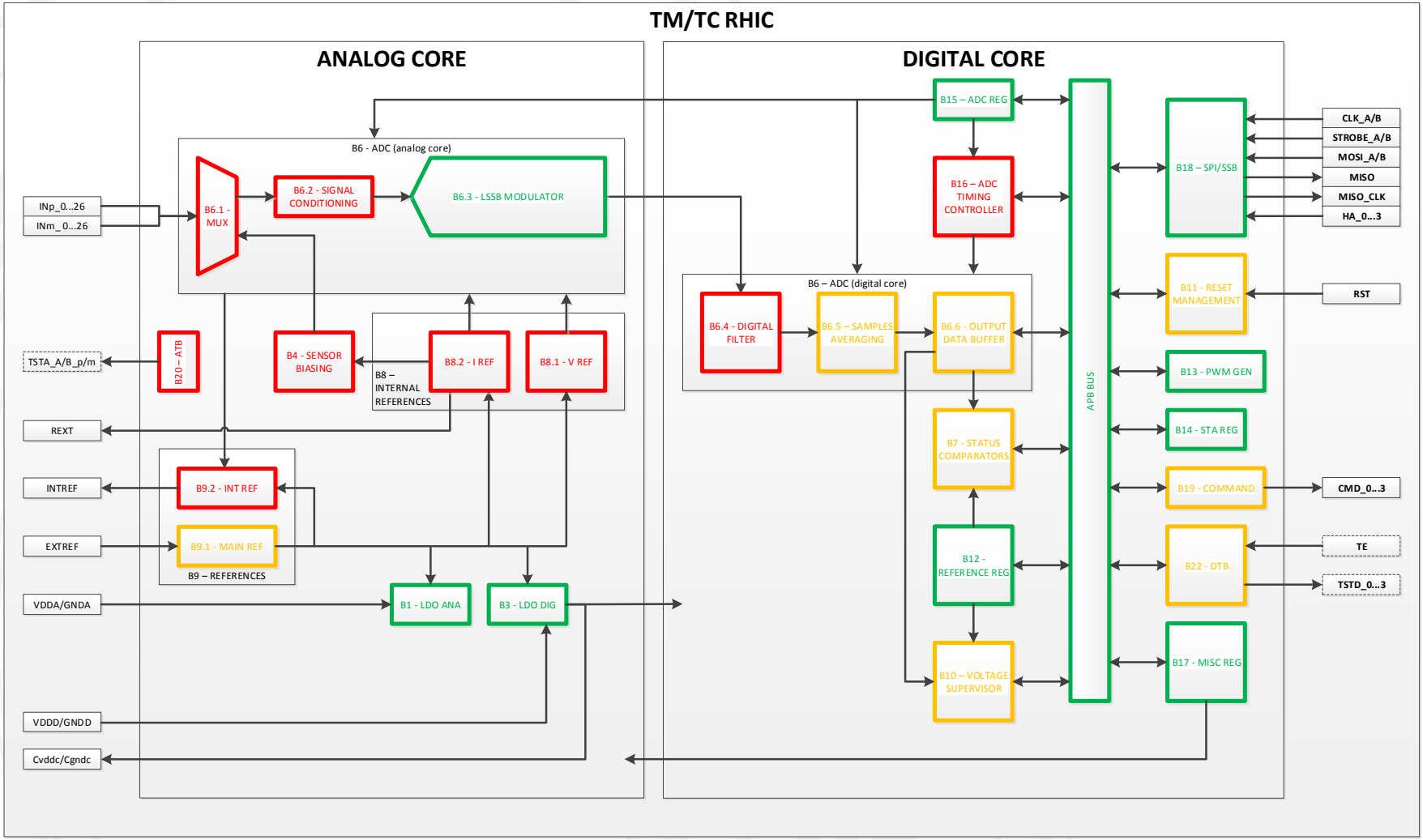
B19 – COMMAND drives the telecommands using the information stored in other blocks.
B22 – DTB is the digital test bus.

Architecture Analysis – Reused IPs (2/8)



Architecture Analysis – Reused IPs (3/8)

Advantages of IP reuse

- Same project scope with reduced development time and cost
- Risk mitigation
- Higher reliability
- Shorter time-to-market

Drawbacks of IP reuse

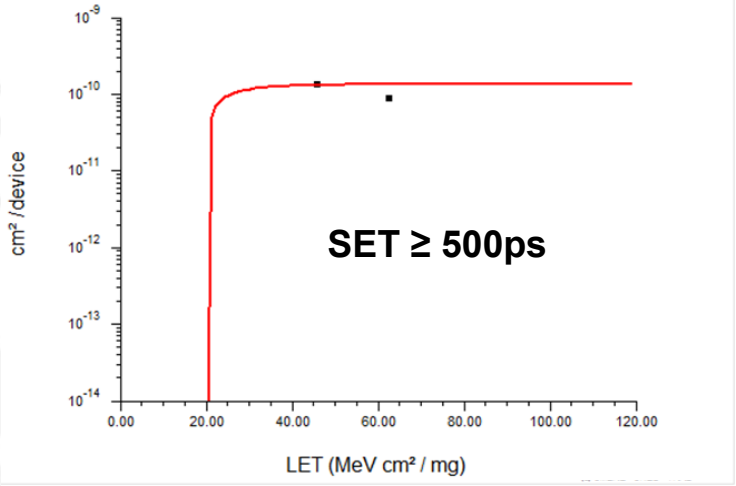
- Additional evaluation costs, if IP is finally discarded.

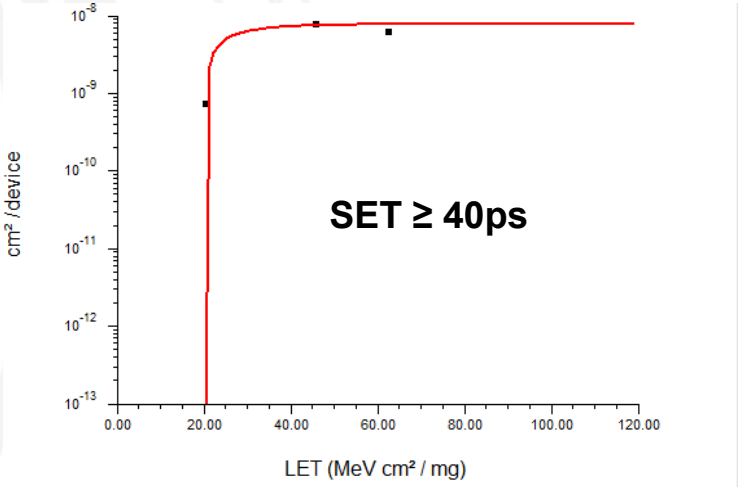
Architecture Analysis – Reused IPs (4/8)

LDO Regulator Type 1

- Designed to supply power to analogue circuitry that require continuous bias (functionality of B1 – LDO ANA).
- Additional checks were performed to verify that its performance is not affected by the operational frequency of the DC/DC converter providing the 3.3V supply at system level.
- It was concluded that it is **reusable for TM/TC RHIC.**

Parameter	Value	Units
Supply voltage	3.3	V
Reference voltage	1.25	V
Regulated output voltage	1.8	V
Maximum output current	60	mA
TID / LDR	505 / 310	krad(Si) / rad(Si)/h
SEL LET_{th}	> 72	MeV·cm²/mg
SET(≥500ps) LET_{th} (Weibull fit)	[20,4 ; 45,8]	MeV·cm²/mg
SET(≥40ps) LET_{th} (Weibull fit)	[10 ; 20,4]	MeV·cm²/mg
SET(≥500ps) XS (Weibull fit)	9.3E-11	cm²/device
SET(≥40ps) XS (Weibull fit)	6,4E-9	cm²/device



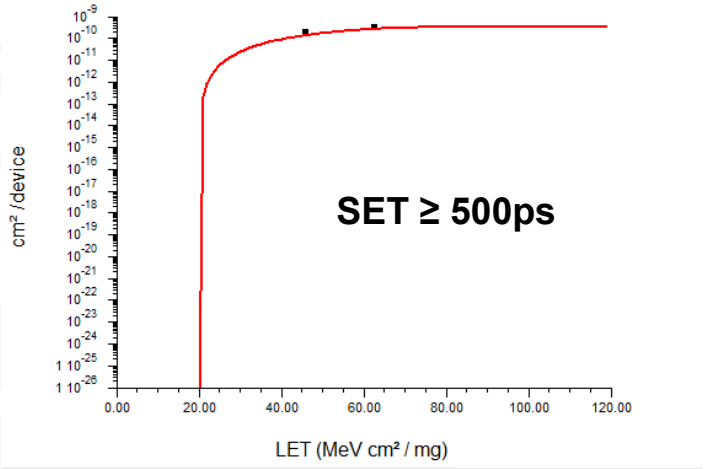


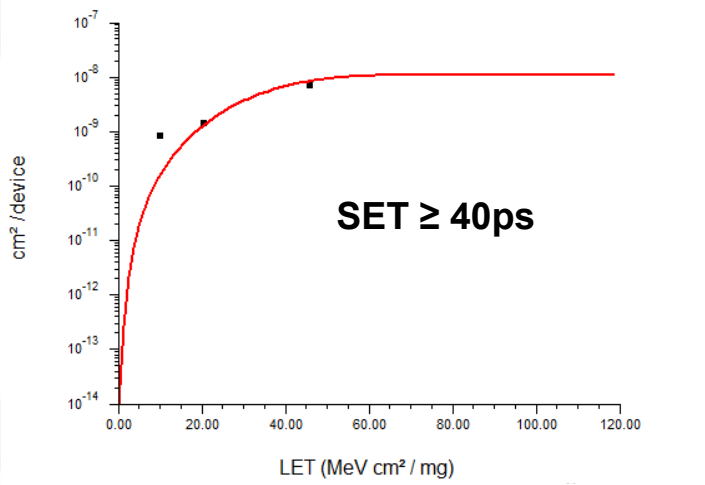
Architecture Analysis – Reused IPs (5/8)

LDO Regulator Type 2

- Designed to supply power to digital circuitries (functionality of B3 – LDO DIG).
- Additional checks were performed to verify that its performance is not affected by the operational frequency of the DC/DC converter providing the 3.3V supply at system level.
- It was concluded that it is **reusable for TM/TC RHIC.**

Parameter	Value	Units
Supply voltage	3.3	V
Reference voltage	1.25	V
Regulated output voltage	1.8	V
Maximum output current	30	mA
TID / LDR	505 / 310	krad(Si) / rad(Si)/h
SEL LET_{th}	> 72	MeV·cm²/mg
SET(≥500ps) LET_{th} (Weibull fit)	[20,4 ; 45,8]	MeV·cm²/mg
SET(≥40ps) LET_{th} (Weibull fit)	< 10	MeV·cm²/mg
SET(≥500ps) XS (Weibull fit)	3,95E-10	cm²/device
SET(≥40ps) XS (Weibull fit)	1E-8	cm²/device



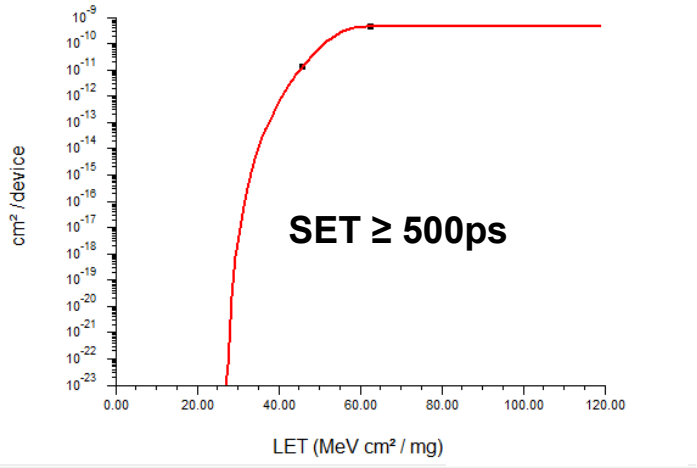


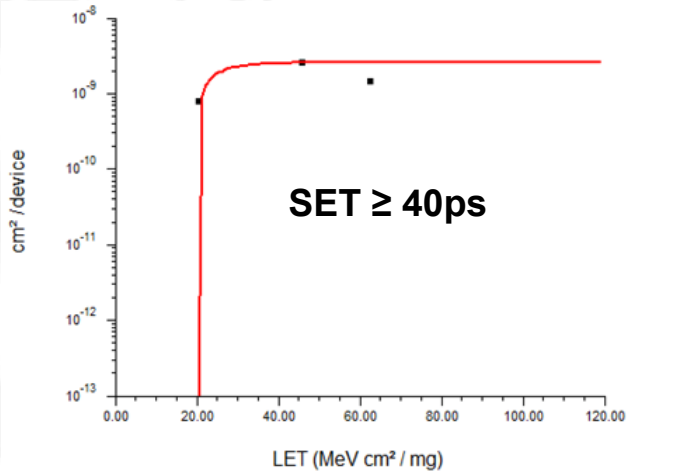
Architecture Analysis – Reused IPs (6/8)

Band-gap Reference

- Designed to provide the voltage reference for LDO regulators types 1 and 2 (part of the functionality of B9.1 – MAIN REF).
- Additional checks were performed to verify that the bandgap reference is accurate enough to meet top level requirements.
- It was concluded that **ΔV(T) enhancements are required to be reused for TM/TC RHIC.**

Parameter	Value	Units
Supply voltage	3.3	V
Reference voltage	1.25	V
Regulated output voltage	1.8	V
Maximum output current	60	mA
TID / LDR	505 / 310	krad(Si) / rad(Si)/h
SEL LET_{th}	> 72	MeV·cm²/mg
SET(≥500ps) LET_{th} (Weibull fit)	[20,4 ; 45,8]	MeV·cm²/mg
SET(≥40ps) LET_{th} (Weibull fit)	[10 ; 20,4]	MeV·cm²/mg
SET(≥500ps) XS (Weibull fit)	4.8E-10	cm²/device
SET(≥40ps) XS (Weibull fit)	1,5E-9	cm²/device





Architecture Analysis – Reused IPs (7/8)

ΔΣ Modulator

- Designed to provide a 16 ENOB 1-bit output data stream inside 50 kHz Nyquist bandwidth with a 13.6 MHz sampling clock. (functionality of B6.3 – LSSB).
- Additional checks were performed to verify that the IP could operate for different sampling frequencies (up to 15 MHz) without degradation below 11 ENOB.
- It was concluded that it is **reusable for TM/TC RHIC.**

Parameter	Value	Units
Supply voltage	1.8	V
ENOB	> 11 (16 nom.)	effective bits
Nyquist Bandwidth	50	kHz
Sampling clock frequency	< 15 (13.6 nom.)	MHz
Current consumption	8	mA
SEL LET_{th}	> 72	$MeV \cdot cm^2/mg$

Architecture Analysis – Reused IPs (8/8)

Digital IPs

- Almost all the digital core of TM/TC RHIC is composed by digital IPs already implemented in FPGA.
- The [10; 20] MHz system clock frequency should not entail complications for the implementation of these IPs with DARE180U libraries.
- Radiation performances are bound to DARE180U libraries'.

Conclusions

- This work presents a telemetry and telecommand rad-hard chip that aims to be a recurrent part inside the Airbus group.
- Its usage will entail weight, volume and price reduction of RIU/RTU and ICU satellite subsystems. Regarding price, the target reduction for each of the three products is between 10 and 15%.
- To mitigate risks and reduce time development, the following analogue and AMS IPs based in the same technology (UMC L180) were selected to compose the chip: two type of regulators, a bandgap reference and a ΔΣ modulator. The suitability of each IP was evaluated with additional checks.

Thank you for your attention!

Any questions?

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