A rad-hard system-on-chips solution for closed-loop motion control

Presented by Dr. Ying Cao

On behalf of MAGICS Instruments,
Fusion for Energy,
and Veolia Nuclear solutions

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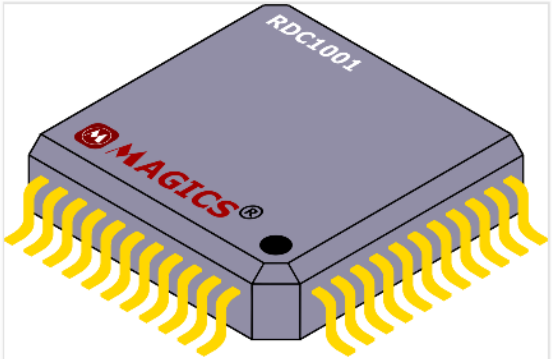
Rad-hard CLMC for ITER remote handling

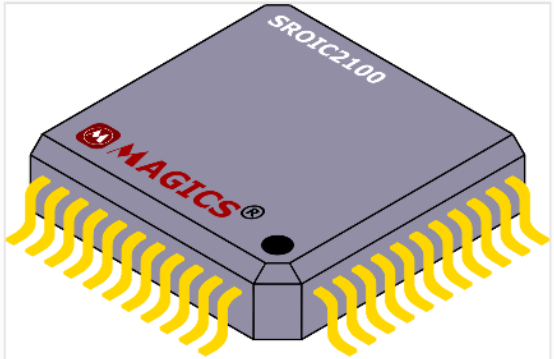
- Project background:
  - Contracted by Fusion for Energy, for ITER remote handling
    The goal of ITER is to build an artificial sun on the earth, to provide safe, non-carbon emitting and virtually limitless energy for our planet.
  - Design and manufacture of rad-hard ASICs for position sensing, motion control, and bus communication
- Solution:

  The solution consists of five rad-hard system-on-chips:
  - A resolver/LVDT to digital converter to read out angle information from a resolver or linear distortion information from a LVDT
  - A resistive bridge sensor signal conditioning ASIC to read out sensors such as RTD, thermocouple, and strain gauge
  - A 24V 10-channel limit switch conditioning ASIC to read the status of limit switches connected to it
  - A 24V 10-channel relay driver ASIC to drive high-side solid-state or mechanical relays
  - A bus communication ASIC to implement the BiSS interface protocol, the SPI master protocol, and the RS485 bus transceiver

Featured rad-hard ASICs



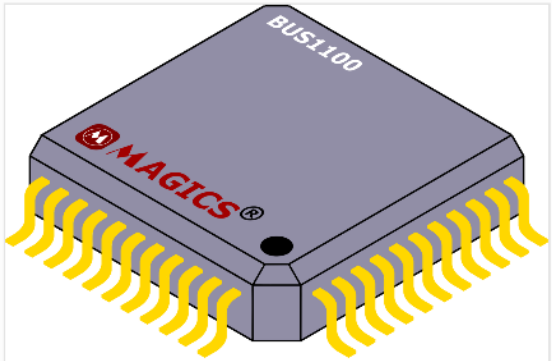
RDC1001
Resolver/LVDT-to-digital converter



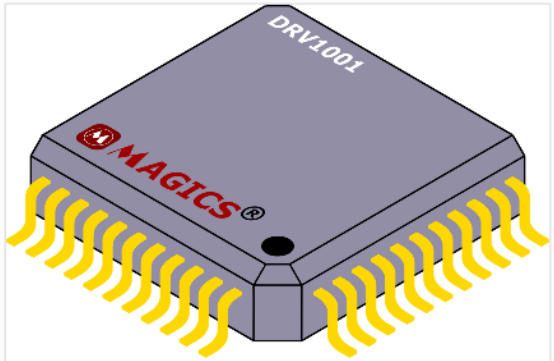
SROIC2100
Resistive bridge sensor signal conditioner

Potential space applications:

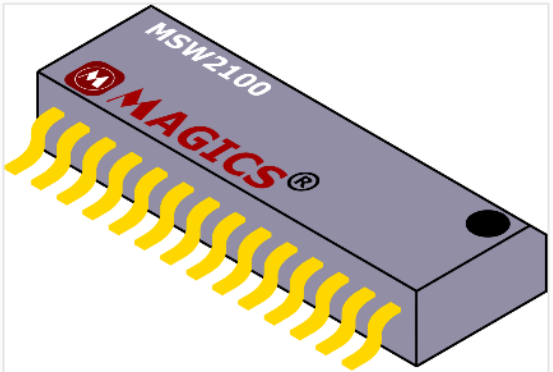
- Control of remote handling manipulators, and remote operated vehicles;
- Speed control of reaction wheels;
- Control of electrical propulsion systems;
- Altitude control;
- Control of electrical valves.



BUS1100
BiSS interface (RS-485) communication ASIC



DRV1001
Rad-hard 10-channel relay driver



MSW2100
10-channel limit switch sensing ASIC

How does MAGICS develop rad-hard ASICs

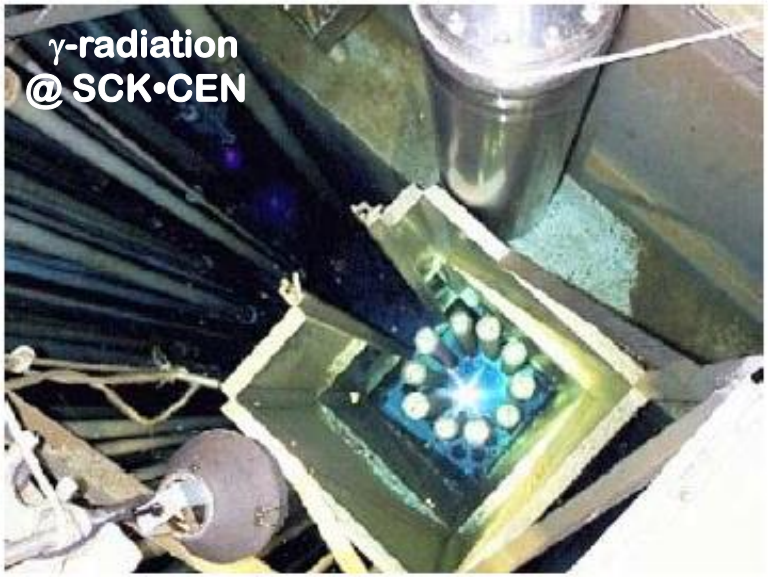
Radiation hardening design flow

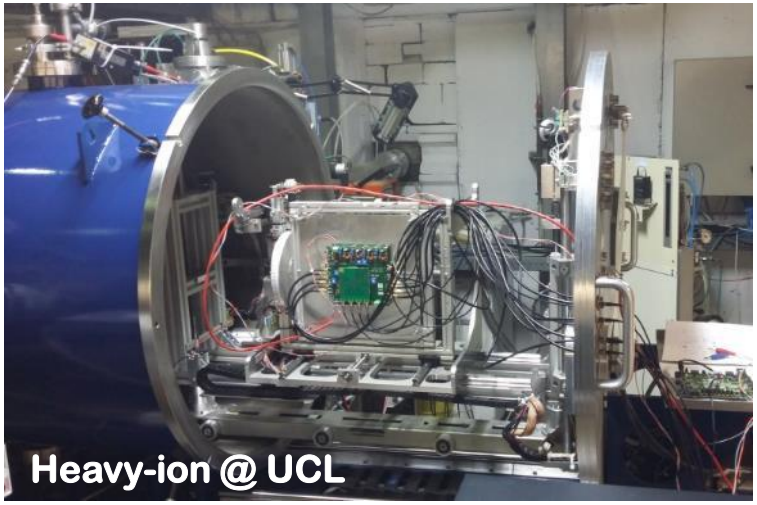
Rad-hard IC design flow

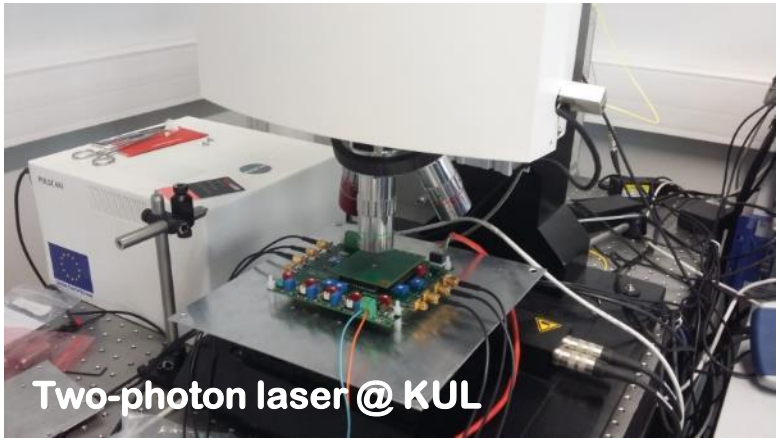
- MAGICS has developed a unique rad-hard IC design environment to achieve high first-time-right rate and high reliability:
  - Gain insights into radiation effects on ICs through extensive radiation assessments
  - Industrial standard EDA tools: MATLAB for system behavioral model simulation; Cadence Virtuoso design tools for schematic edit, simulation and layout; Cadence Incisive and Innovus for digital design and implementation; Mentor Graphics Calibre for physical verification and sign-off.
  - Experimentally verified transistor radiation model for TID (total-ionizing-dose) simulation.
  - In-house proprietary TMR (triple modular redundancy) generator and SET simulator for single-event simulation.
  - A wide range of qualified rad-hard analog/mixed-signal IP blocks (e.g., PGA, ADC, PLL, Clock reference, Bandgap, LDO, Temperature sensor, etc.).

Radiation assessment

MAGICS has easy access to different kinds of irradiation facilities, e.g., x-ray, two-photon laser, gamma ray, heavy ion, proton. (follow ESCC 22900 and ESCC 25100 standards)







MAGICS' close-loop control system-on-chips solution

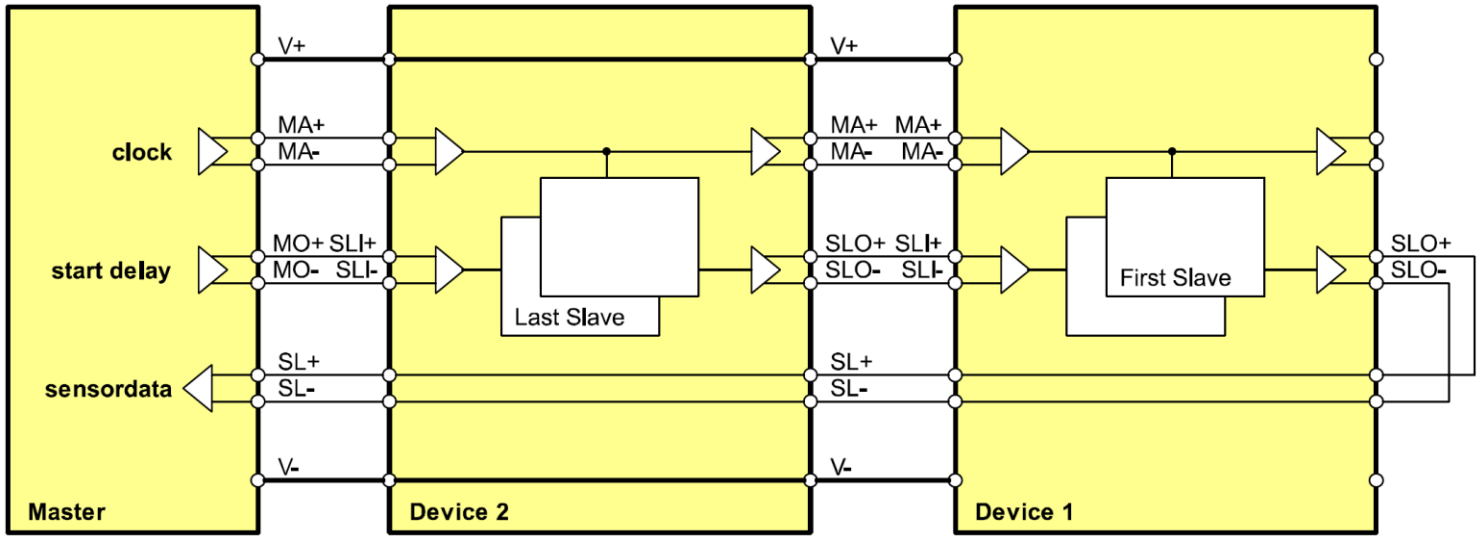
Rad-hard CLMC ASICs

BiSS-Interface

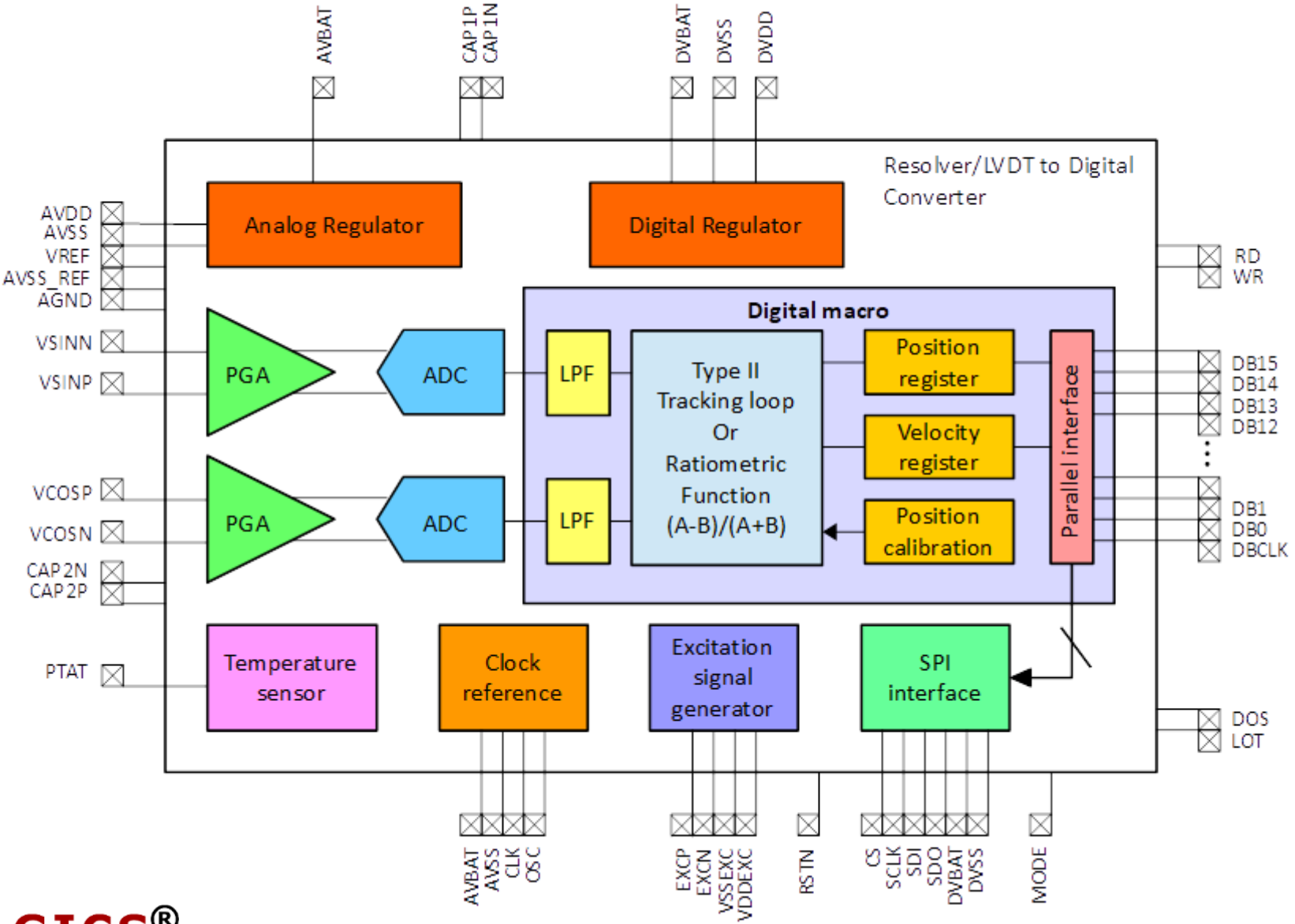
BiSS-interface is an open-source, real-time fieldbus protocol. It enables a digital, serial and secure communication between controller, sensor and actuator.

- It is designed in both point-to-point and continuous mode.
- It is designed for industrial applications which require transfer rates, safety, flexibility and minimized implementation effort.
- It can reach a speed of 10 Mbps over a cable length of 100 meters.

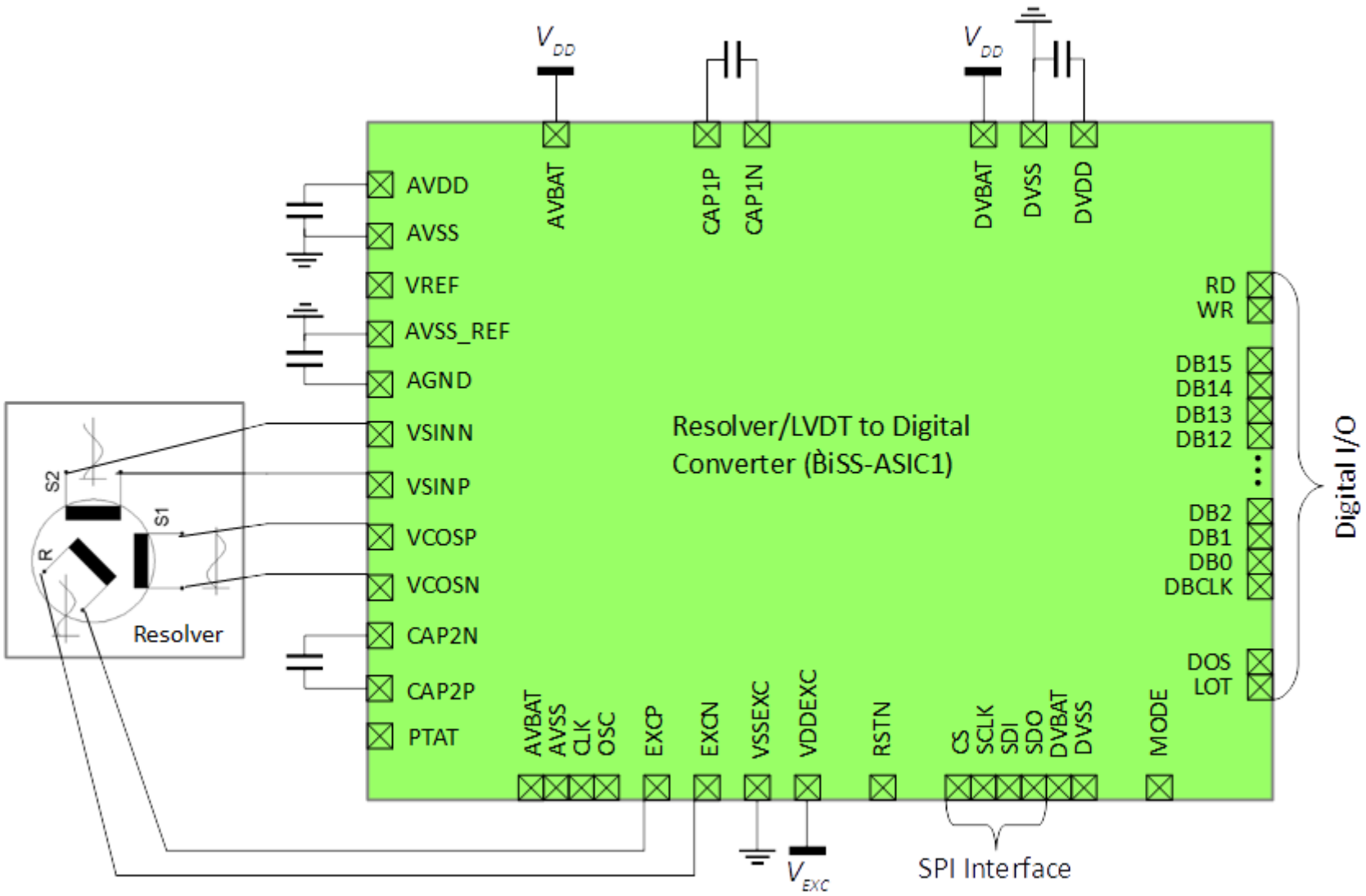
Example BiSS-Interface configuration with multiple slaves



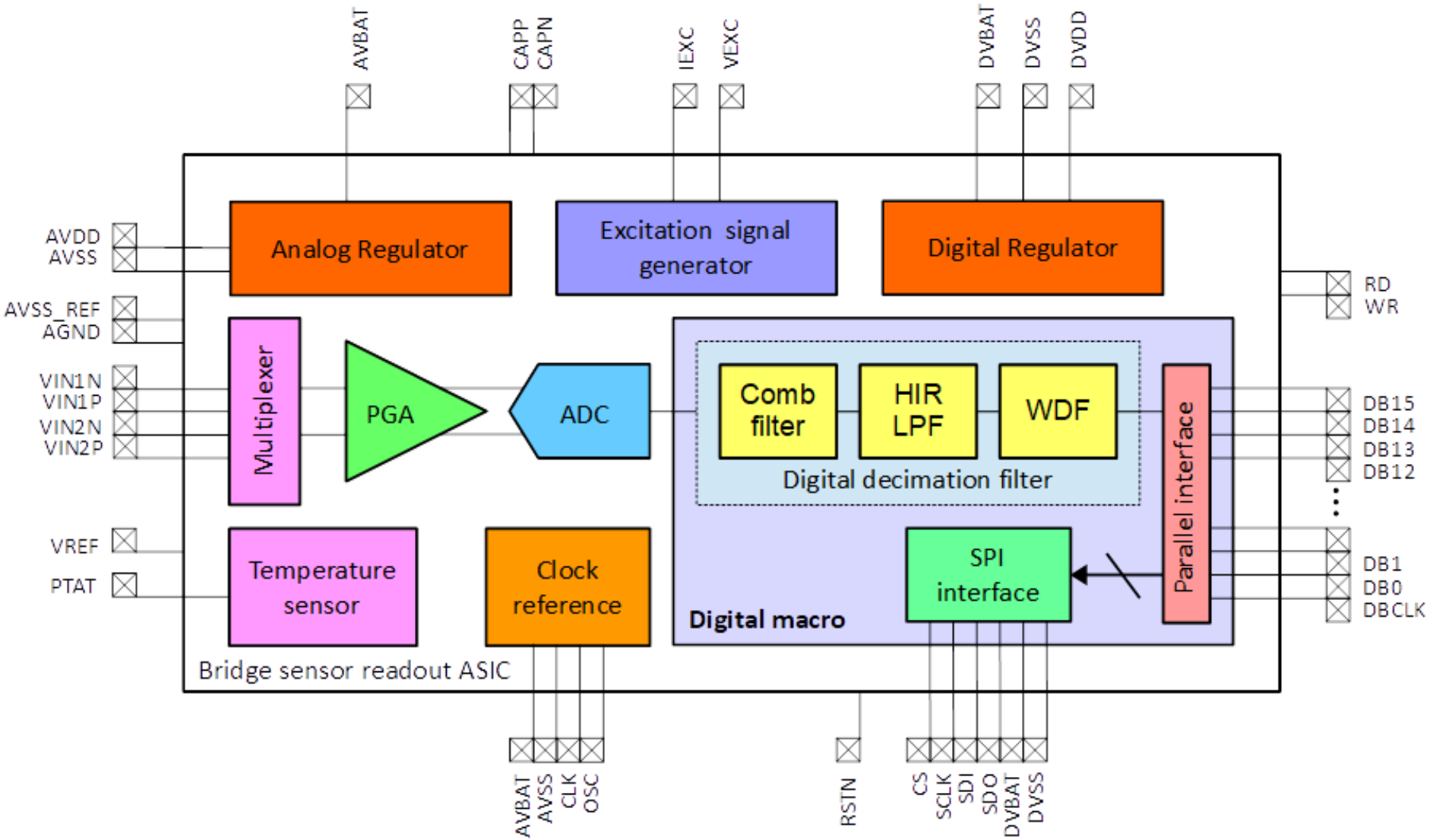
BiSS-ASIC1 (block diagram)



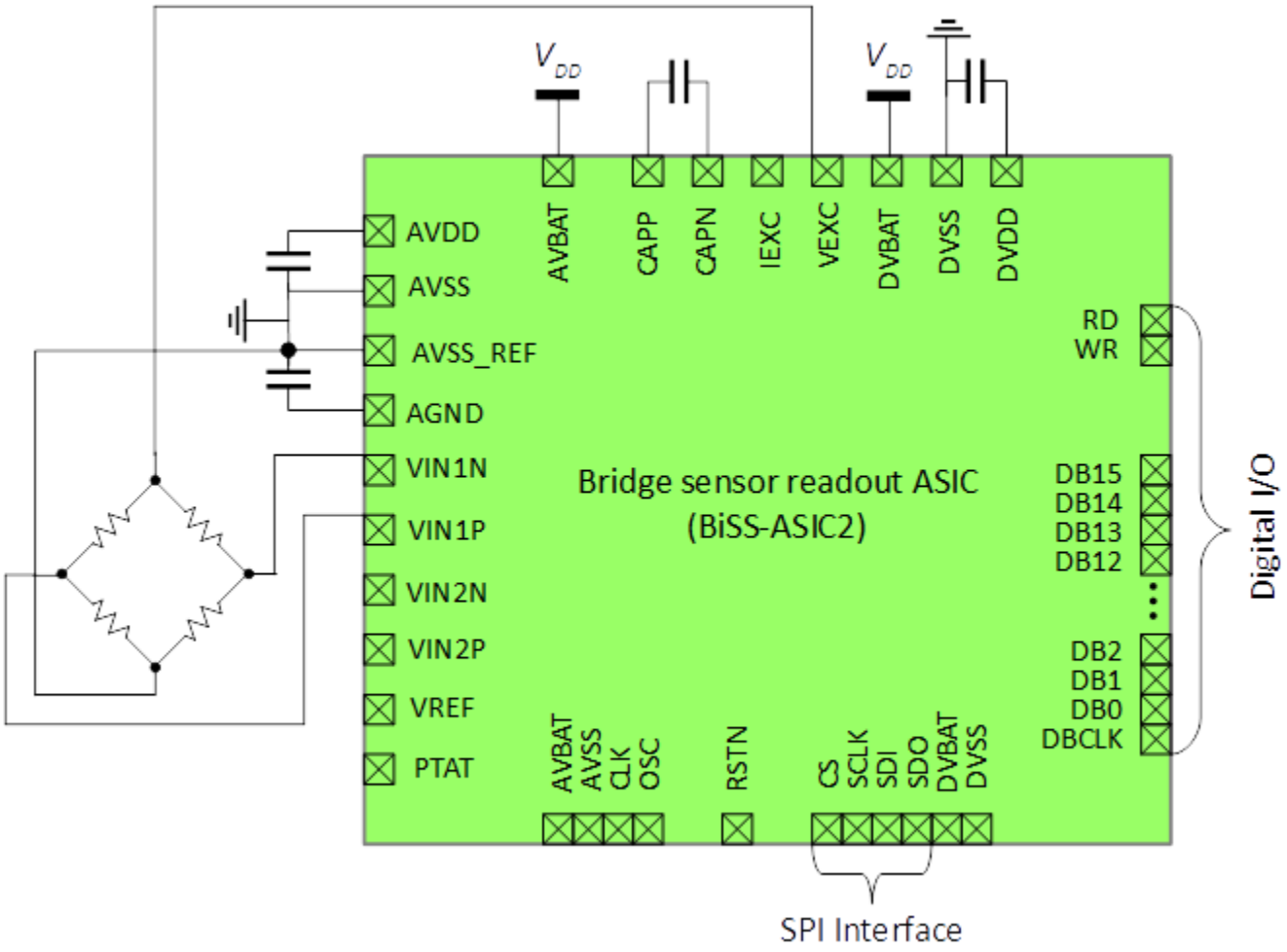
BiSS-ASIC1 (system integration)



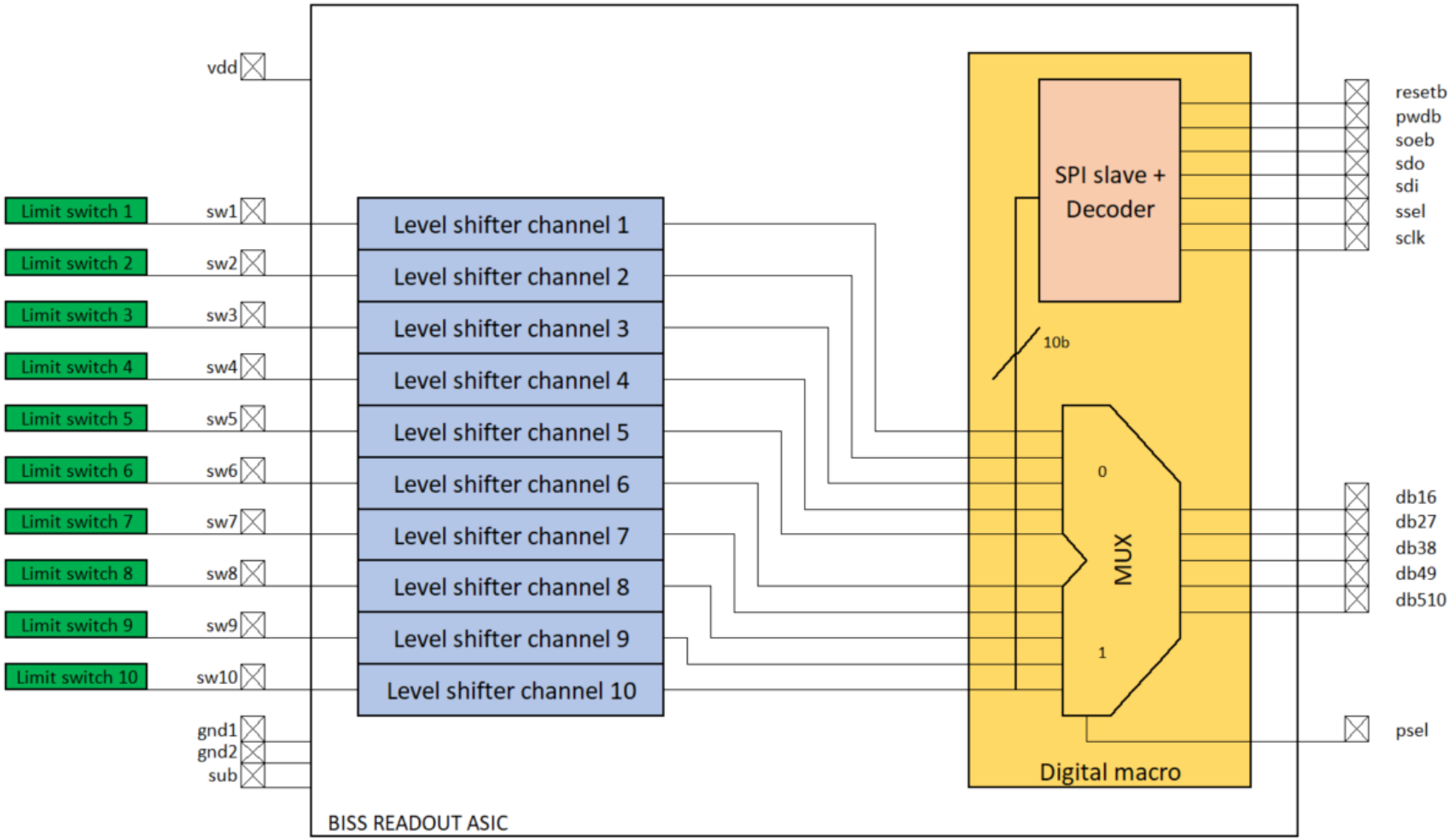
BiSS-ASIC2 (block diagram)



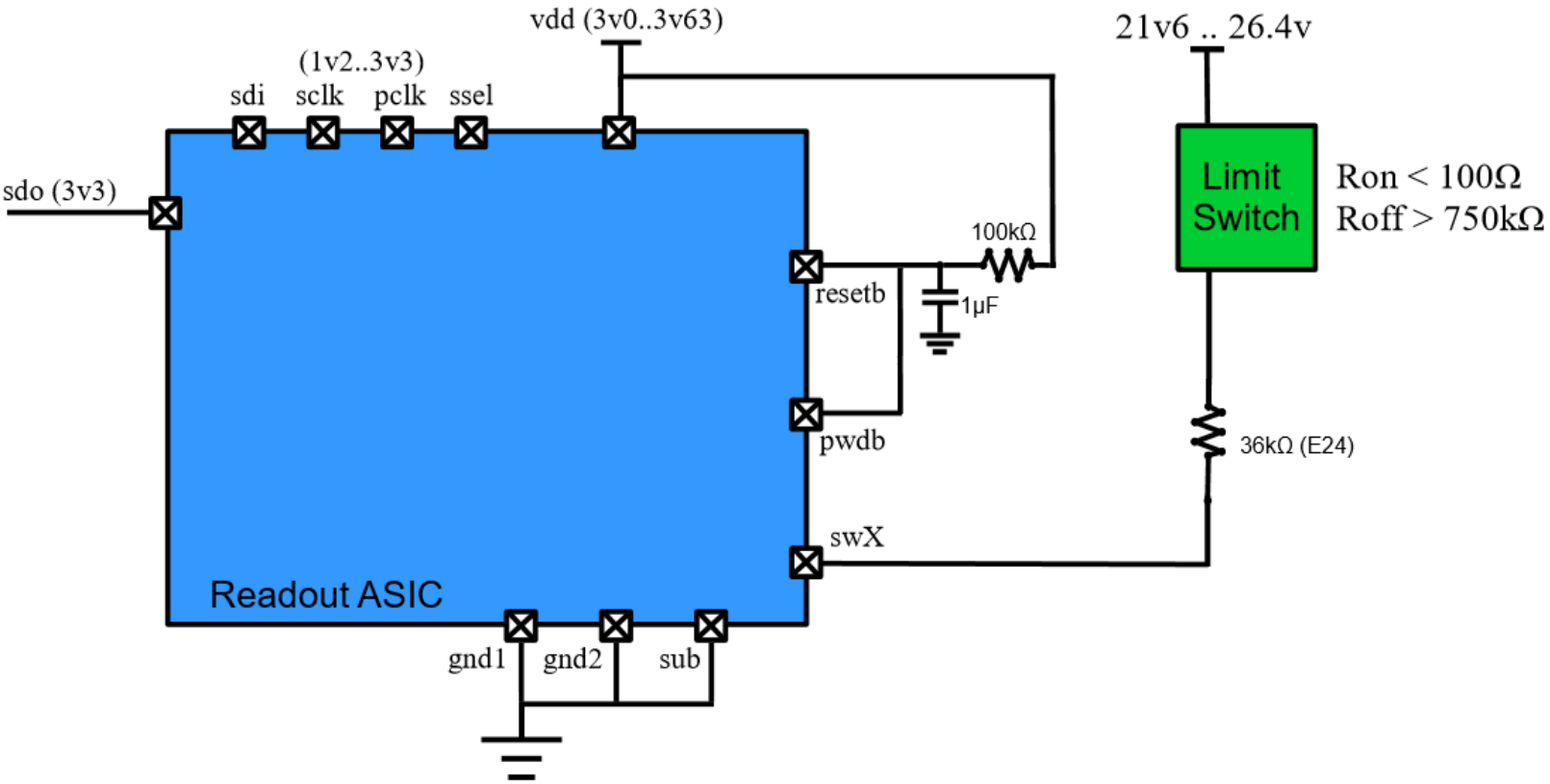
BiSS-ASIC2 (system integration)



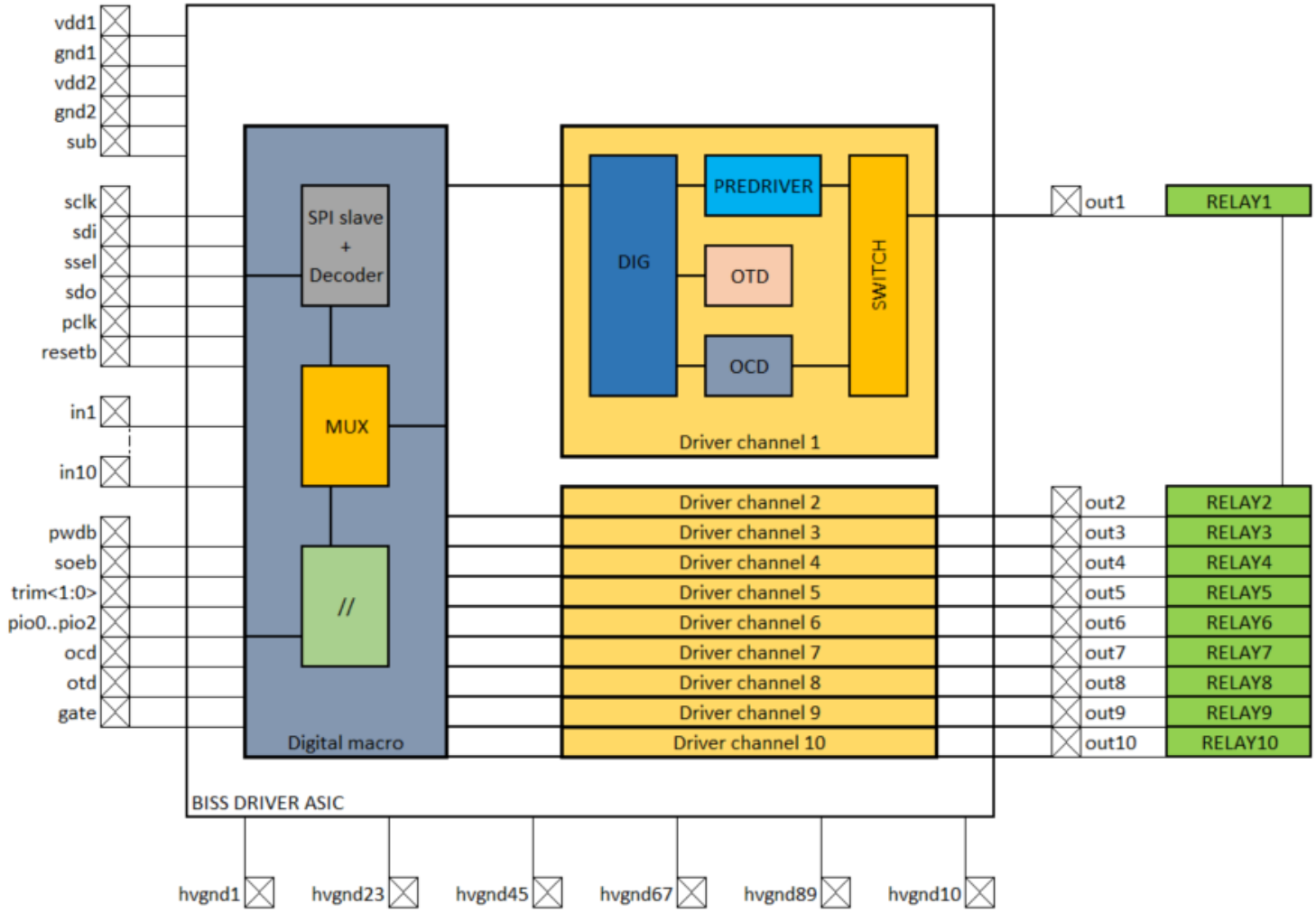
BiSS-ASIC3 (block diagram)



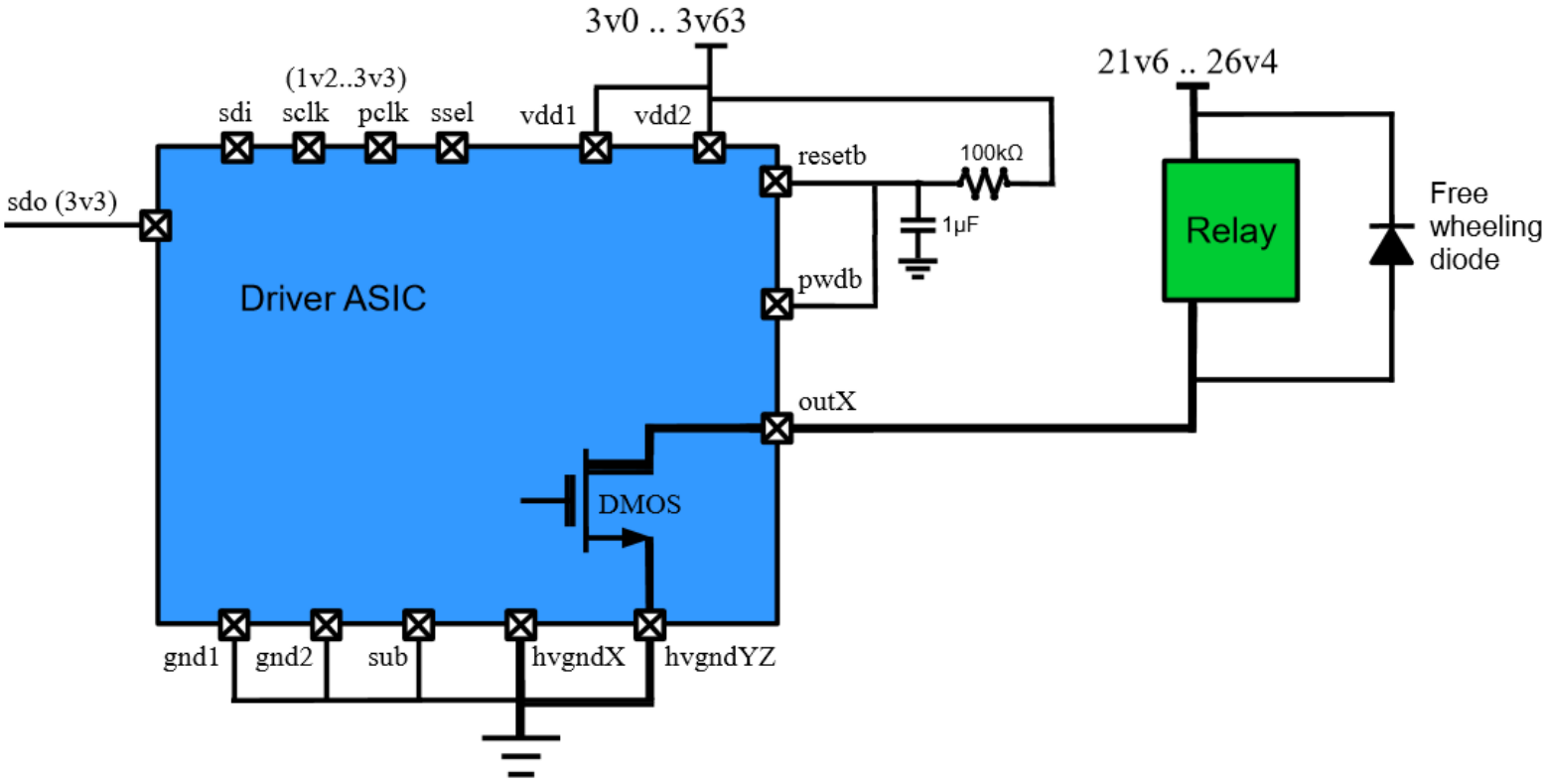
BiSS-ASIC3 (system integration)



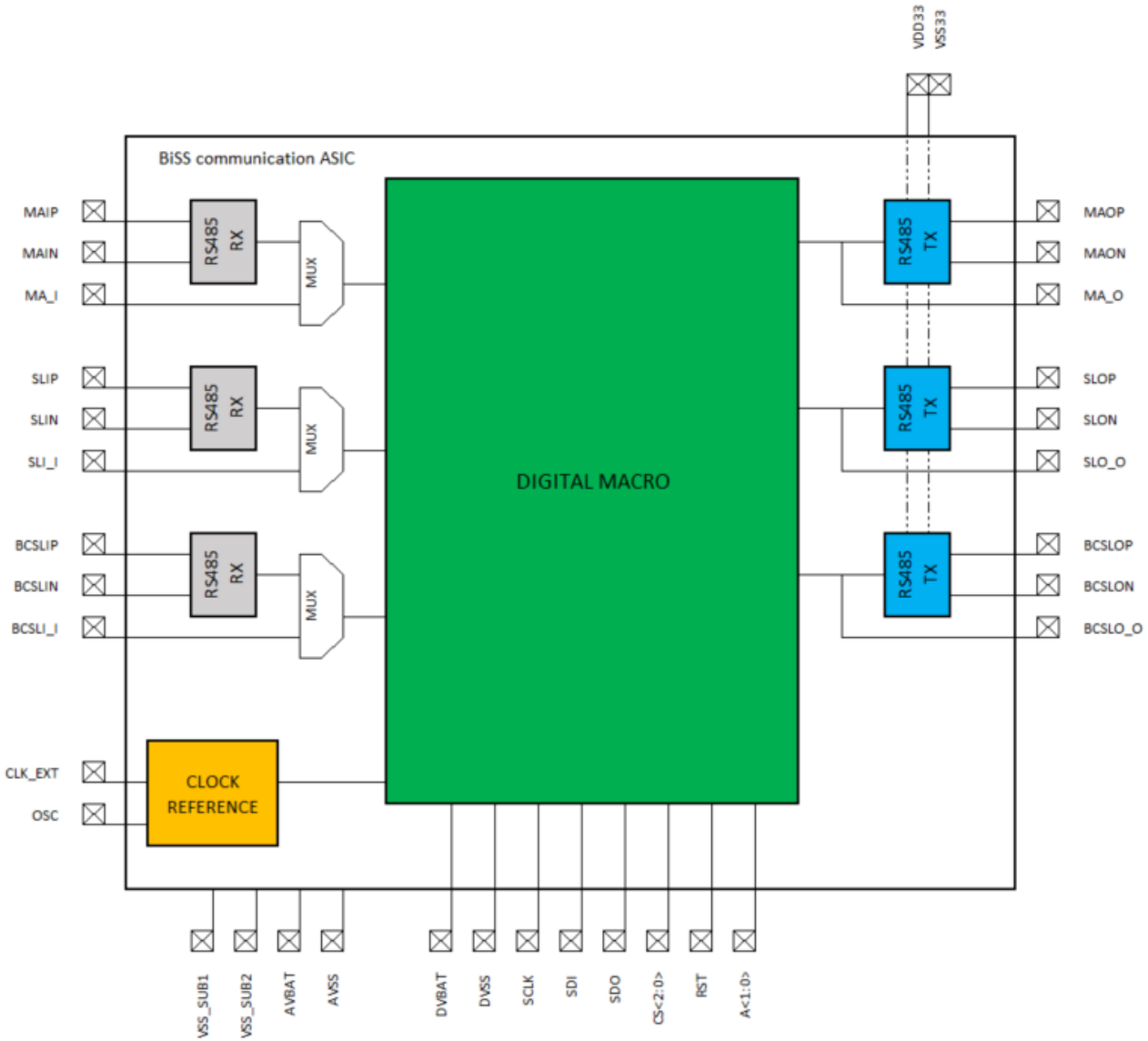
BiSS-ASIC4 (block diagram)



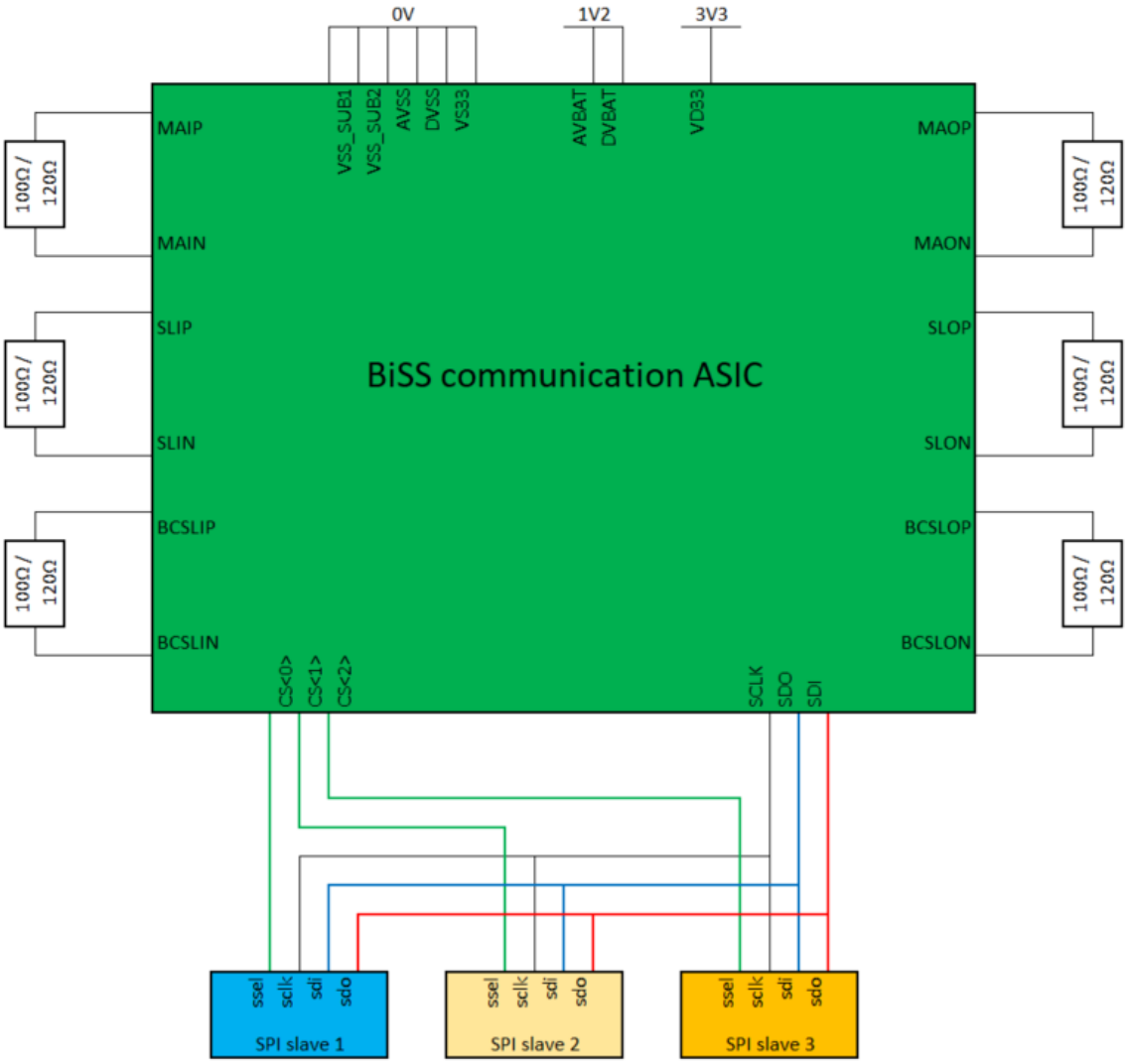
BiSS-ASIC4 (system integration)



BiSS-ASIC5 (block diagram)



BiSS-ASIC5 (system integration)

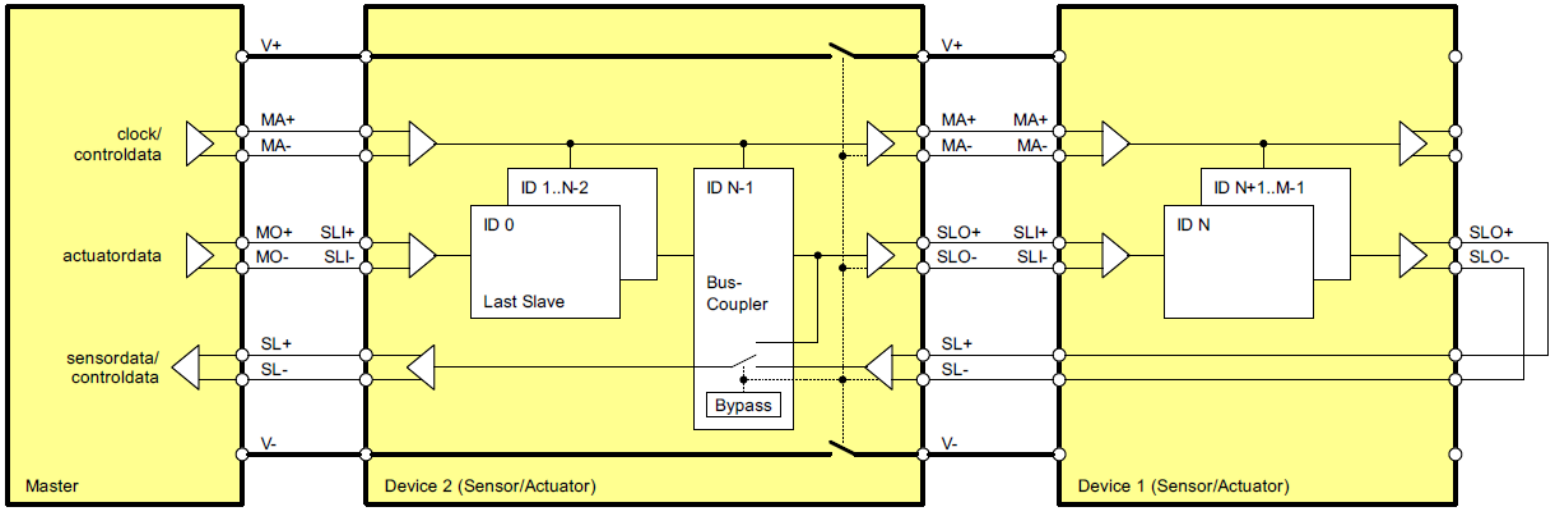


BiSS physical layer configuration

- Depending on the chosen bus topology, the BiSS system can be configured into 4 modes:

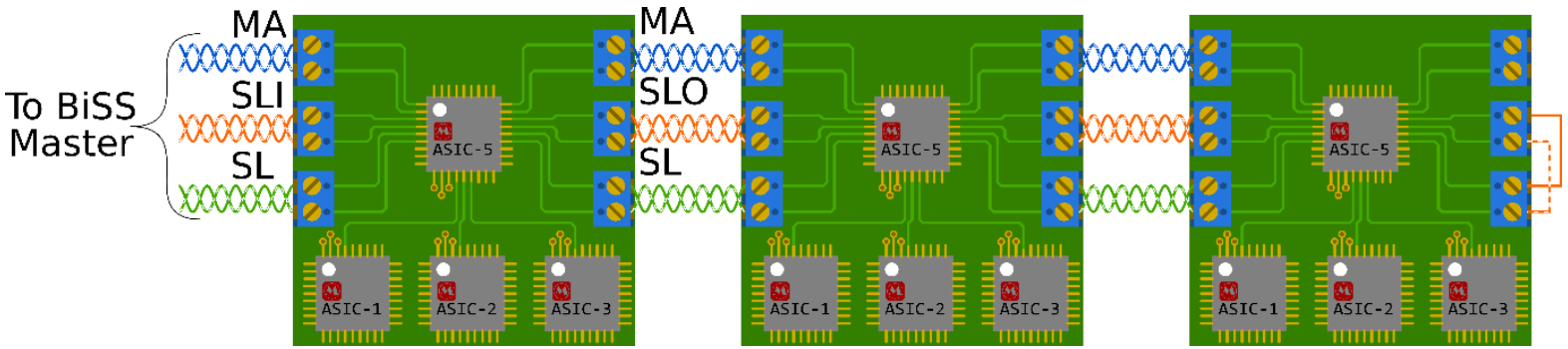
	Configuration input		MA and SLI RS-485 receiver	MA_o and SLO_o RS-485 driver
Comment	A[1]	A[0]		
RS-485FULL	0	0	Enabled	Enabled
RS-485RX	0	1	Enabled	Disabled
RS-485TX	1	0	Disabled	Enabled
PAD	1	1	Disabled	Disabled

- A bus coupler is also implemented on the BiSS-ASIC5 to allow fault-tolerant bus system design.

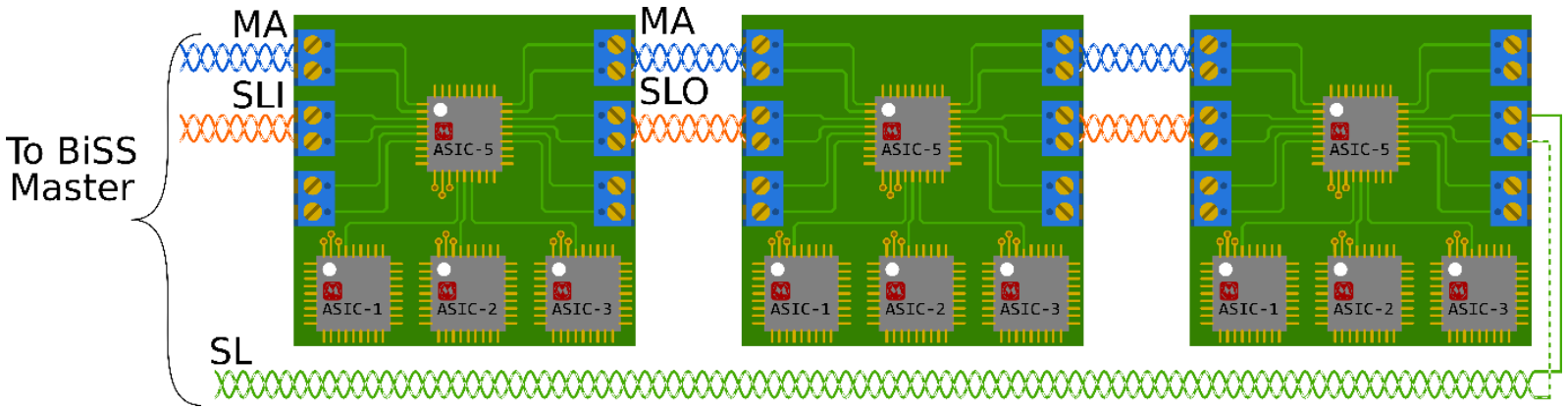


Full RS-485 mode

Default configuration of the BiSS-interface with bus coupling feature:

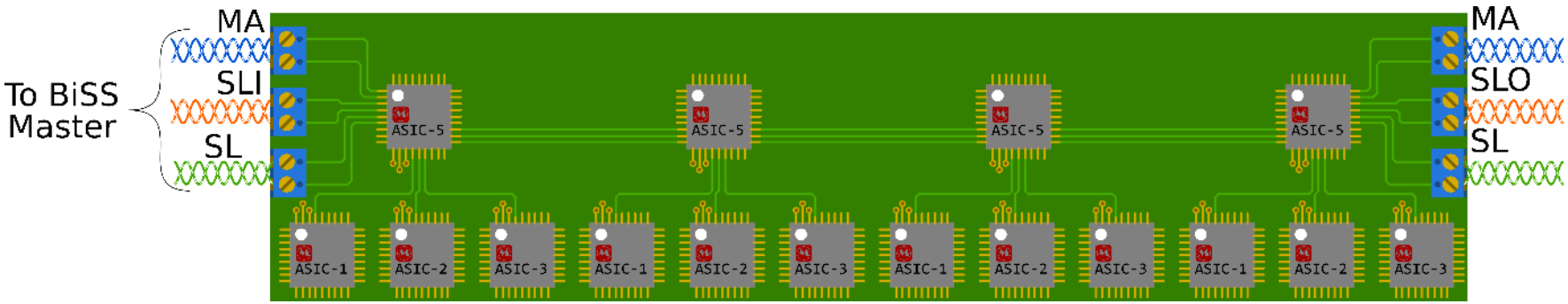


Full RS-485 mode without bus coupling feature:

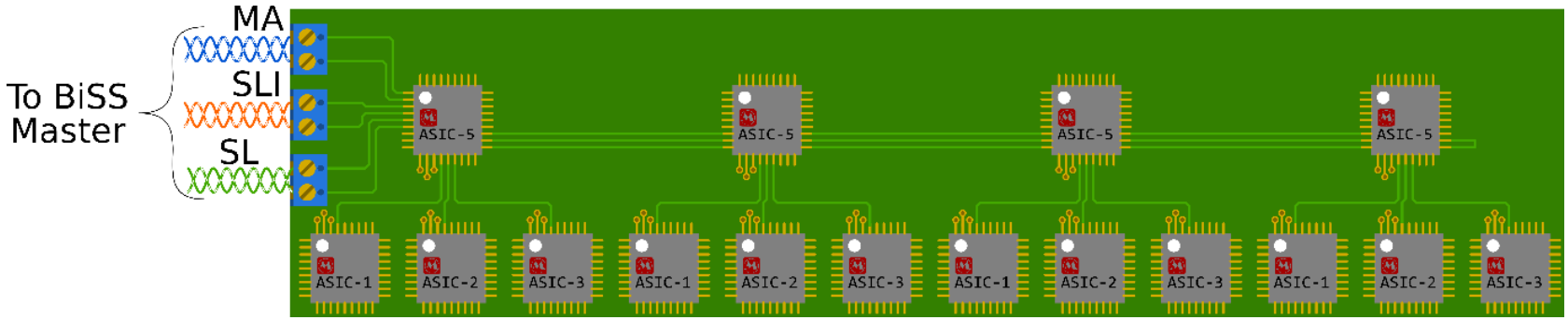


Mixed RS-485 mode

Mixed-mode operation on a single PCB (middle slave-nodes):



Mixed-mode operation on a single PCB (the last slave-node):



General-purpose silicon-proven rad-hard IPs used in the development of BiSS ASICs

65nm CMOS rad-hard analog/mixed-signal IPs

MAGICS®

65nm CMOS rad-hard IPs

Programmable Gain Amplifier	Phase-Locked Loop	Analog-to-Digital Converter
Gain: 1 ~ 256 Gain error: ±0.5% Gain drift: 10 ppm/°C Offset: 5 µV Offset drift: <10 nV/°C Input noise: 20 nV/√Hz TID tolerance: >100 Mrad SEE tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Frequency: 2.2 ~ 3.2 GHz Bandwidth: 0.7 ~ 2 MHz RMS jitter: 350 fs Power: 12 mW TID tolerance: >100 Mrad SEE tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (silicon proven)	Resolution: 16 bits Bandwidth: 20 kHz SNDR: 96 dBFS Power: 5 mW TID tolerance: >100 Mrad SEE tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)
Voltage reference	**Clock reference**	**Temperature sensor**
Temperature range: -50 ~ 125 °C Temperature coefficient: 30 µV/°C Power: 80 µW TID tolerance: >100 Mrad SEE tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Frequency: 8 ~ 12 MHz Temperature coefficient: 30 ppm/°C RMS jitter: 25 ps Power: 360 µW TID tolerance: >100 Mrad SEE tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Temperature range: -50 ~ 125 °C Temperature coefficient: 1.5 mV/°C Accuracy: <1 °C Power: 60 µW TID tolerance: >100 Mrad SEE tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)

65nm CMOS rad-hard library (tbc…)

- The library is still growing. New elements will be added to the library (e.g., regulator, SAR ADC, SERDES, LVDS, DAC, Bus transceiver, XO).
- Digital cores are also available upon request (e.g., SPI, Bus controller, filter, etc.).
- The library can be ported into another process, if a customer requires.

Contact us

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Rad-Hard ASIC development

Smart Nuclear and Space robotics

Intelligent Sensors for harsh environments