Validation of a High Resolution ADC for Space Applications

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Outline

- Target specifications overview
- Design overview
- Electrical validation results
- TID test results
- SEE test results
- Performance summary
- Conclusions

Target specs

Innovations:

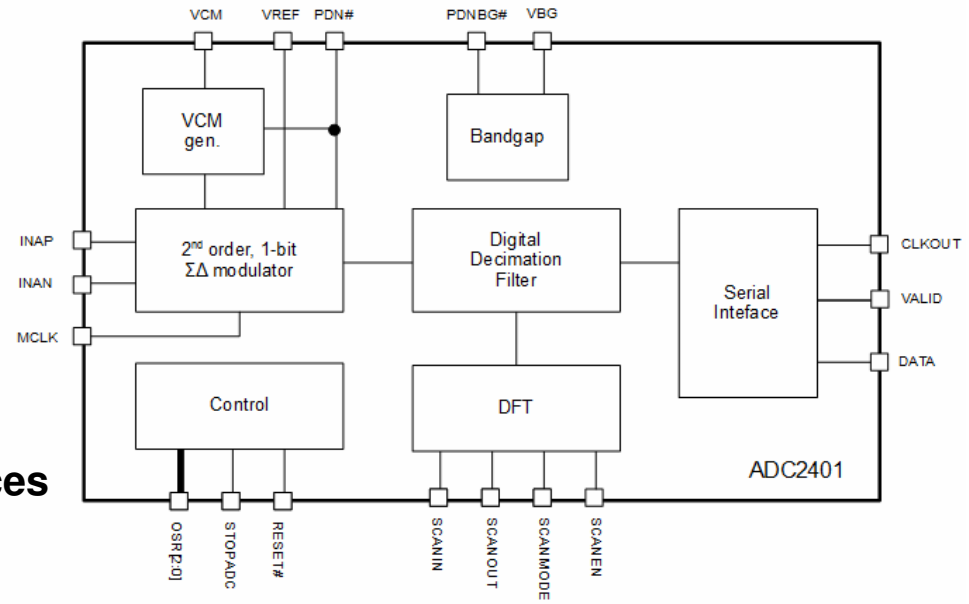
- ✓ **Rad-hard**
- ✓ **High resolution**
- ✓ **Very low sampling rate**

Resolution	24 bit
Analog input bandwidth	DC-10kHz
Effective resolution	16+bits
Dynamic Range	> 100dB
SNR	> 100dB
Sampling rate	≥ 5 kHz
Monotonicity	Full code range
Power dissipation	< 70 mW
LET for SEL immunity	≥ 70 MeV/mg/cm^{-2}
SEU immunity	Protection of critical memory cells
SET immunity	Protection of the digital part
TID tolerance	≥100 krad
Temperature range	-55 °C < T < 125 °C

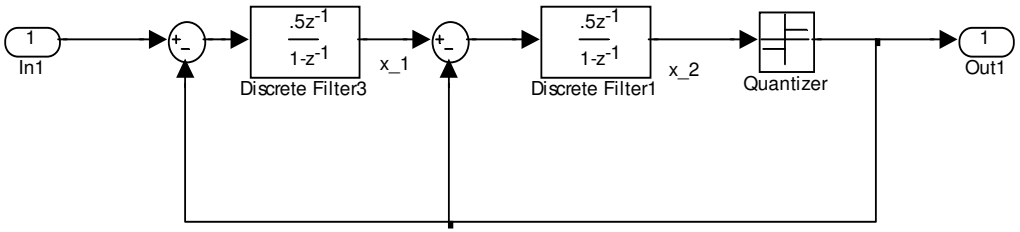
Architecture and features

- Single-bit (inherently linear) ΣΔ modulator
- Single clock domain
- Very low sampling frequency operation
- Correlated double sampling input stage
- Differential or single-ended voltage drive
- ΣΔ modulator can be combined with external DSP core
- Simple serial output interface
- Selectable over-sampling ratios (OSR) allow sampling rates up to **265kSPS**
- Analog bandwidth from **DC to 45kHz**
- 1.8V/3.3Vpower supplies (3.3V I/O)
- Embedded or external voltage reference
- Radiation hardened against SEE and TID

- **Technology**:
  Atmel ATMX150RHA 0.15µm CMOS on SOI
  - **5 metals, 1 poly**
  - **Fully SPICE modeled and characterized devices**
  - **Rad-hard proven logic**
  - **DTI option, annular devices, HV…**

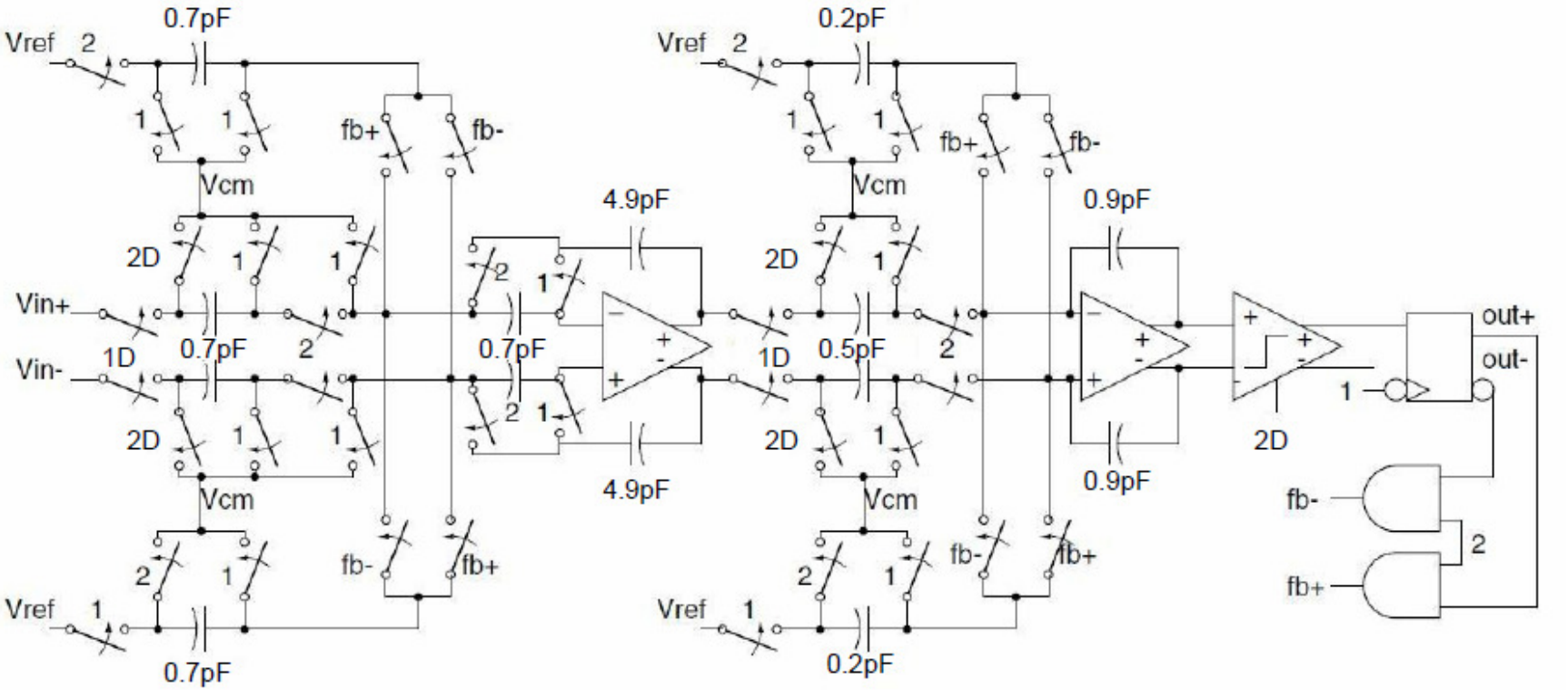


ΣΔ modulator



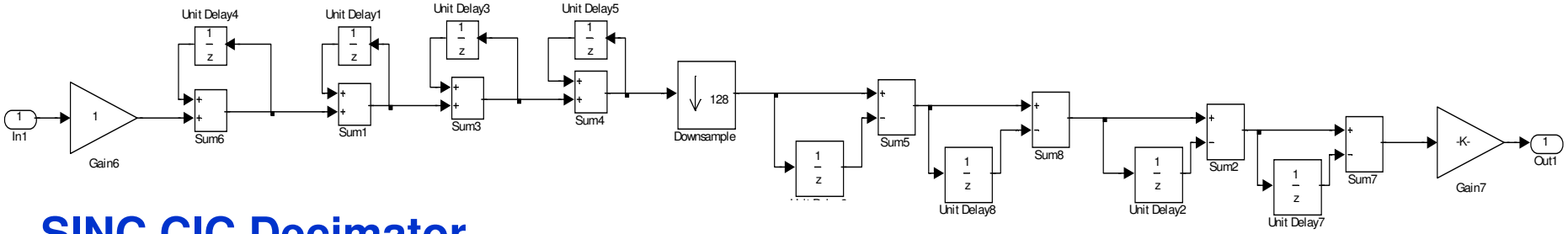
- 1-bit quantizer
- Two fully differential OTAs
- Pass gates as analog switches
- Single-ended Vref input
- 1-bit feedback DAC

Model introduced by *[Norsworthy S.R., R. Schreier, G.C. Temes, 1997]*



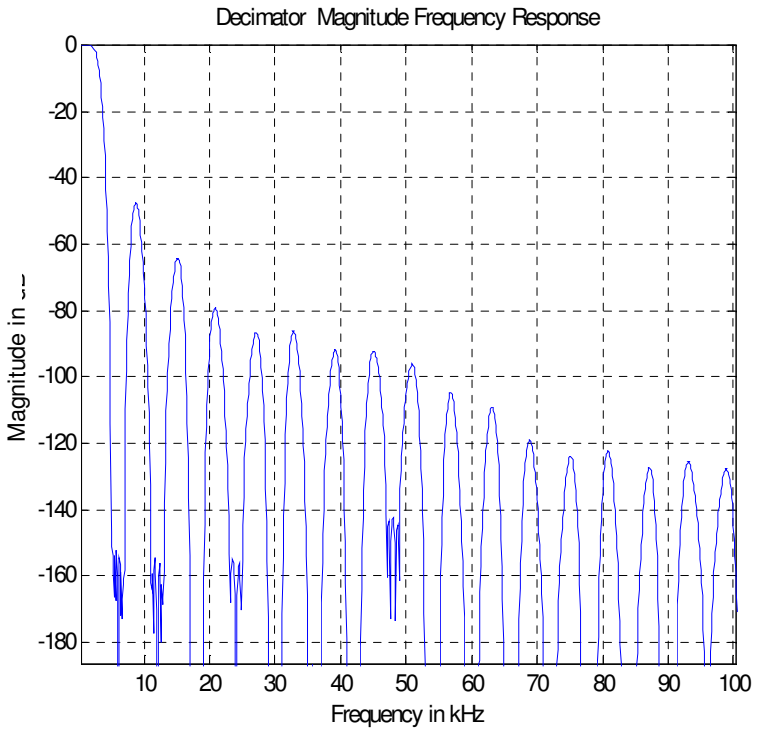
architecture based on *[Nieminen T. and Halonen K, NORCHIP 2010]*

Digital part



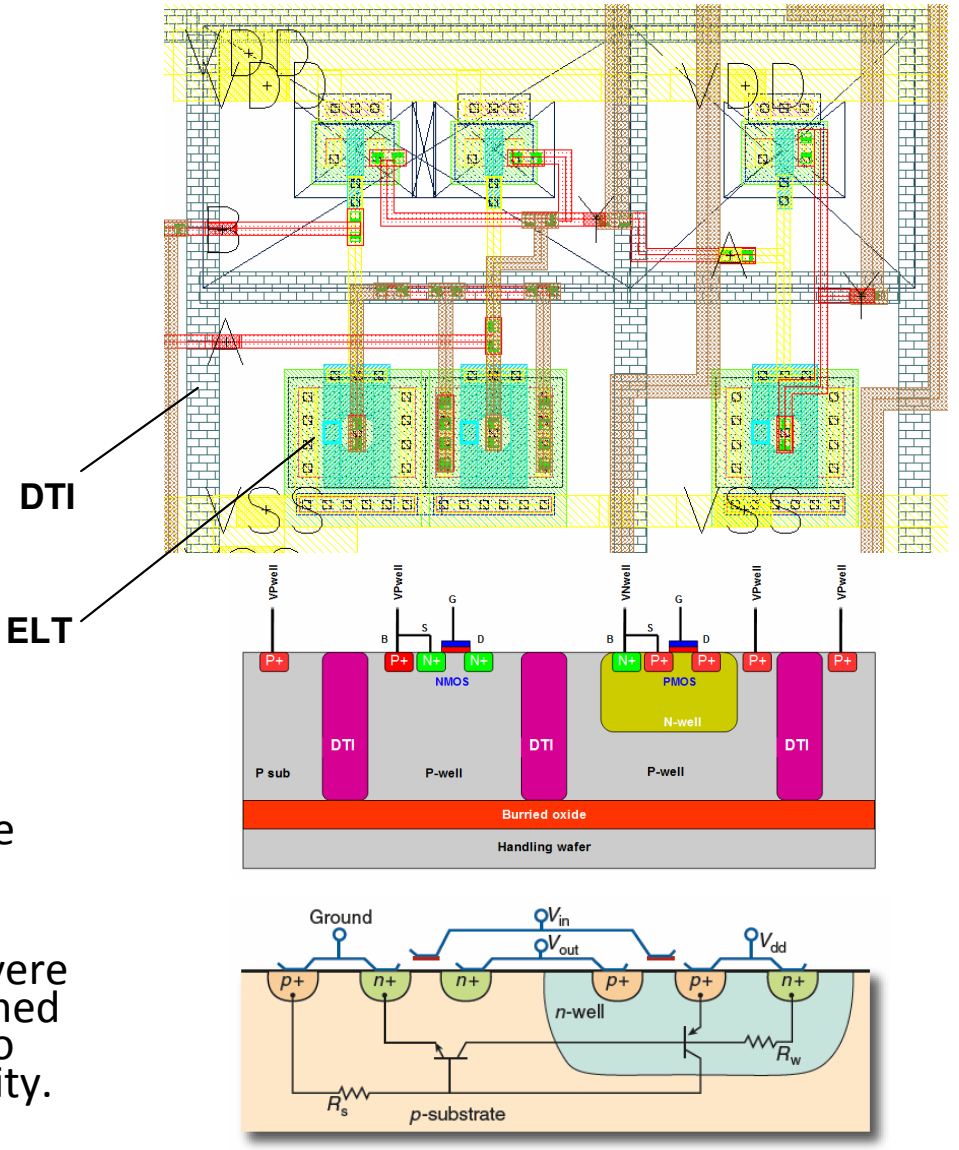
- **SINC CIC Decimator**
  - **4th order**
  - **Very efficient implementation**
  - **Integrators are allowed to overflow**
- **Half Band Decimator filters**
  - **Images of the baseband are only suppressed**
  - **Group delay: 1.35ms**

Filter ID	Order	Normalized pass-band freq., *Fo*	Sampling frequency in kHz
HBF1	6	1/48	96
HBF2	10	1/24	48
HBF3	14	1/12	24
HBF4	22	1/6	12

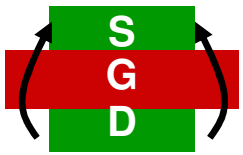


Radiation hardening: analog part

- **Deep Trench Isolation (DTI)** option cuts away the parasitic structures between PMOS and NMOS that may trigger SEL
- All NMOS transistors are of enclosed layout type (**ELT**) which greatly improve analog degradation due to TID effects (over-consumption due to severe leakage currents at edge formed parasitic channels)
- Relaxed layout rules



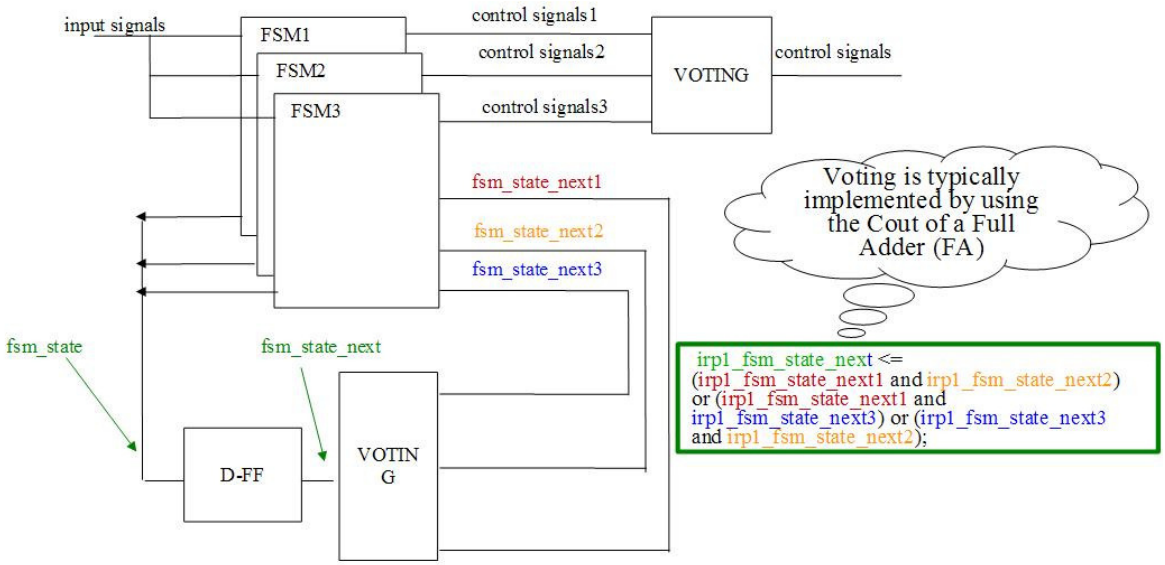
[fig: R. Mauerer, et.all, 2008]



- Radiation induced charges are trapped in the oxides or at Si interface.
- Over-consumption due to severe leakage currents at edge formed parasitic channels may lead to total loss of circuit functionality.

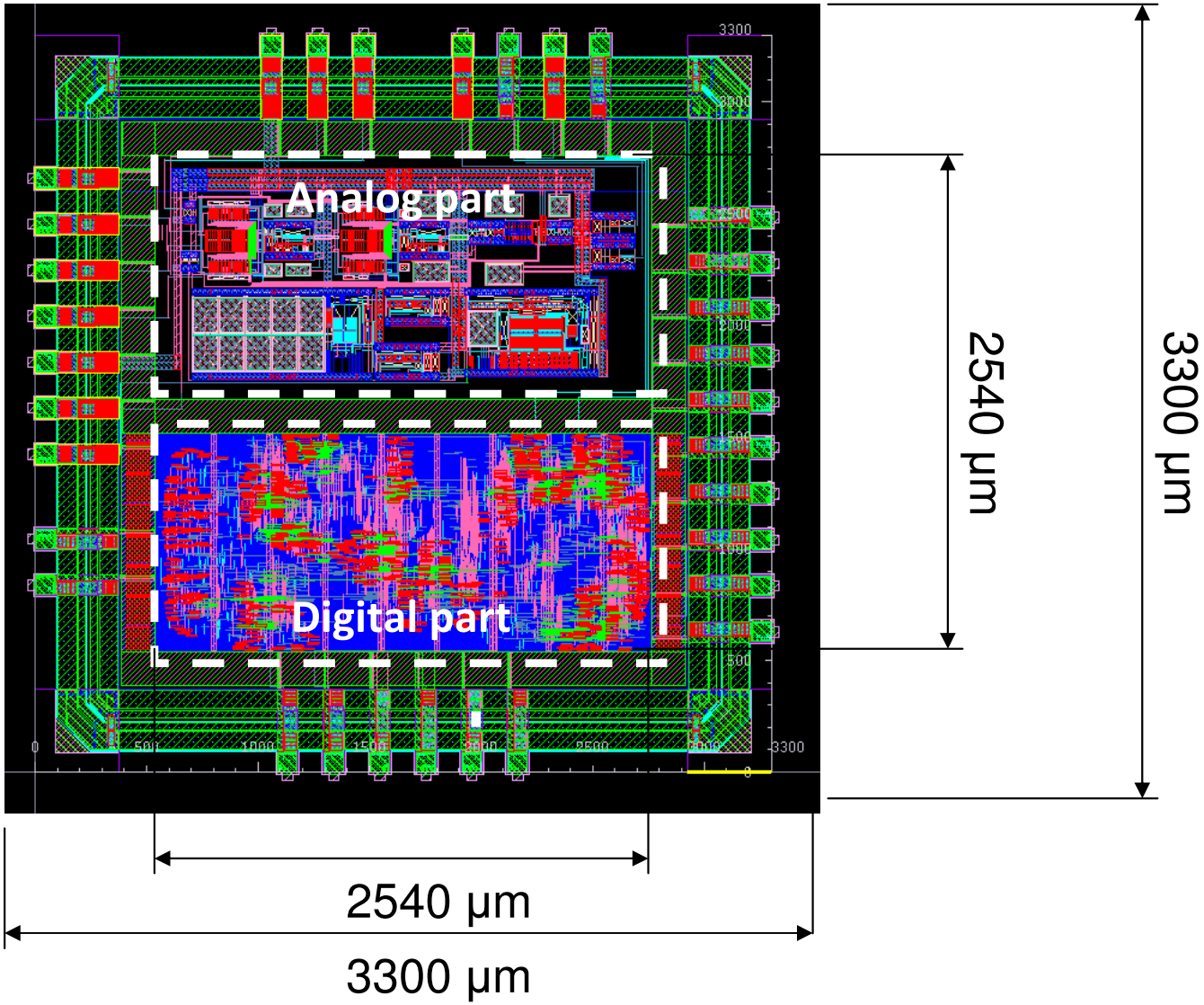
Radiation hardening: digital part

- **Technology level**
  - Atmel ATMX150RHA 0.15µm is a rad-hard proven technology.
- **Library level**
  - Oversized and robust standard cells were use (including latches and fli flops).
- **Digital design level**
  - Global insertion of TMR in FSMs and counters
  - Synchronous reset



Layout

- IP core area 6.45mm^2



Performance validation

AC performance, low sampling rate

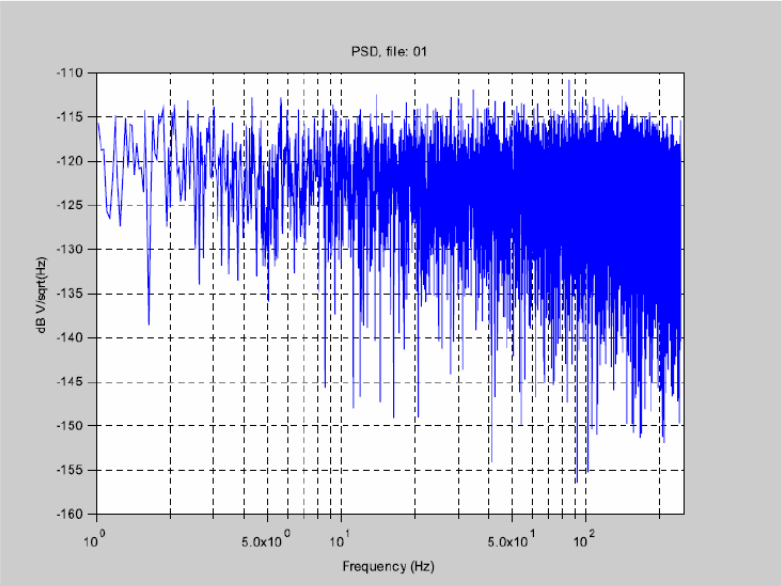


Figure 1: PSD for File id1 of Table 5 (f_{MCLK}=1MHz, 488Sps)

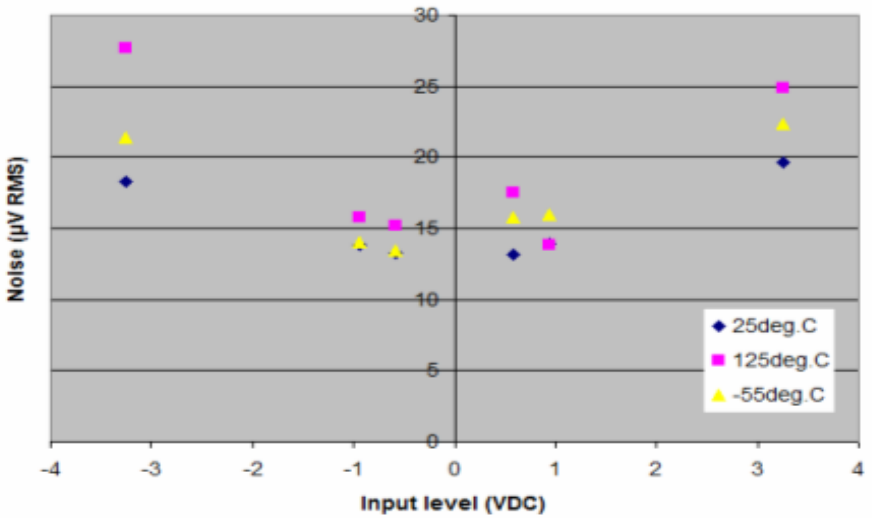


Figure 12: RMS noise vs input level across temperature (vsupply=nominal, OSR=2048, f_{MCLK}=1MHz, fs=488Sps)

- **Full Scale-to-Noise Ratio (FSNR):**
  - FSNR = $20.\log_{10}$(FS / RMS noise)
- where FS corresponds to the full scale input of the ADC and the RMS noise is the standard deviation of the perturbation of the amplitude of the measured signal.

Table 5. Low sampling rate AC performance

File idx	OSR	MEAN input voltage (V)	RMS noise (µV)	FSNR no post filter (dB) [2]	ENOB no post filter (bit)	FSNR with post filter (dB)[2],[3]	ENOB with post filter (bit) [3]
5	2048	3.250	19.6	106	17,7	119	19,7
4	2048	2.176	20.1	107	17,8	119	19,8
3	2048	1.453	14.8	107	17,8	119	19,8
2	2048	0.944	13.9	108	18,0	120	20,0
1	2048	0.583	13.2	108	18,0	120	20,0
6	2048	- 0.583	13.3	108	18,0	120	20,0
7	2048	- 0.944	13.8	108	18,0	120	20,0
8	2048	- 1.452	15.9	107	17,8	119	19,8
9	2048	- 2.175	22.3	107	17,8	119	19,8
10	2048	- 3.250	18.3	106	17,7	118	19,7

AC performance, high sampling rate

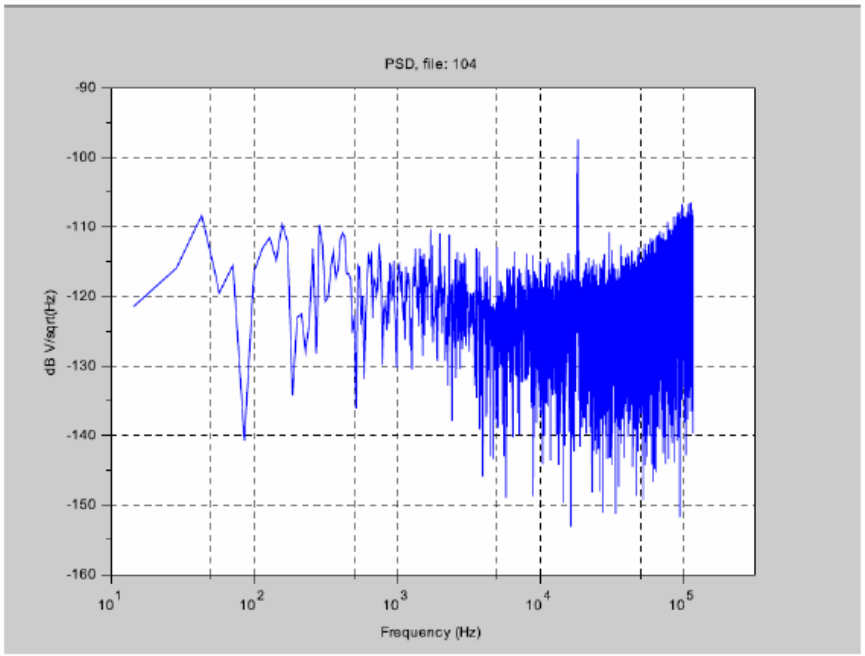
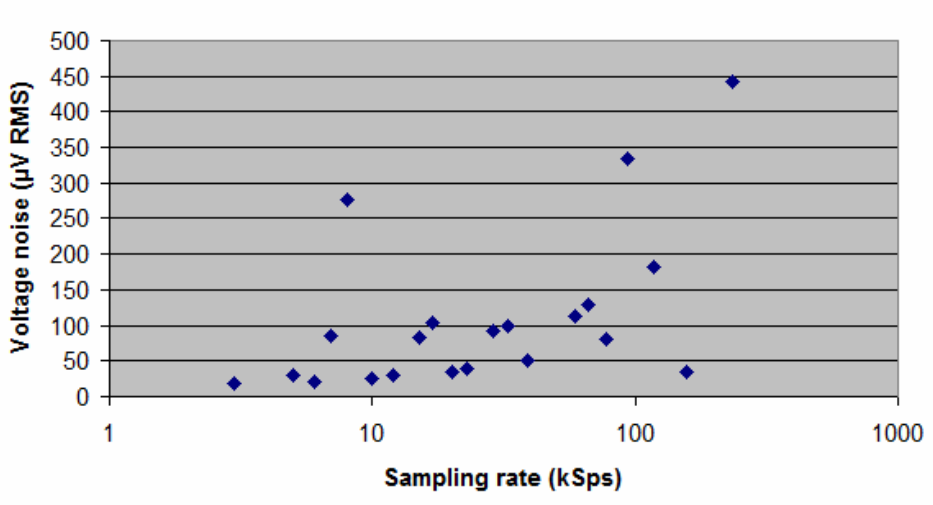


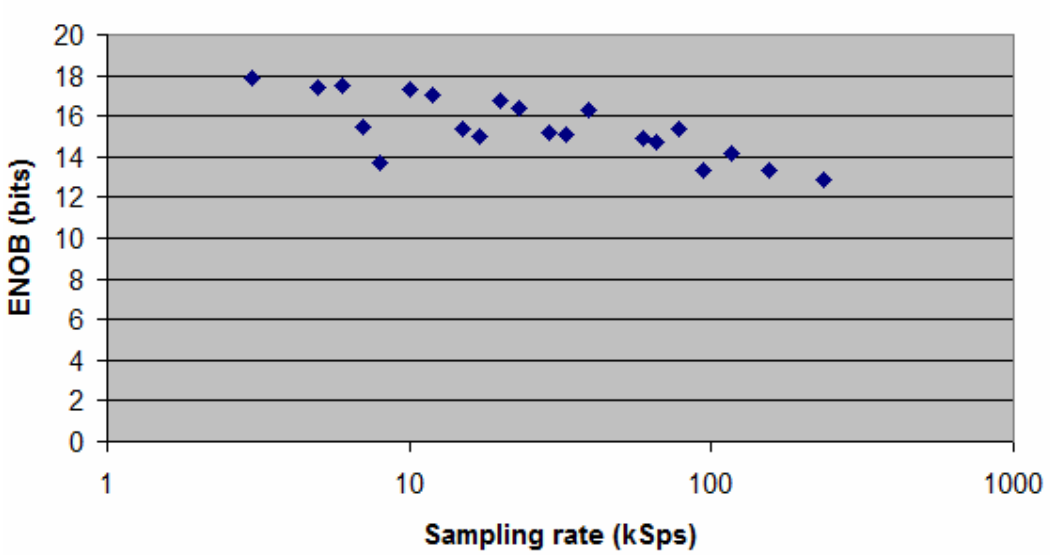
Figure 5: PSD for #21 of Table 6 (f_{MCLK}=15MHz, 234kSps)

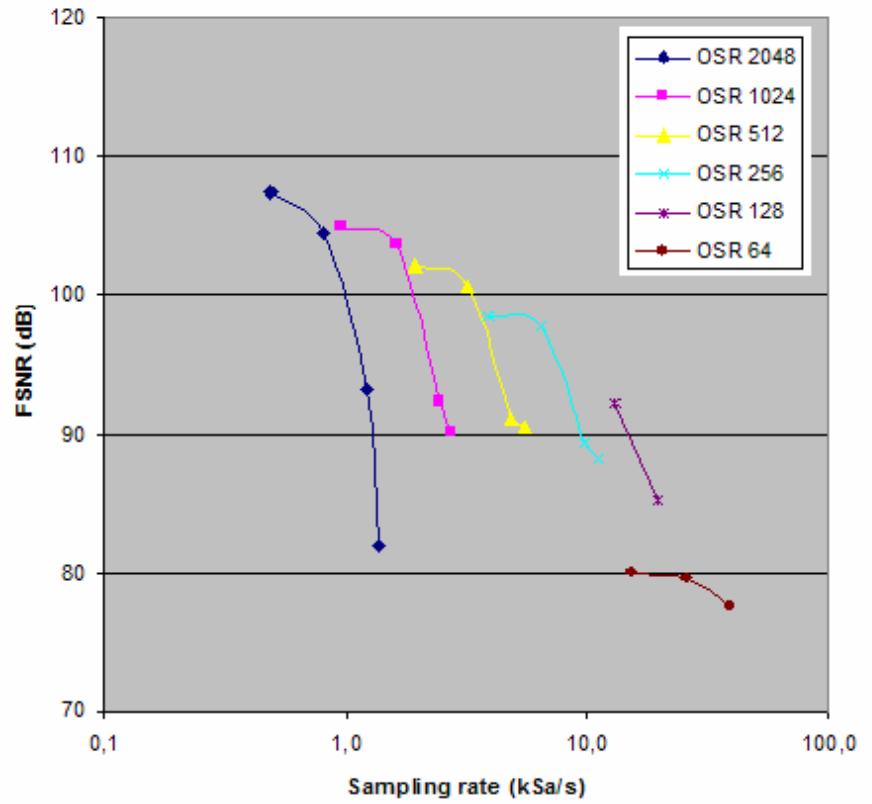


- **Maximum allowable clock**: 17MHz
- **Maximum sampling rate:** 265kSPS @ OSR x64
- **Bandwidth**: 45kHz

f_{MCLK} (MHz)	OSR	Sampling rate (kSps)	FSNR >1Hz (dB)	ENOB (bits)
6	2048	3	108	18
6	1024	6	105	17.5
6	512	12	102	17
6	256	23	98	16
6	64	94	80	14

Noise vs. sampling rate





*** without post processing (filtering)**

Power consumption

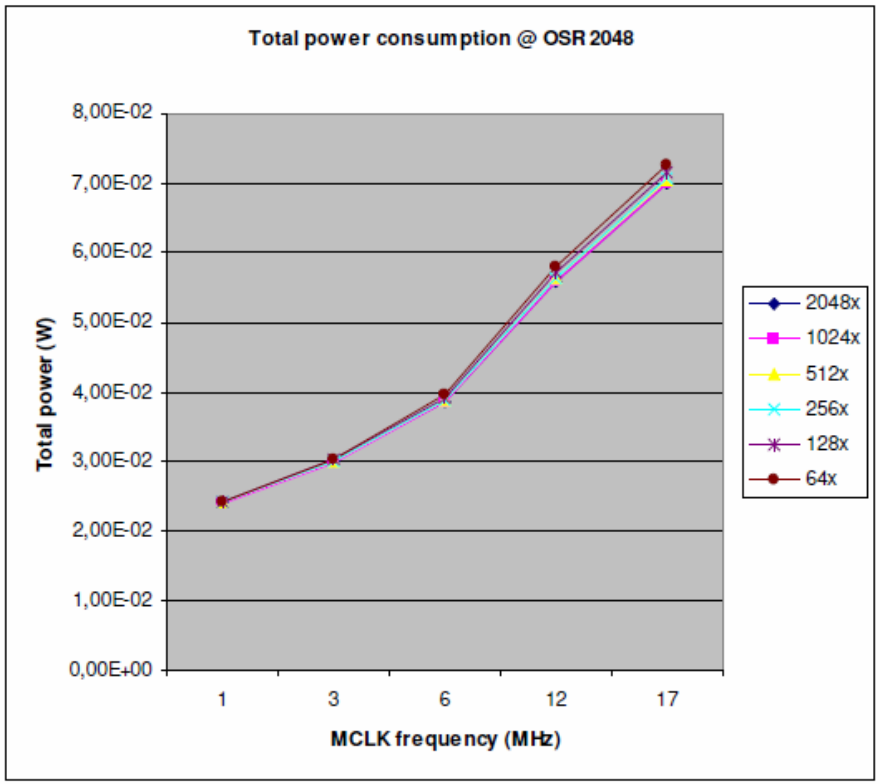


Figure 8. Total power consumption vs MCLK
(Ta=21 deg.C, nominal supply voltages)

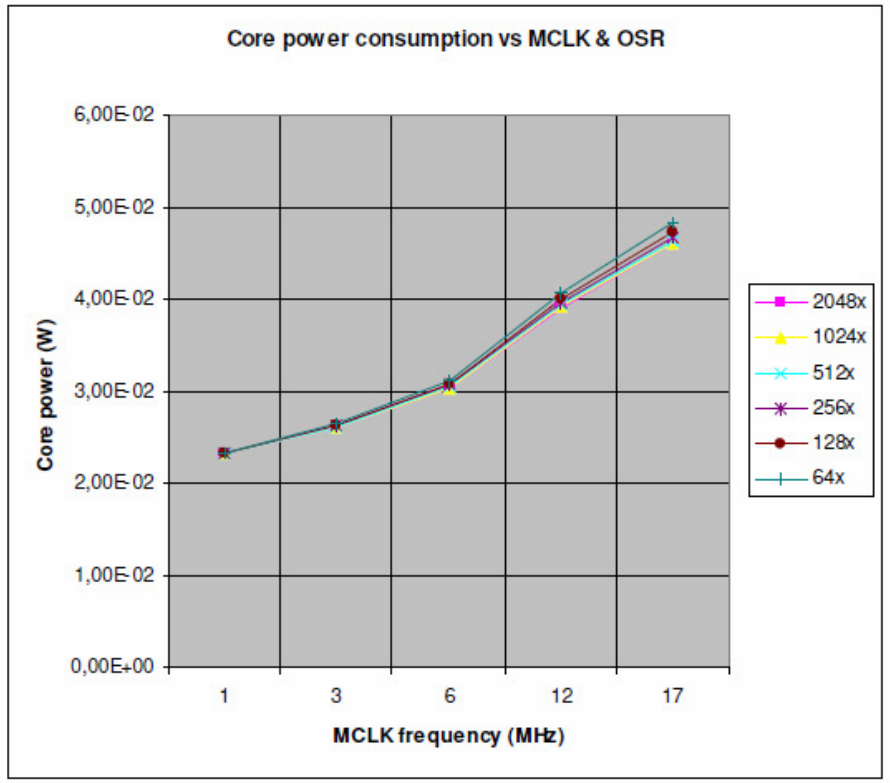


Figure 9. Core power consumption vs MCLK
(Ta=21 deg.C, nominal supply voltages)

Time domain AC response

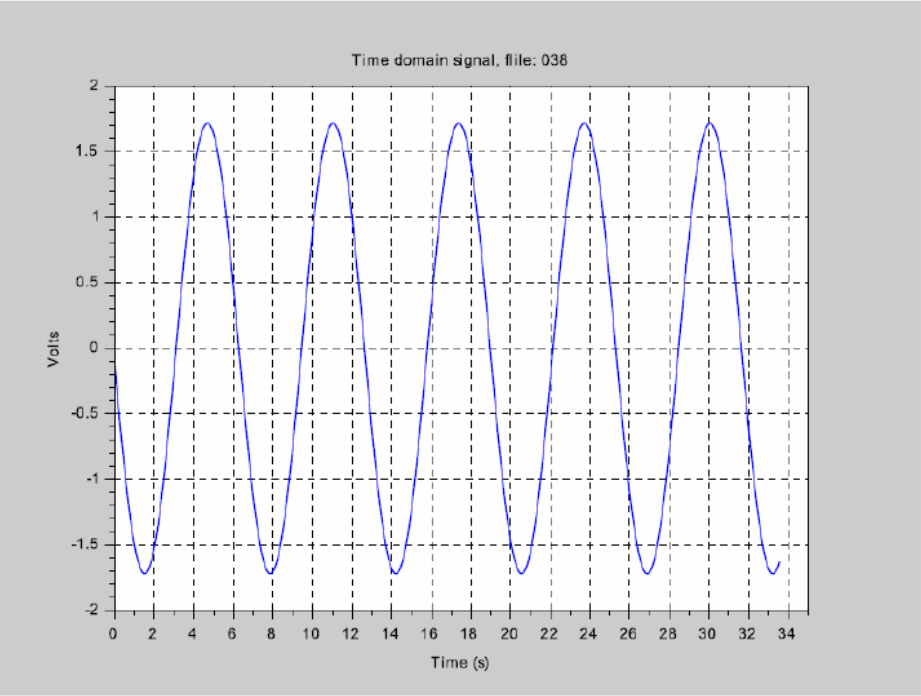


Figure 10. Sampled sine wave 0.16Hz, 3.2Vpp, at f_{MCLK}=1MHz, OSR=2048, 488 Sps

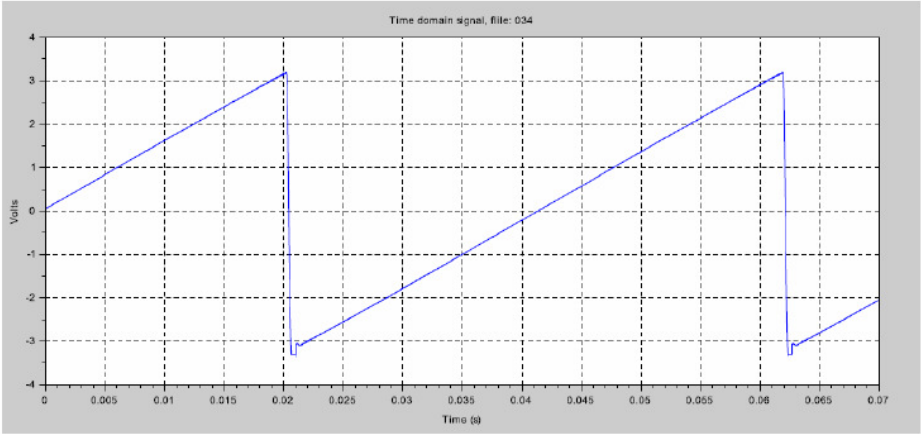


Figure 11. Sampled ramp signal 24Hz, 3.2Vpp, at f_{MCLK}=15 MHz, OSR=64, 234 kSps

Performance summary

Parameter	Condition	min	typ	max	Unit
Dynamic range	VIN=VINAP-VINAN differential	-3.3		+3.3	V
SNR	BW = 1Hz to 288 Hz to Nyquist frequency w.r.t to Full-Scale **FSNR**, -55ºC ≤ Ta ≤ +125ºC	108		105	dB
Noise	f_{MCLK}=1 MHz, OSR=2048 Sampling rate 488 Sps	13.2		22.3	μV_{RMS}
ENOB(*)	BW = 1Hz to 288 Hz to Nyquist frequency **(*) without post processing**	17.6		18	Bit
Sampling rate	Typ: OSR=2048x Max: OSR=64x		6	265	kSps
Core power consumption	-55ºC ≤ Ta ≤ +125ºC			50	mW
Total power consumption	C_L=5pF, Ta=21°C		25	80	mW
INL	Corresponding to 33% of FS and 17 bit resolution			1.5	LSB
Internal reference drift (band gap)	-55ºC ≤ Ta ≤ +125ºC		573		µV/°C

Total Ionizing Dose Tests (TID)

Test conditions & parameters

- **Time & place**: Sept. 2017 at ESA-ESTEC
- 4 irradiated samples + 1 control device
- **During exposure**
  - Irradiation of DUT under bias (max voltage)
- **Between the exposures**
  - **Supply current** at various op. modes
  - **Offset error** at var. sampling rates
  - **RMS noise, PSD, SNR, ENOB** at var. sampling rates

TID test bench

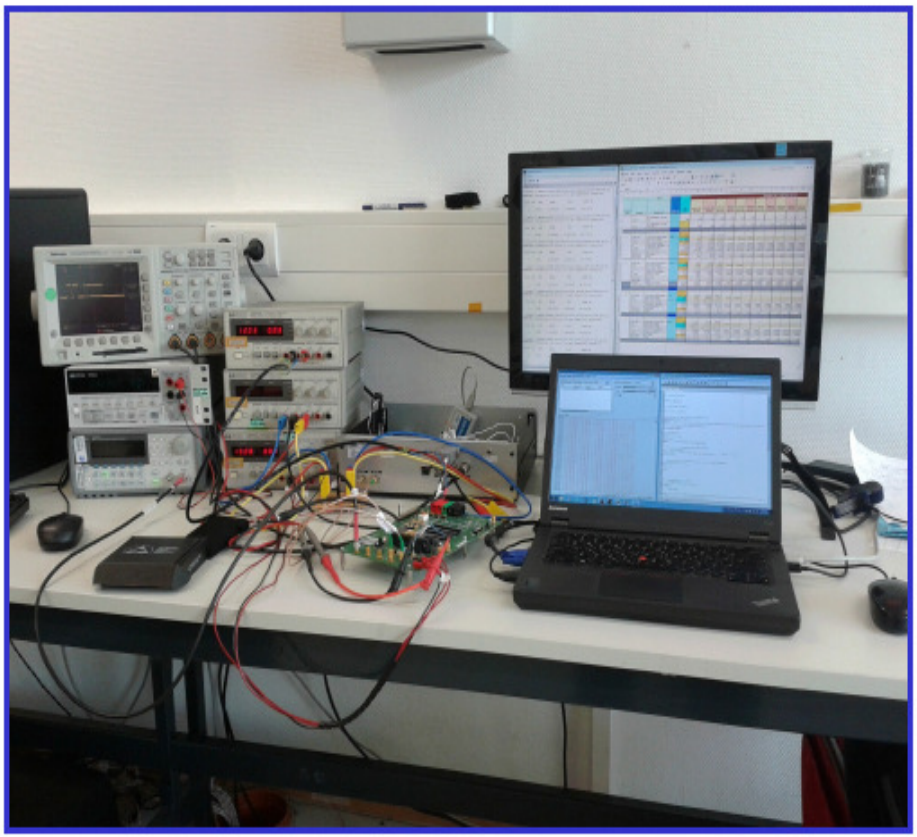


Figure 5.2: Measurement test bench at ESTEC

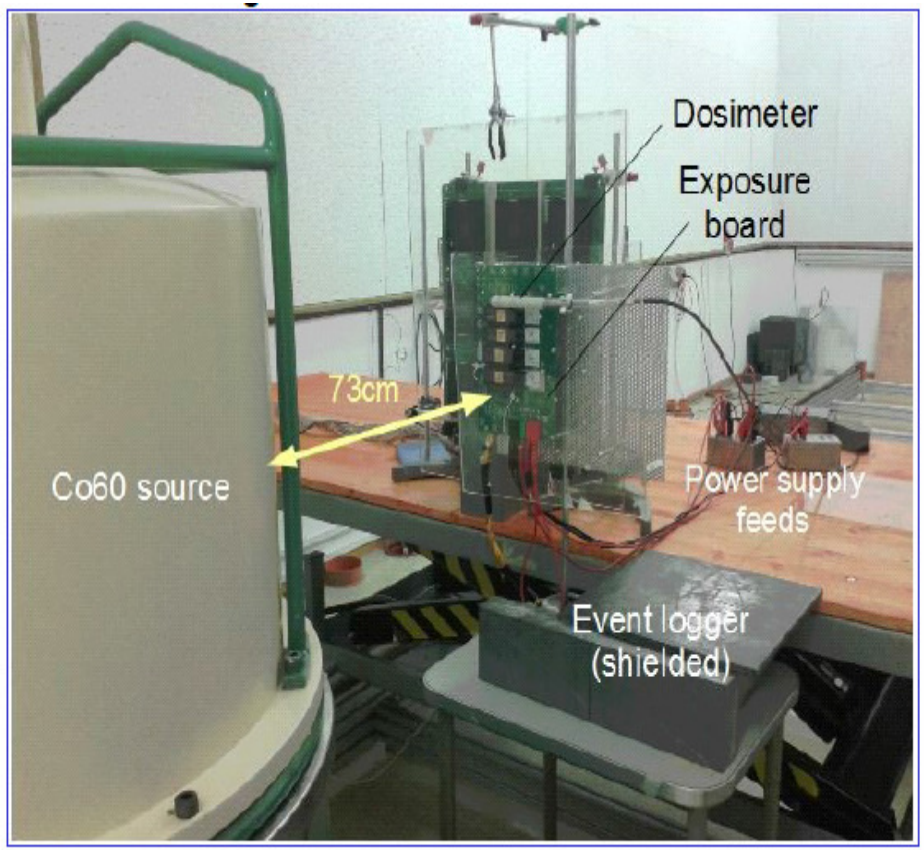


Figure 5.3: Irradiation setup at ESTEC Co60 facility

Radiation dose plan

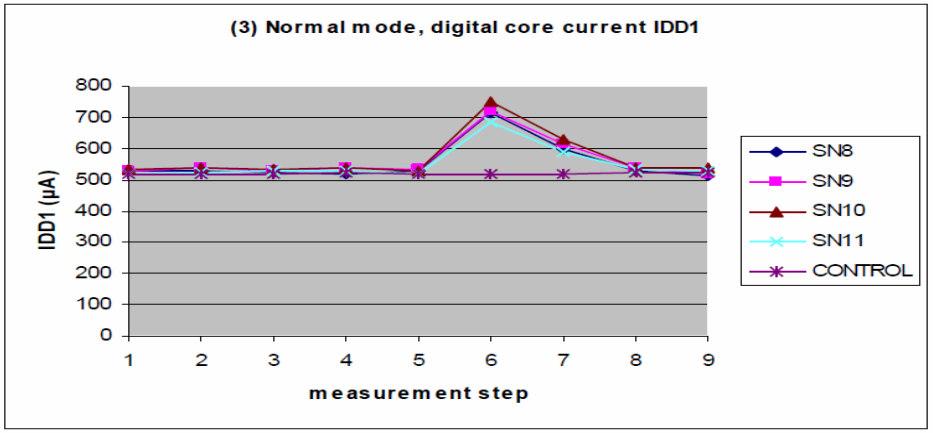
- 5 irradiation steps
- Total accumulated dose **300krad Si**
- Steady dose rate **59 rad/min**
- Total irrad. time **83h 56m**
- Annealing for 168h at ISD
- Ageing for 168h at ISD

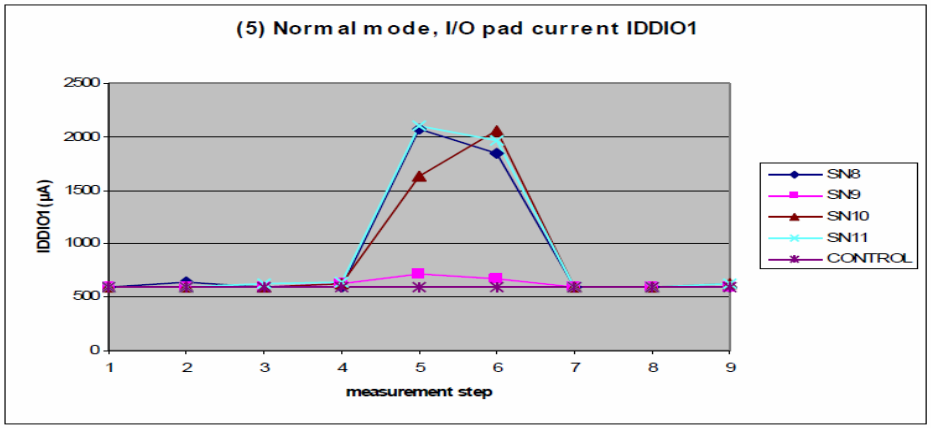
step	
1	initial
2	21krad
3	67krad
4	83krad
5	133krad
6	300krad
7	anneal. 24h
8	anneal. 168h
9	ageing 168h

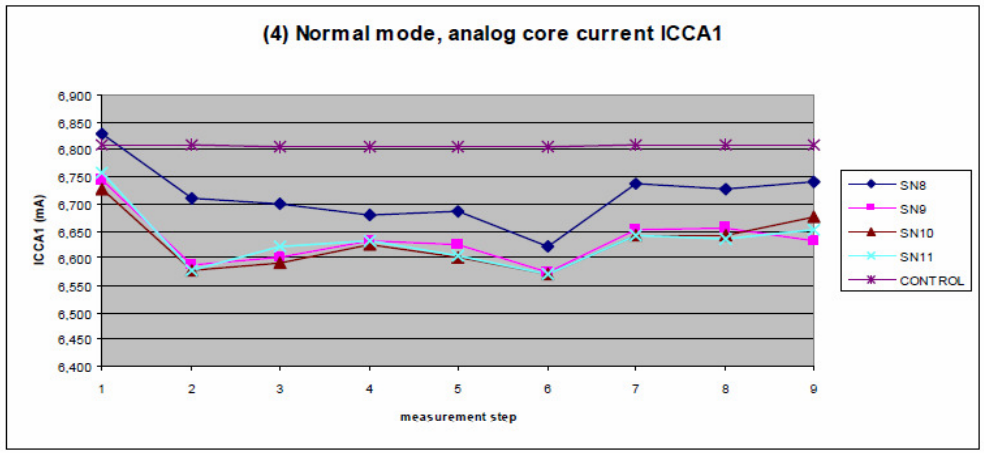
Irr. run	Total ionizing Dose (water) Gy	Total Ionizing dose (Si) krad	Cummulative dose (Si) krad	Dose rate (water) Gy/h	Dose rate (Si) rad/min	Irr. Time (hh:mm:ss)
1	241,8	21,5	21,5	39,94	59,24	6:03:15
2	515,4	45,9	67,4	40,23	59,67	12:48:41
3	177,4	15,8	83,2	40,11	59,50	4:25:22
4	558,6	49,7	132,9	39,84	59,10	14:01:16
5	1848,0	164,5	297,4	39,63	58,78	46:37:53
Total	3341,2	297,4	297,4			83:56:26

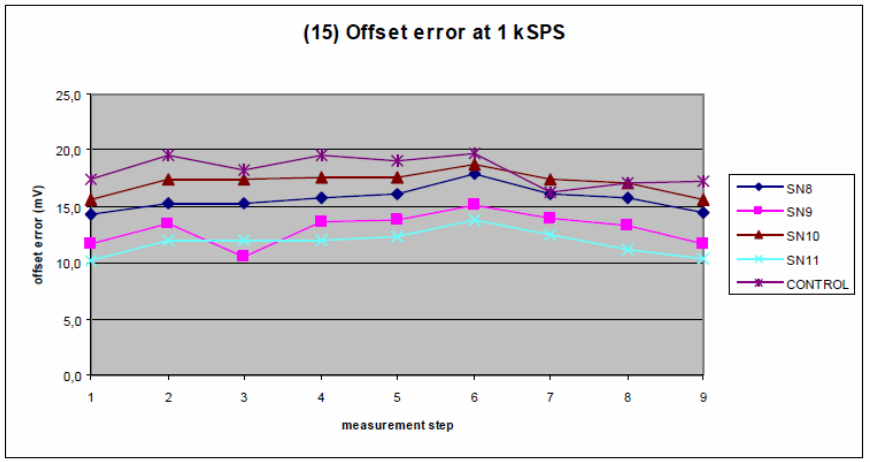
Table 5.4: Radiation dose summary (Si deposition)

TID test results: DC parameters









TID test results: AC parameters

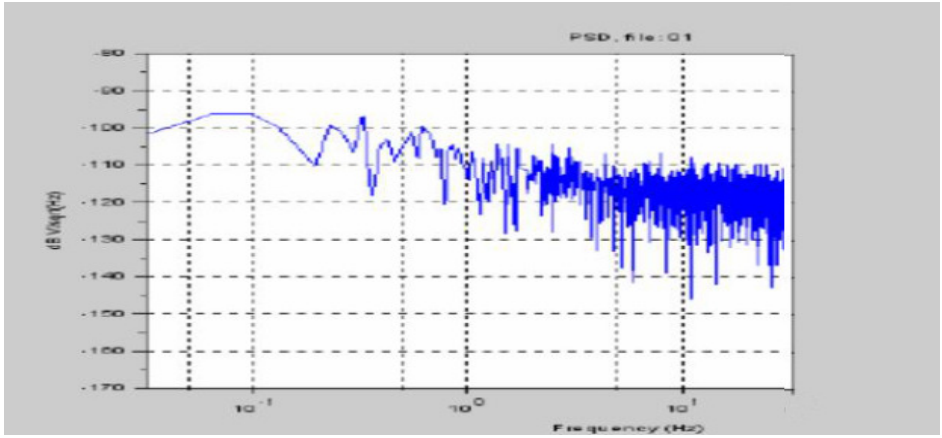


Figure 5.5: PSD, 100% (FS) input, SN11 initial

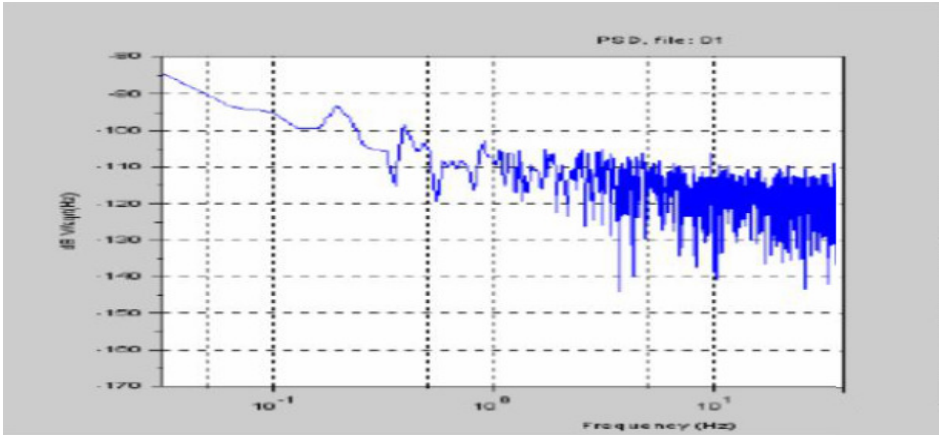


Figure 5.15: PSD, 100% (FS) input, SN11, 300krad

TID testing conclusion

- All the samples remained fully functional throughout the test campaign
- The leakage current of the digital core and the I/O pads increased by **13-20 times after** the **133krad** step but fully recovered at the end of the campaign
- **Noise and SNR**: no noticeable degradation in any of the sampling rates tested up to 300krad dose
- **Target TID value ≥100krad confirmed**

SEE Tests
(Heavy Ions)

HI test bench

- FPGA based data capture platform
- Custom S/W development for experiment monitoring and data logging
- 3-CH SEL monitor
- Test signal DAC module
- 1MSPS full custom Data Acquisition card

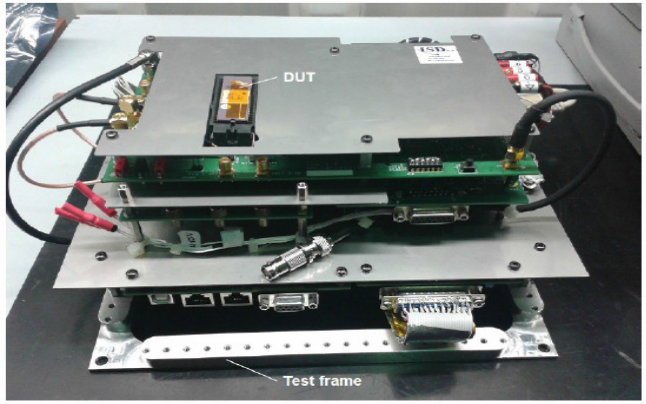


Figure 6.4: Heavy-ion test-bench assembly

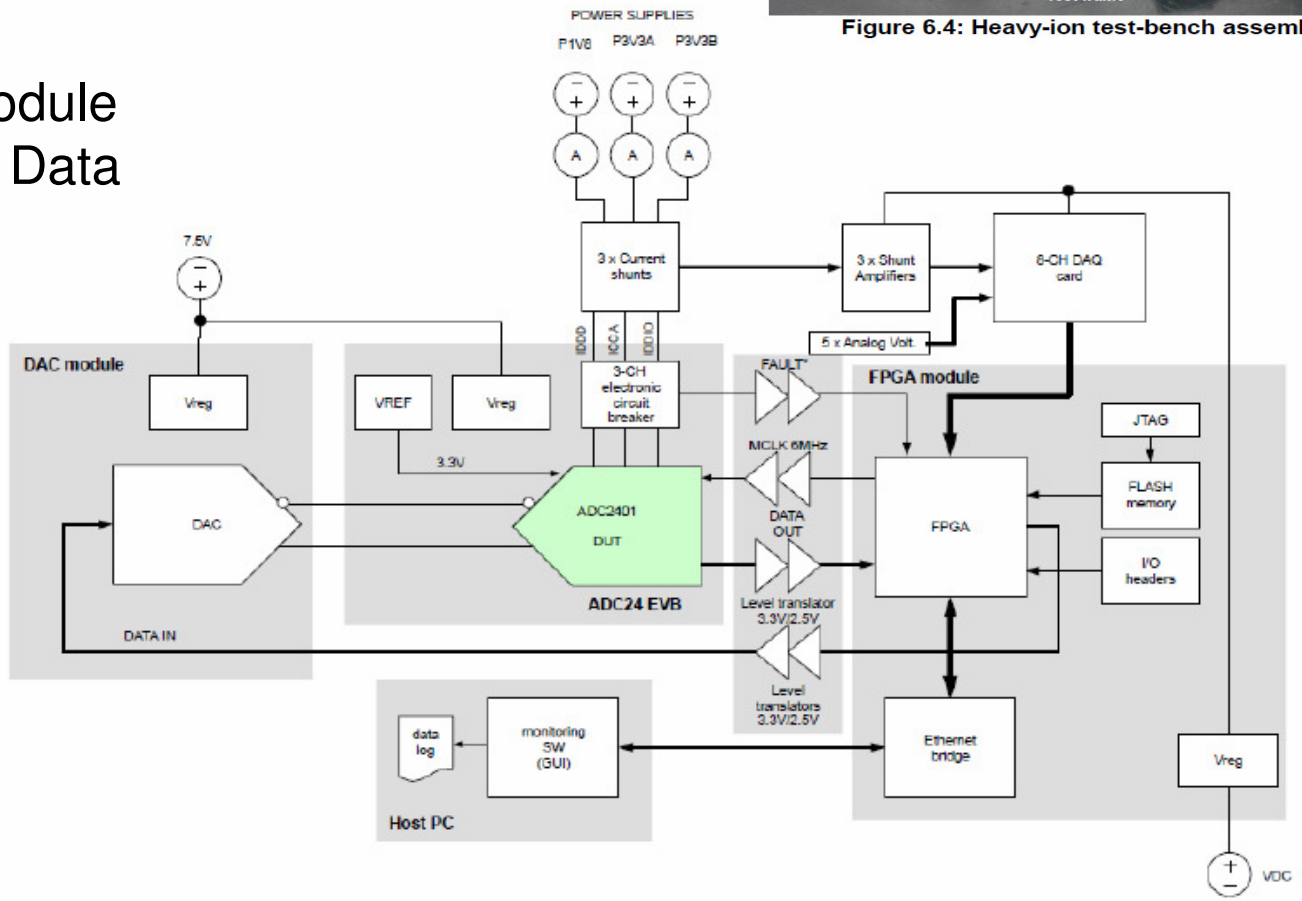


Figure 6.1: Heavy-ions test bench block diagram

HI test bench at UCL

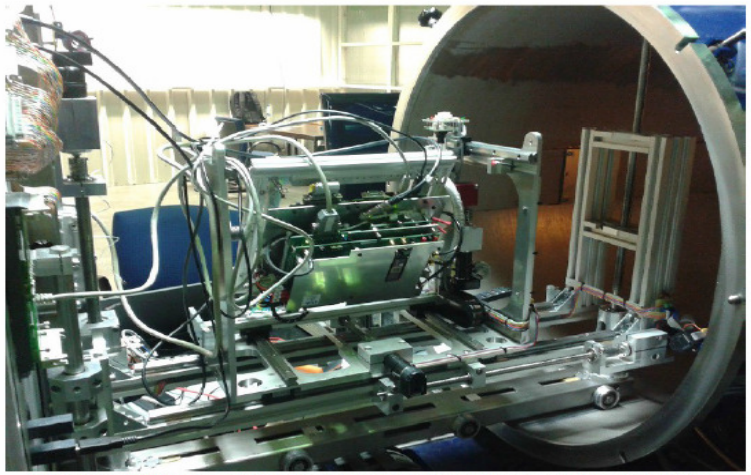


Figure 6.2: positioning of the test-bench inside the chamber

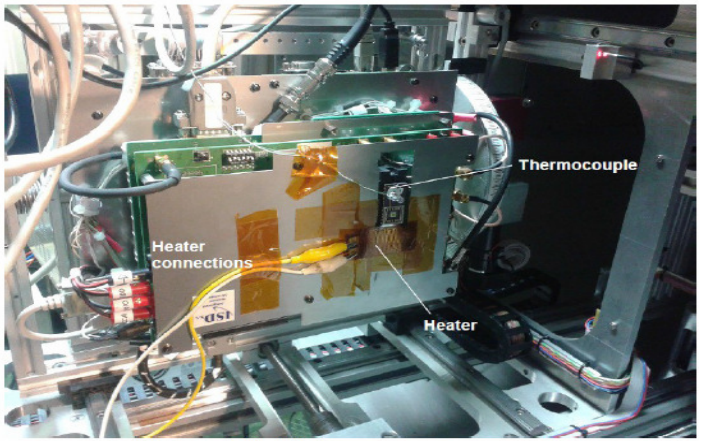


Figure 6.5: high temperature setup

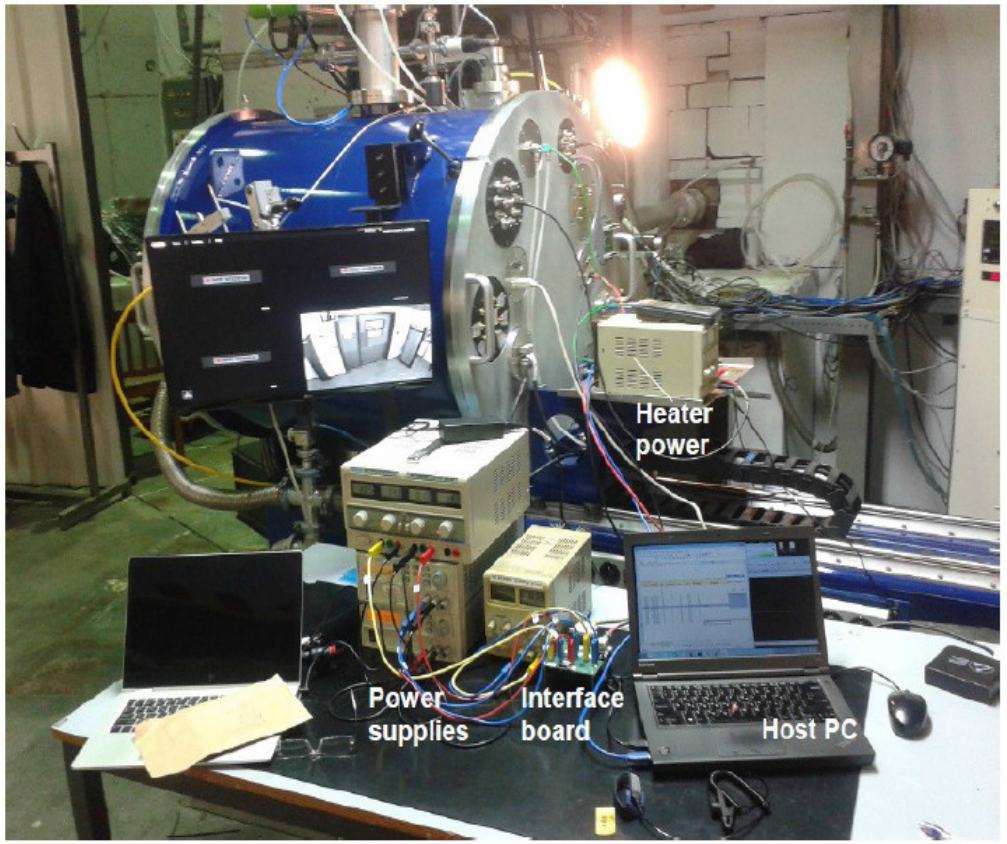


Figure 6.3: HI test-bench overview

Test conditions & parameters

- **Time & place**: Dec 2017 at UCL Louvain in BE
- 24 test runs in total
- 3 irradiated samples
- **Test parameter variation**
  - LET → type of ion and/or incident angle
  - Supply voltage
  - Sampling rate
  - Temperature
- **Test signal**
  - Linear ramp ±0.5V differential
  - Each slope quantized to 32 steps
  - Period 1s
  - Step duration: 15.6ms

HI testing conclusion

- All the samples fully functional throughout the test campaign
- All the tested samples immune to SEL, SEU, and SEFI up to LET of 88.4 MeV/mg/cm^2
- Some SET on the analog and the I/O buffer consumption was observed, deemed as insignificant
- **Target value for SEL immunity ≥70 MeV/mg/cm^2 confirmed**

Conclusions

- Performance is beyond expectations
- Wider target accessible market
  - High reliability instrumentation and data acquisition
  - Precision test and measurement
  - Process control
- Radiation endurance exceeded the target specifications

Thank you for your attention!

Questions?