DARE SET Simulation Flow Integrated in Virtuoso ADE L/XL Design Environment

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Abstract

One of the important steps when doing radiation hardening by design for mixed-signal and analog blocks is simulation of SET events. It is needed to find the SET sensitive nodes in a design and then adapt the design to bring the SET hardness in compliance with the specification. In order for an analog designer to do this efficiently the tools used should be integrated in the normal analog design flow. It should be flexible enough to screen for sensitive nodes in a design and later on focus on certain nodes. In analog design the timing of an event is important as a strike often only generates a non-compliant SET on the output when the circuit is in a certain state or transition. The timing may be dependent on the simulation corner and ideally the testbench should not need to be changed for this dependence. Additionally it should be avoided that a certain circuit has to be adapted to be able to inject an SET pulse in any node in its hierarchy.

In this paper the history of the SET simulation environment used in imec for DARE[1] is presented and the discussion of current state as used for the DARE65 project within imec.

I. SET Simulation Flow and its History

In this chapter the current SET simulation flow used in imec is discussed based on the history of the introduction of the different features. The history shows the different steps taken to fulfil the requirements of an efficient and user friendly SET simulation flow.

A. Ocean Scripts

As already discussed in [2] at AMICSA 2016 our SET simulation flow originally started from Ocean scripts that did SET injection in all nodes on a netlist. This flow is still used at imec for example for the screening of a standard cell library for SET sensitivity. But for analog design this flow was not considered ideal. Ocean scripting and working on netlist level is not typically the level an analog designer will work. It also does not cooperate well with all the analysis capabilities provided by tools like Cadence Virtuoso ADE XL or Cadence Virtuoso ADE Assembler; a lot of manual intervention is needed to make that possible and own custom post-processing needed to view and summarize the results.

So development has been started on a SET flow more integrated in the Cadence GUI based analog design flow. This is described in the following paragraphs.

B. SET Striker Verilog-A Model

The first step taken was to implement a device that can be instantiated in a circuit schematic and allows to perform SET injection during simulation.

All p-n junctions in a circuit are possible collection points for generated electrons and holes by particle strikes. The effect of the collected charges can be represented as a current injected from the n-side of the junction to the p-side of the junction. In Figure 1 an instantiation of the SETstriker cell that provides this functionality is shown in an example circuit. The SETstriker cell is implemented by a Verilog-A model that generates a double exponential current injection. The time constants of the double exponential curve are hard coded in the Verilog-A model and based on literature ([3],[4]).

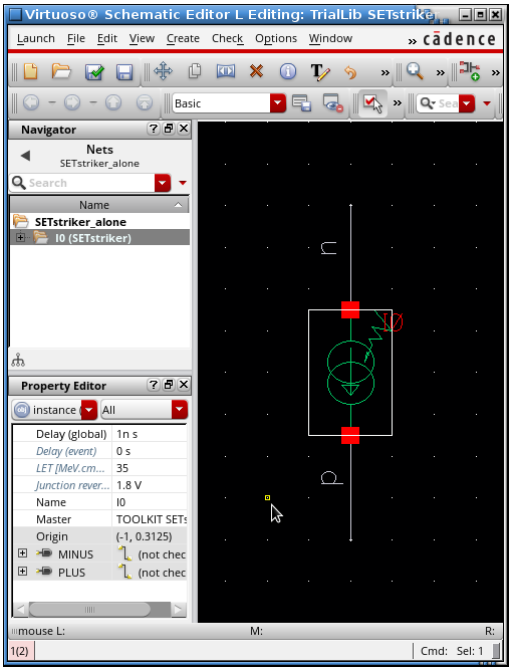

Figure 1: SETstriker Verilog-A element

The total charge Q injected over the time of an SET event is dependent on the energy of the particle that generates the charge and on the collection depth. As shown in Figure 1 the energy of the particle is a parameter of the cell. The collection depth is tuned by the voltage over the related junction. Other technology parameters affecting the collection depth are hard coded inside the Verilog-A model. The two other parameters for SETstriker cell are delays that allows to time the SET event. There is a global delay and an event specific delay. The first parameter is to be used to move all SET events to a certain time in the simulation and the second one to let each event happen one after the other.

C. *Use of Deepprobe*

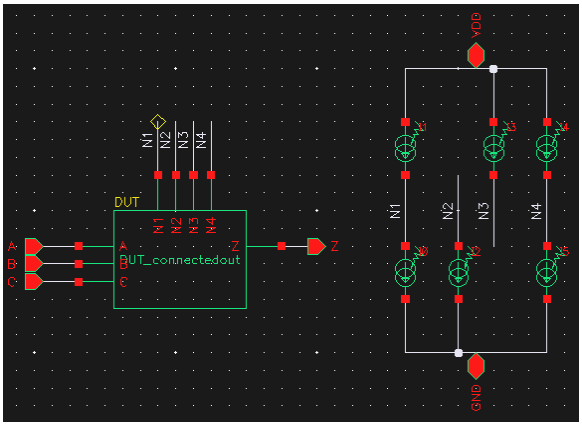

Figure 2: Testbench with DUT with internal nodes connected out

In Figure 2 an example test bench is given that shows how this SETstriker can be used for injection into a Device Under Test (DUT) to investigate its SET sensitivity. In this example N1 and N2 are connected to diffusion area of both a NMOS and PMOS, N2 of only a NMOS and N3 of only a PMOS. The nodes to be injected in the DUT have been connected out which means the design needs to be adapted to allow SET simulation. Especially when there are multiple levels of hierarchy or a lot of nodes in the design this becomes tedious. The deepprobe cell has been introduced to ease this. The schema from Figure 3 performs the same functionality as in Figure 2 but without the need to adapt the design of the DUT. The four instantiated deepprobes allow to connect to the nodes inside the DUT by a hierarchical name given as parameter. The deepprobe is a cell originally downloaded from the Cadence support website and is now available in the analogLib of the latest releases for Virtuoso.

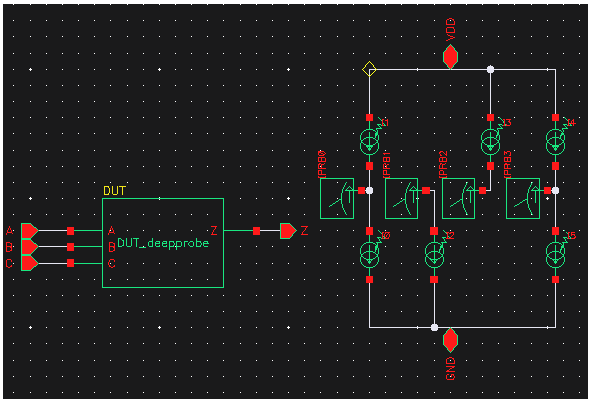

Figure 3: Test bench using deepprobes for injection

D. *Use Periodic SET Striker and Dual Deepprobe*

If a lot of nodes need to be investigated or one wants to focus later on only on a subset of the nodes this setup is still tedious. A SETstriker and a deepprobe needs to be instantiated for each node and the timing has to be set up. For reducing the simulated nodes set, instantiations need to be removed again and the timing of all SETstrikers needs to be updated. Two new cells have been introduced to make this flow more fluent: a periodic SETstriker and a period deepprobe switcher with two inputs. The periodic striker generates events with a specified period and allows to replace all SETstrikers with one in a schema. The periodic deepprobe allows to replace all deepprobes with one. A paremeter of the the deepprobe referes to a text view which list the nodes to connect to. The extension to two inputs of the deepprobe allows to combine the events generated on the diffusion area of both NMOS and PMOS transistor by taking always the n-type region as first node and the p-type region as second node. The cells have some extra outputs that allow to easily monitor the state of the device, e,g, it will show the number of the event and the time the event has started. With the event number the corresponding nodes can be looked up in the nodes list.

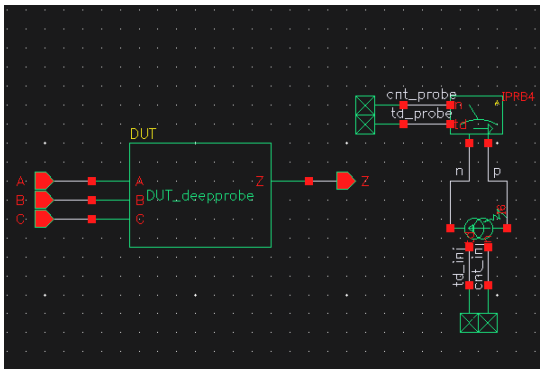

Figure 4: Testbench using periodic striker and deepprobe

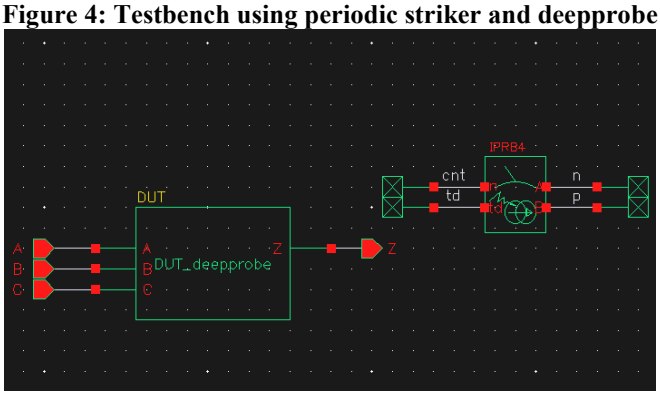

Figure 5: Test bench using combined periodic striker+deepprobe

An updated test bench with the same functionality is shown in Figure 4. Most of the time the periodic probe will be combined with a periodic SETstriker. So for this purpose a cell is provided that combines the two functionalities and is used in the test bench presented in Figure 5; again with the same functionality. The node list is Skill code in text view and has the following content for this test bench:

```
probes = '("Probes")
probes->list = '(
   ("/DUT/N1" "/GND")
   ("/VDD" "/DUT/N1")
   ("/DUT/N2" "/GND")
   ("/VDD" "/DUT/N3")
   ("/DUT/N4" "/GND")
   ("/VDD" "/DUT/N4")
)
```

This text file can be easily edited to add or remove nodes from simulation. So one can easily start with a broad screening of the nodes in the DUT and then later on focus on a small subset of the nodes by editing the file without any other changes needed in the test bench.

E. *Using Triggered Striker and Deepprobe*

Up to now the SET events generated on the nodes in a DUT have always be done after a fixed amount of time and repeated with a fixed period. Sometimes one would like to start generating events when the DUT has reached a certain state. For this purpose a SETstriker+dual deepprobe are provided that will generate an event triggered by a rising edge on an extra input and a configurable threshold value.

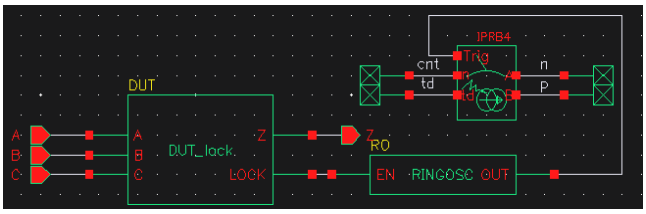

Figure 6: Test bench using combined triggered striker+deepprobe

In Figure 6 this is shown on a test bench where the DUT provides a lock signal – a signal that often is an output of a PLL. The lock signal is used in the test bench to enable an oscillator that drives the trigger for generating the SET events. In this way only events will be generated after the DUT is in lock state. In this example the combined SETstriker+deeppprobe cell with a trigger input is shown but for the separate SETstriker and the dual deepprobe also versions that work on a trigger signal are available.

F. *Node Selection GUI Support*

With the introduced cells a SET simulation can be performed easily in Virtuoso but generating the list of nodes can still be a labour intensive task and important nodes may be overlooked. For this reason a tool is provided that lists all SET generating junctions in a DUT and allows to select on which nodes to inject a SET.

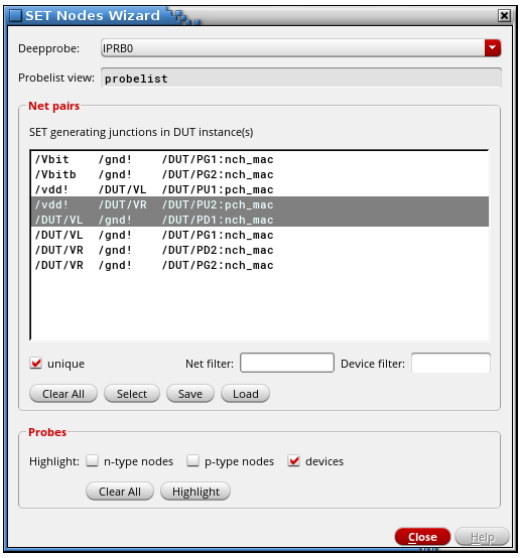

Figure 7: SET sensitive nodes selection and investigation

In Figure 7 the window of the tool is shown when applied to a classic 6T-SRAM cell. A 6T-SRAM cell – as the name indicates - contains 6 transistors: 2 NMOS pull-down transistors, 2 PMOS pull-up transistors and 2 NMOS pass gates. In the GUI a list is provided of all the event generating junctions. The first column lists the net connected to the n-type region of the device, the second column the one to the p-type and the third column the device that contains this junction. The net combinations one wants inject SET events into can be selected from the list and saved in a text view. In this case the two events on the internal nodes were selected that can cause a SEU on a 1 stored in the SRAM cell.

II. Status and Future Work

The current release version of the DARE180U Analog Design Kit (ADK) contains the single event SETstriker and the deepprobe; for DARE65T no ADK is released yet. The plan is to include the updated flow in the next release of both the DARE180U and DARE65T ADKs.

Part of the Verilog-A SETstriker model is based on literature and so not on exactly the same technology as used for DARE. Efforts are ongoing to verify and possibly improve the model. For both technologies TCAD effort is ongoing and for the DARE180U technology a SET test chip is available and waiting for testing.

III. Summary

In this paper the current SET simulation flow as used in imec for the DARE65 project is discussed. An overview of the evolution is given. The current flow allows an analog designer to investigate SET sensitivity and perform radiation hardened by design (RHBD). The flow is built on the Virtuoso design flow and integrates efficiently in a typical analog design flow. In the DARE65 a SET verification test chip is in the planning.

IV. Acknowledgements

This SET simulation and radiation hardened by design flow has been developed within the DARE180 and DARE65 ESA projects. Discussions with ESA experts and the users of our DARE technologies are a big inspiration for the improvements to the flow. Especially the guidance and feedback of Boris Glass and Richard Jansen have contributed to where we are now.

V. References

[1] Imec DARE website: http://dare.imec-int.com/en/home

[2] S. Verhaegen et.al. (2016, June).”Incorporating more in-depth radiation knowledge in the DARE180U analog design kit”. Presented at AMICSA 2016; https://indico.esa.int/indico/event/102/session/9/contribution/48

[3] Rajesh Garg, Sunil P. Khatri (2006) “Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations”, Springer

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