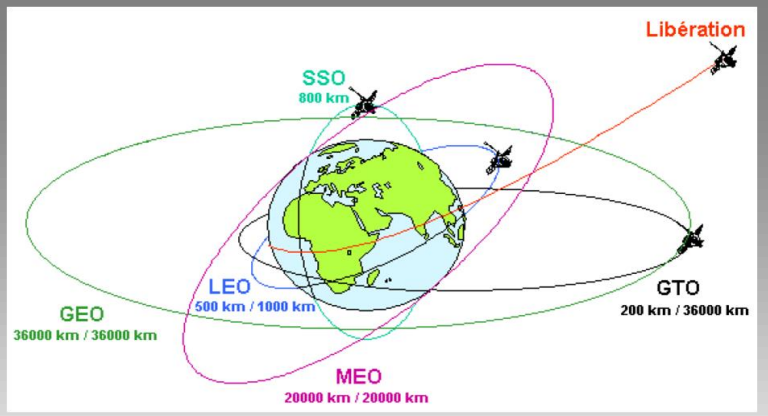

MICROCHIP

Aerospace & Defense BU

Radiation Characterization

ATMX150RHA Rad-Hard Platform
The solution for mixed-signal ASIC

Project supported by CNES

June 20, 2018

ATMX150RHA PD-SOI 150nm Technology

- **Funded by CNES (Centre National d'Etudes Spatiales)**
  - Evaluation and Qualification of ATMX150RHA ASICs offer
  - Radiation Evaluation of LDMOS : TID and SEB/SEGR

    CNES CONTRACT n° 4500037909 / DCT094 of 2011.09.27

    CNES CONTRACT n° 4500044431 / DCT094 of 2013.10.24
  - Radiation Characterization of other devices (HV, MOS 5V, Bipolars & Capacitors) : TID and SEB/SEGR

    CNES CONTRACT n° 4500053131 / DCT094 of 26.08.2016

Microchip ATMX150RHA Rad-Hard CMOS 150nm cell-based ASIC family
Radiation Characterization Test Report - Total Dose (TID) and Single Event Effects (SEE)

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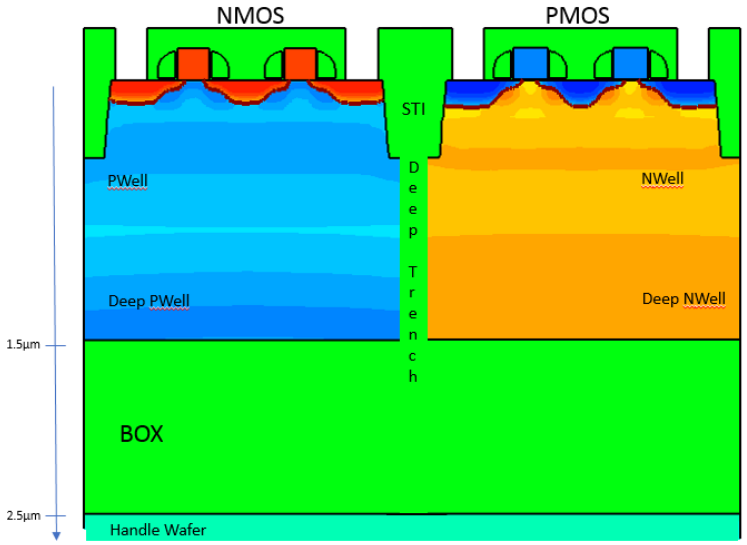
CENTRE NATIONAL D'ÉTUDES SPATIALES

ATMX150RHA – GENERAL FEATURES

- **150nm SOI CMOS process**
  - 5 Level Metals + Thick Metal AlCu / 1.8V core supply
  - Life time 20 years at Tj=110°C
  - **Dual deep-well** for SEL immunity
  - **Deep Trench** option
- **Hardened Library**
  - Logic std cells and DFF
  - Hardened I/Os 5V, 3.3V & 2.5V, LVDS, PCI
  - High Voltage Devices
    - 25V, 45V LDMOS
  - A catalog of pre-qualified analog blocks
    - Regulators/ PLL/ RC-Oscillator/ BandGap/ Comparator/ Analog-MUX/DAC-ADC…
- **Virage compiler of SRAM/DPRAM/ROM**
- **Qualification of Hardened ASICs (-55°C to 125°C) up to 22MGates equivalent NAND2**
  - Standard Evaluation Circuit (SEC) with **44M transistors**



View of ATMX150RHA technology

ATMX150RHA – PDK Devices Content

Device type	Domain	Device Name	77KRHA 1.8V/3.3V 5V 250Å	77K9RHA 1.8V/3.3V 5V 250Å oxide HVEE-NVM
			37 masks	47 masks
N/P MOS	1.8V	Nfet - Pfet	●	●
		Nfethvt - Pfethvt		●
	3.3V	Nfetox3 - Pfetox3	●	●
		Pfetox3hw	●	●
		Nfetox3de	●	●
		Nfetox3de_esd	●	●
		Nfetox3_ring	●	●
		Nfetox3de_ring	●	●
	5V	Nfetox5 - Pfetox5	●	●
		Nfetox5de - Pfetos5de	●	●
		Nfetox5de_esd Pfetox5de_esd	●	●
		Nfetox5_ring	●	●
		Nfetox5de_ring	●	●
	HV	nwhvfet		●
		nmvfet		●
		nmvafet		●
		nhvfet/phvfet		●
		nhvfet_ring		●
		phvafet		●
LDMOS	25V	ldnfet25 / ldpfet25		●
	45V	ldnfet45 / ldpfet45		●
BIPOLAR		pnp_vert_b	●	●
		lnpn	●	●

ATMX150RHA – PDK Devices Content

Device type	Domain	Device Name	77KRHA 1.8V/3.3V 5V 250Å	77K9RHA 1.8V/3.3V 5V 250Å HVEE-NVM
DIODE		dfreew_esd		●
		dfreew120_esd		●
		dz_6p2		●
		dz_6p2_esd		●
		nd3p3_esd	●	●
		schottky	●	●
CAPACITOR		cmim34	●	●
		Momcap – Moscap	●	●
		moscapox3	●	●
		Moscaphv	●	●
		P2bncap		●
RESISTOR		Rplow – Rphigh	●	●
		Rpolysh	●	●
		Rpolyhigh	●	●
		Rnsd - Rpsd	●	●
OTHER		Fuse	●	●
		hwc		●

- **PDK 2.8 delivered with**
  - Radiation Characterization report
  - Generic and Aerospace design rules
  - Generic and Hardened Pcell library with associated electrical models (Spectre, Hspice, Eldo)

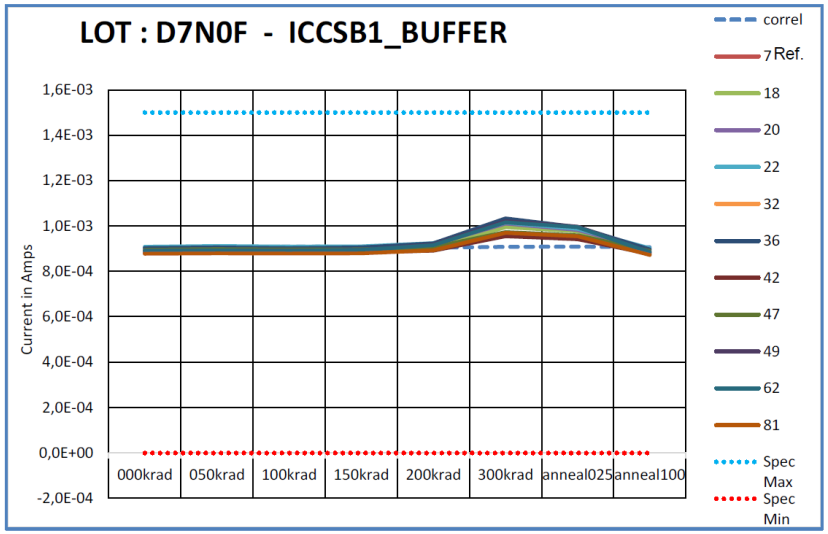
ATMX150RHA – Total Ionizing Dose

Tests in compliance with ESCC 22900 & MIL-Std 883 TM1019

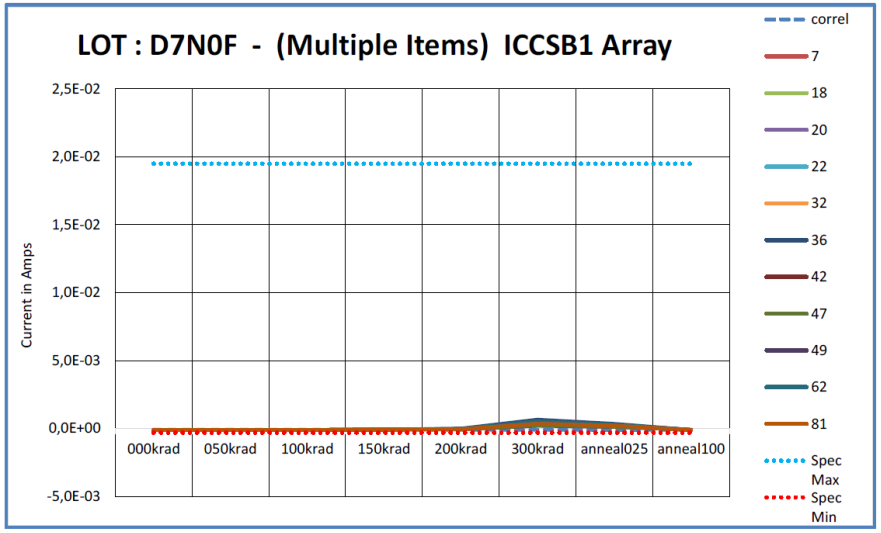
Total Ionizing Dose (TID) - Digital offer qualification

- **1.8V and 3.3V devices (Standard Evaluation Circuit - SEC)**
  - **Successfully tested up to 300krad(Si) with ELT * 3.3V devices**

3.3V IOs buffer Stand-by current vs cumulative dose
Specification=1.5E-3 A



1.8V Core Stand-by current vs cumulative dose
Specification = 2E-2 A



QML-RHA level R Qualified

up to 100 krad(Si) RHA

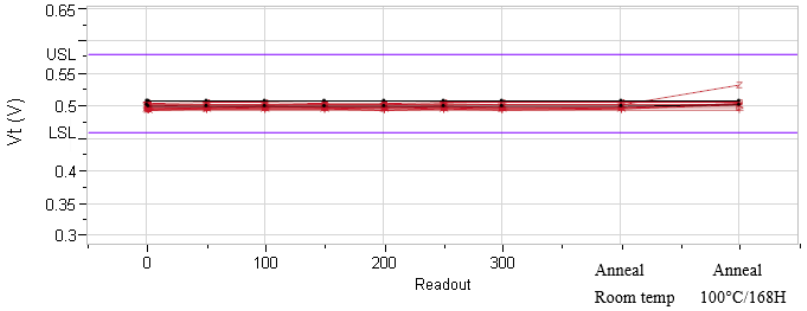
** ELT : Enclosed Layout Transistor*

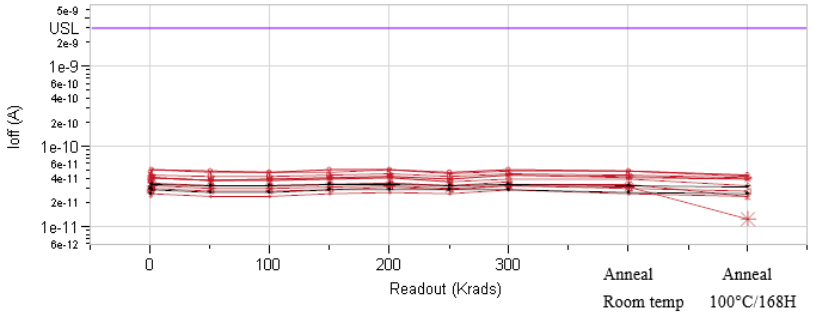
ATMX150RHA – Total Ionizing Dose

Tests in compliance with ESCC 22900 & MIL-Std 883 TM1019

Total Ionizing Dose (TID) - Digital offer qualification

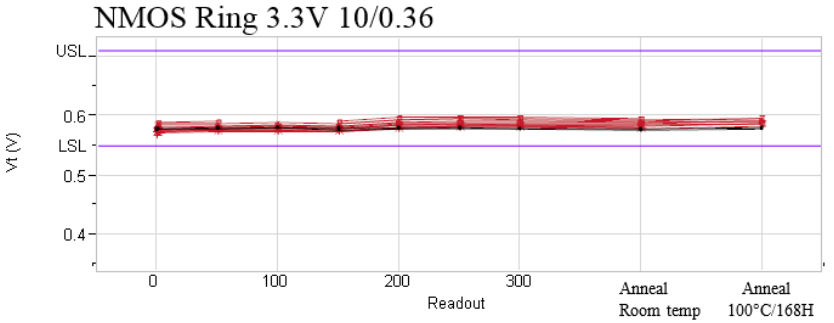
1.8V elementary devices - NMOS

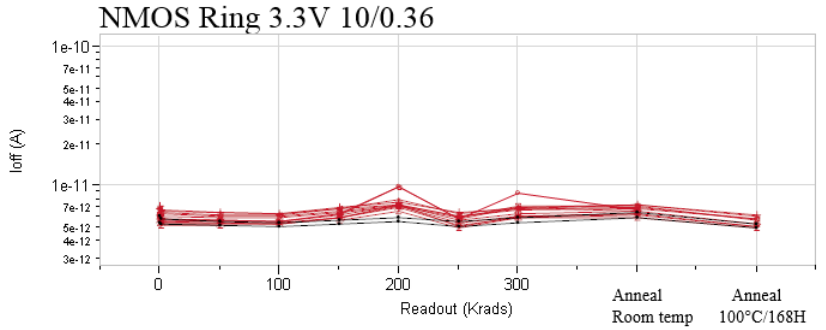




Threshold Voltage and Subthreshold current of NMOS 1.8V vs Cumulated Dose

3.3V elementary devices - NMOS





Threshold Voltage and Subthreshold current of NMOS 3.3V ELT vs Cumulated Dose

TID supply conditions

Devices	Drain	Source	Gate	Body	HWC	NB
NMOS	0V	0V	3.6V	0V	0V	0V

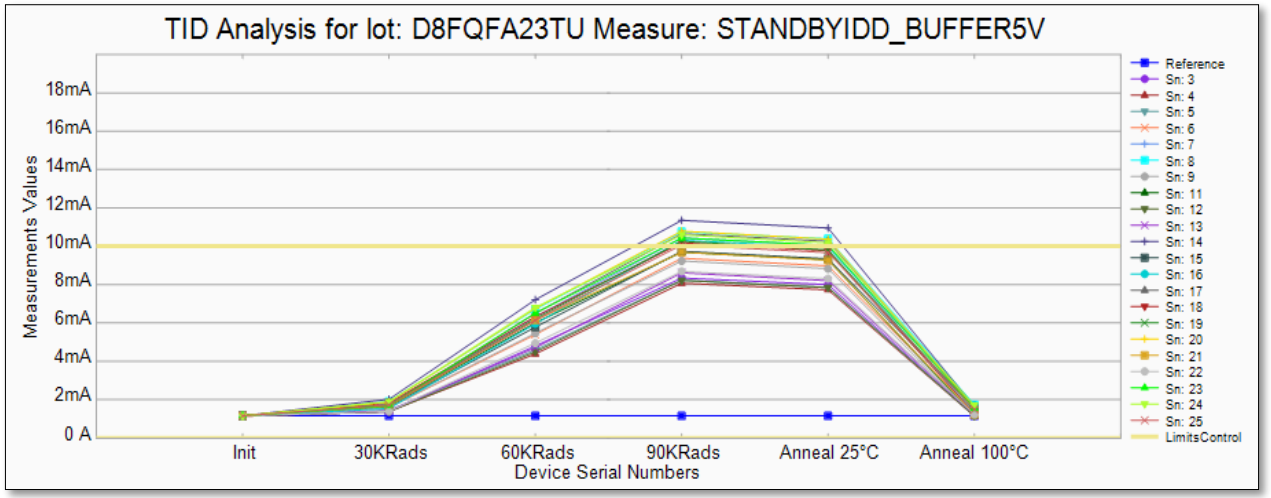
ATMX150RHA – Total Ionizing Dose

Tests in compliance with ESCC 22900 & MIL-Std 883 TM1019

Total Ionizing Dose (TID) - Digital offer qualification

- **5V devices (Standard Evaluation Circuit - SEC) : IO5V**
  - **TID sensitivity increased due to 250 Å oxide (same as HV devices)**
  - **Successfully tested up to 60 krad(Si) with ELT* layout**

5V IOs buffer Stand-by current vs cumulative dose
Specification=10 mA



QML-RHA level P

up to 30 krad(Si) RHA

** ELT : Enclosed Layout Transistor*

ATMX150RHA – Single Events

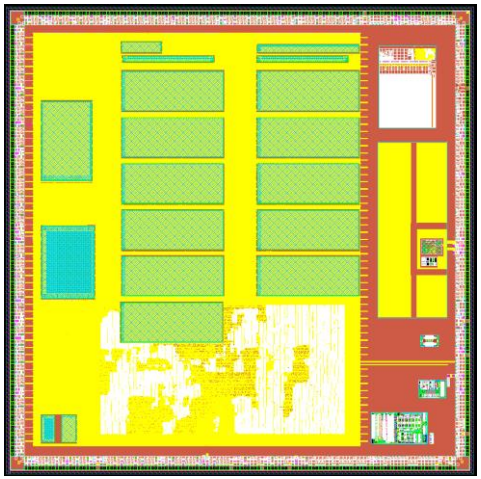
Tests in compliance with ESCC 25100 & MIL-Std 883 TM 1020

Single Event Effects

Digital offer qualification

- **Single Event Latch-up @ Vcc_{max}, 125°C**
  - **Full SEL Immunity by Deep trench**
  - **Dual Deep Well solution for high integration**

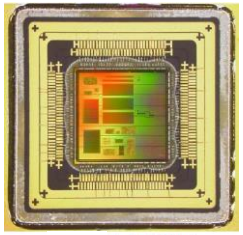
    → **SEL LET_{th}> 78MeV.cm²/mg**



Standard Evaluation Circuit of ATMX150RHA

ATMX150RHA – Single Event Upset

Tests in compliance with ESCC 25100 & MIL-Std 883 TM 1020



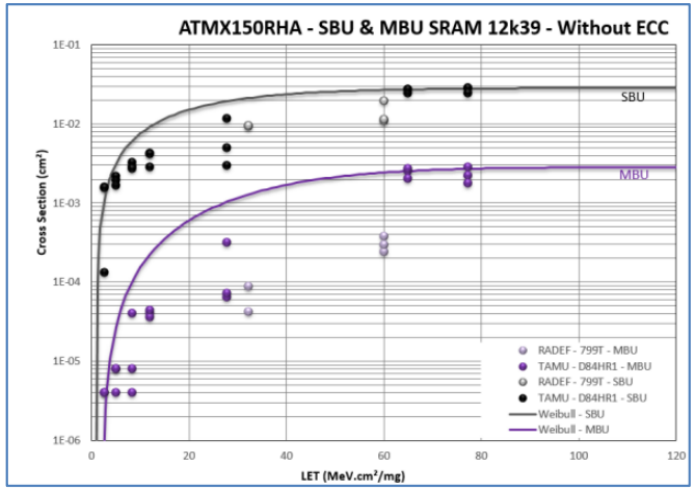
Device delidded

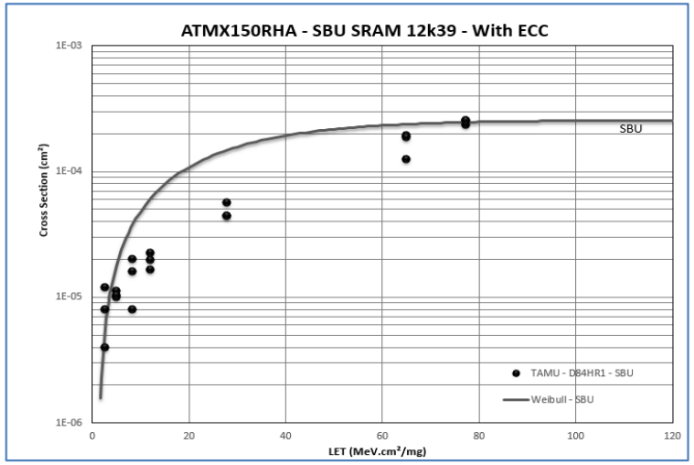
Single Events Upset (SEU): RAM Virage compiler

MBU/SEU Hardening by Scrambling and ECC

Memory type	LET threshold (MeV.cm²/mg)	SEU Xs (cm²/dev)	Weibull param. W	Weibull param. S
SRAM16k32	1	$3.61E^{-2}$	24	1.2
SRAM12k39	1	$2.85E^{-2}$	24	1.2
DPRAM6k39	1	$1.95E^{-2}$	22	1.0
DPRAM2k8	1	$1.15E^{-3}$	25	0.9
TPRAM 1k16	1	$5.55E^{-4}$	30	0.8
SRAM12k39 with ECC	1	$2.56E^{-4}$	30	1.3
DPRAM6k39 with ECC	3.3	$1.30E^{-5}$	28	1.2
Memory type	**LET threshold (MeV.cm²/mg)**	**MBU Xs (cm²/dev)**	**Weibull param. W**	**Weibull param. S**
SRAM16k32	2	$1.74E^{-3}$	40	1.8
SRAM12k39	2	$2.84E^{-3}$	40	1.8
DPRAM6k39	2	$2.43E^{-3}$	34	1.4

Summary of the SBU/MBU Weibull parameters (LET_{th}, cross section, W & S) for main RAMs Virage

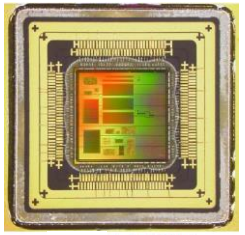




SBU/MBU cross section vs LET -12k39mux16 SRAM with/without ECC

ATMX150RHA – Single Event Upset

Tests in compliance with ESCC 25100 & MIL-Std 883 TM 1020



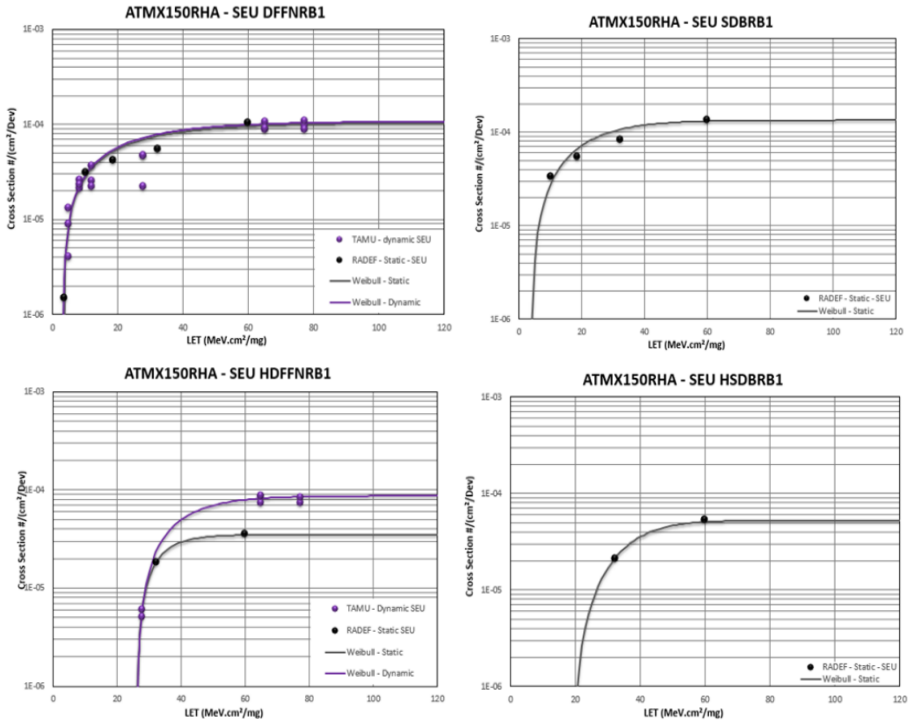
Device delidded

Single Events Upset (SEU): Register files

HDFF LET > 26 MeV.cm²/mg

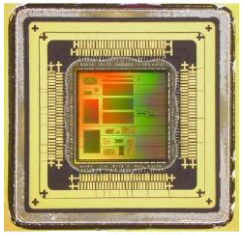
Memory type	LET threshold (MeV.cm²/mg)	SEU Xs (cm²/dev)	Weibull param.	
			W	S
DFFNRB1	3.0	$1.08E^{-4}$	22	1.0
DFFNRB2	3.6	$1.14E^{-4}$	22	1.0
SEU hard. DFFNRB1	26	$8.70E^{-5}$	16	1.2
SEU hard. DFFNRB2	26	$1.06E^{-4}$	16	1.2
Scan Std DFF SDBRB1	3.6	$1.34E^{-4}$	20	1.3
Scan Std DFF SDBRB2	3.6	$1.06E^{-4}$	20	1.1
Scan SEU hard. DFF SDBRB1	18.5	$5.25E^{-5}$	20	1.7
Scan SEU hard. DFF SDBRB2	18.5	$4.00E^{-5}$	22	1.7

Summary of the SBU/MBU Weibull parameters (LET_{th}, cross section, W & S) for main Register Files



SEU cross sections of shift registers in cm²/device a device is a chain of 1024 DFF

ATMX150RHA – SER synthesis


Device delidded

RAM Virage compiler

SRAM - GEO mission profile		MTBF		
	SER (/dev/day)	Device (day)	Word (year)	bit (year)
SEU 16k x 32	4.59E-01	2.18	98	3129
SEU 12k x 39	3.47E-01	2.88	97	3784
SEU 12k x 39 w ECC	6.99E-04	1431	48163	1878347
MBU 16k x 32	1.16E-03	862	38696	
MBU 12k x 39	2.06E-03	485	16343	

DPRAM - GEO mission profile		MTBF		
	SER (/dev/day)	Device (day)	Word (year)	bit (year)
SEU 6k x 39	4.22E-01	2.37	40	1556
SEU 2k x 8	2.64E-02	37.88	213	1700
SEU 6k x 39 w ECC	2.27E-05	44053	741536	28919920

Environmental Conditions

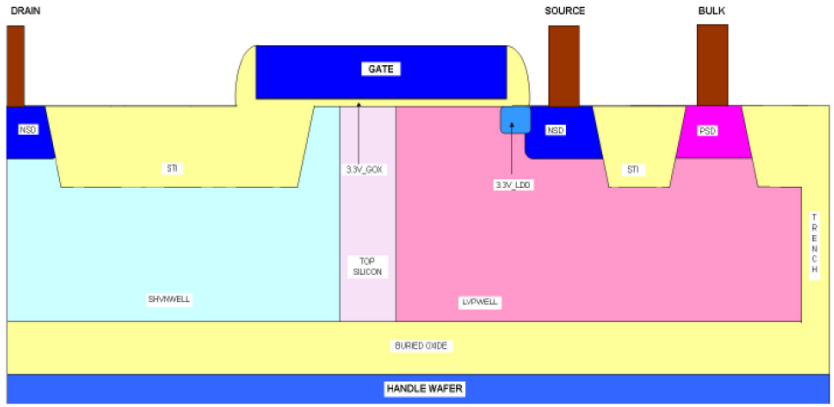
using OMERE
Solar Min
Z=1 to 92
Aluminum shielding of 1g/cm^2

DFF

DFF - GEO mission profile		MTBF
	SER (/DFF/day)	Device (year)
DFF drive 1	7.81E-07	3508
Scan DFF drive 1	6.40E-07	4281
Hardened DFF D1	3.75E-09	730594
Hardened Scan DFF D1	2.50E-09	1095890

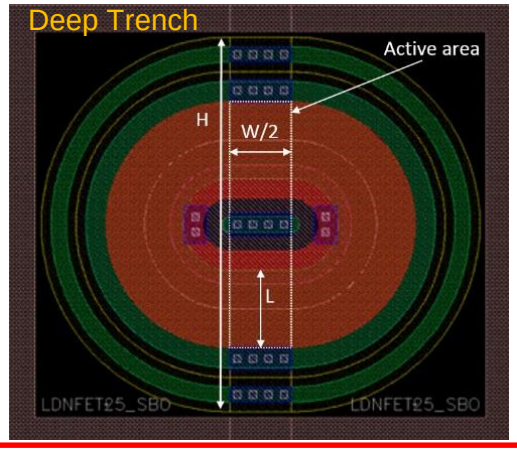
LDMOS Characterization

high voltage lateraly diffused LDMOS



LDNMOS 25V with SBO configuration schematic cross section

- **3.3V Gate oxide**
  - Enables to pass up to 45V on Drain
  - Long diffused Drain to increase R_{ON}
  - Ring layout enclosed by Deep Trench : Full SEL immunity



ATMX150RHA – LDMOS 25 & 45V

Cumulated Dose on LDMOS

- **Supply conditions during irradiation**

Devices	H (µm)	Drain	Source	Gate	Body	HWC	NB	Read outs krad(Si)
LDNMOS	10.76	0V	0V	3.6V	0V	0V	0V	30, 60, 90
LDPMOS	10.36	0V	25V	25V	25V	0V	0V	30, 60, 90

Devices	H (µm)	Drain	Source	Gate	Body	HWC	NB	Read outs krad(Si)
LDNMOS	12.76	0	0	3.6V	0	0V	0V	30, 60, 90
LDPMOS	13.56	0V	45V	45V	45V	0V	0V	30, 60, 90

- **No drift up to 90krad(Si)**
  - **Threshold voltage (Vt)**
  - **Saturation current (I_{ON})**
  - **Subthreshold leakage current (I_{OFF})**
- **Drift with dose on Drain/Source On resistance (Rds_{ON})**
- **No gate rupture**
- **Post radiation model @30krad(Si) for LDMOS 25V & 45V**

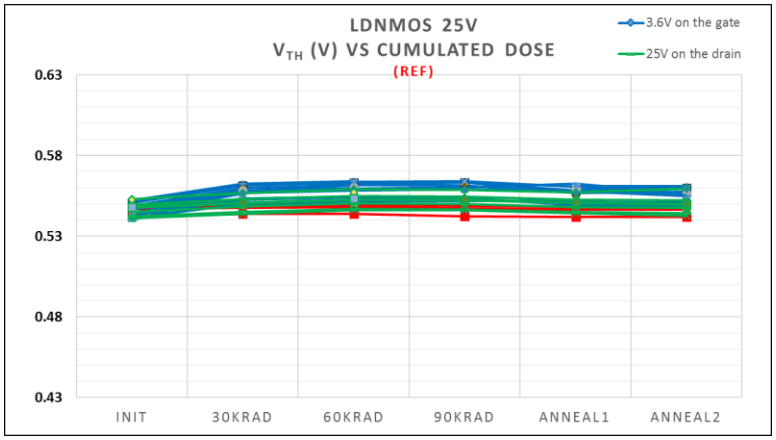
ATMX150RHA – LDMOS 25V

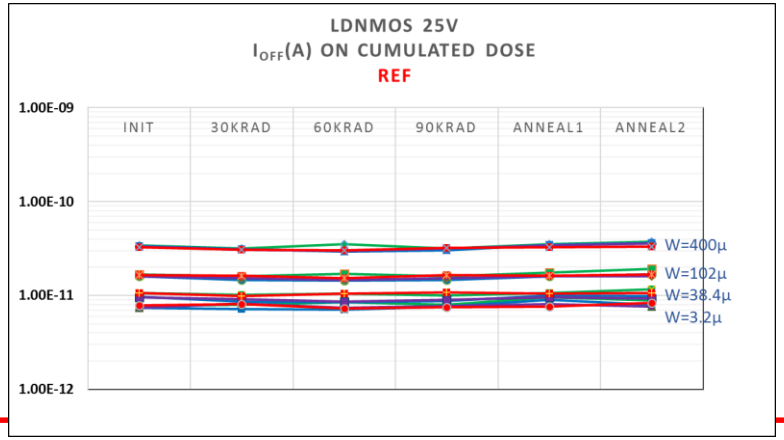
LD NMOS 25V on cumulated dose

- LDMOS 25V & 45V Evaluation
  - Threshold voltage (Vt)
  - Subthreshold current (I_{OFF})

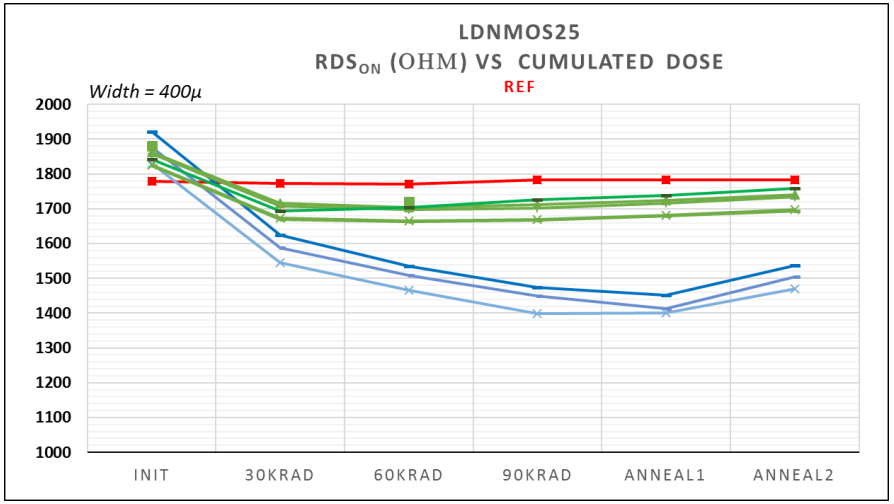
Radiation electrical model

@ 30krad(Si) RHA



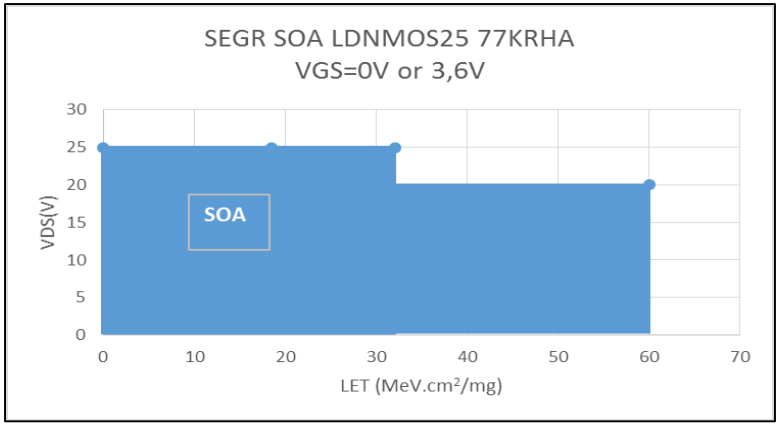


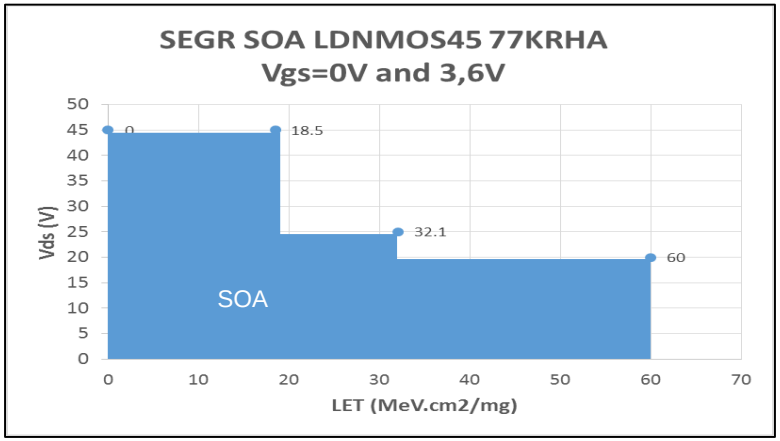
- On Resistance (RDS_{ON})
  - Major drift managed by Gate supply



ATMX150RHA – LDMOS 25 & 45V

- **Single Event Burnout (SEB) & Single Event Gate Rupture (SEGR) on LDMOS**
  - **SEL immune by Deep Trench**
  - **SEB**
    - No SEB encountered up to 60 MeV.cm²/mg at Vcc_{max}, 25°C, 1E7#/cm²
  - **SEGR LDPMOS:**
    - No SEGR up to a LET of 60MeV.cm²/mg at Vcc_{max}, 25°C, 1E7#/cm²
  - **SEGR LDNMOS**
    - No SEGR up to a LET of 60MeV.cm²/mg @ VGSmax and VDS=0V (25°C, 1E7#/cm²)
    - SEGR encountered when drain supply: Safe Operating Area (SOA) (25°C, 1E7#/cm²)





ATMX150RHA – Conclusion

- **Further Works**
  - **Cumulated dose Characterization**
    - HV devices (15V oxide)
    - Capacitors
    - Bipolar transistors

  → **Associated electrical model after TID**

  → **PDK delivery**

  - **SEB / SEGR Characterization**
    - HV devices (15V oxide)
    - Capacitors
    - Bipolar transistors

  → **Associated Radiative SOA**

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