The Design Against Radiation Effects (DARE) design platform for TSMC 65nm process.

M. Kakoulin[a)], S. Redant[a)], G. Thys[a)], S. Verhaegen[a)], G. Franciscatto[a)], B. Chehab[a)], G. Pollissard[a)], L. Berti[a)]

[a]imec, 3001 Leuven, Belgium

michael.kakoulin@imec.be

Abstract

DARE65T is a new radiation hardened (RH) high-performance system-on-a-chip (SoC) design platform including mixed-signal and analogue building blocks. It is built on the commercial TSMC 65nm LP 1.2V/2.5V CMOS technology. The DARE65T incorporates a set of standard and IO cell libraries, LVDS and SSTL cell libraries, memory and analogue IPs. The DARE65T development is based on common radiation design rules, which are implemented in an analog design kit (ADK). This approach facilitates also full custom radiation aware analogue design. DARE65T meats the main performance requirements of Space equipment designers.

The DARE65T platform provides SEE hardening capabilities among with low-power consumption and high density features. The used mitigation methods guarantee TID tolerance higher than 100 krad as well as SEL hardening for LET values higher than 60 MeV/cm2.mg.

The paper is focusing on radiation effects (TID, SEL, SEU, SET) mitigation methods and details the development of the DARE65T library, provides its features and first results.

I. Introduction.

In the last decades the evolution of the technologies for space ASIC and chip production is bringing a high level of miniaturization, giving benefits in terms of less power consumption, less mass, less volume, reduced number of components on the boards, better testability, higher performances and reliability. Newest space technologies (optical and RF communications) as well as miniature CubeSats and communication satellites are demanding more and more performance from electronic components. At the same time, satellites' reliability and lifetime requirements are still requesting for TID and SEE radiation hardness. Space System Designers are always looking for the best integration, area, power, performance, mass, volume, radiation hardness and cost tradeoffs. Hence, there is always a demand to go for not only nodes with more capabilities, but also to more advanced nodes, for they bring new capabilities to the playing field. As the lead time to access new technologies for the development of ASICs for Space applications is several years, and the long-term availability is limited by the technology lifetime, it is important to give system designers for Space applications access to these technologies as early as possible.

The new RH high-performance DARE65T platform is developed to meet those demands. It is built on the commercial TSMC 65nm LP 1.2V/2.5V CMOS technology. Thus it provides two kinds of core libraries: high speed and low-leakage. It has also a list of analogue blocks and SRAM memory solution to help building complex mixed-signal RH ASICs. As it was mentioned the Space designs are demanding more and more performance. The ASIC performance means not just a clock frequency, but also high-speed interfaces. Among classical requirements for LVDS IO cells in order to build SpaceWire interface links, there are new requests for DDR interface and high-performance link, for example, RapidIO or PCIe or JESD204. DARE65T platform supports such needs providing set of LVDS and SSTL IO cells. The relevant section of the paper gives detailed overview of such platform capability.

II. DARE65T mitigation methods.

In order to provide a cost-effective solution for low-volume radiation-hardened applications, a commercial foundry process is used for DARE libraries. Although no process tuning is available in such processes, the features already provided by the technology can be used for efficient mitigation of radiation effects. Thus commercial TSMC technology was selected for new platform: 65nm LP 1.2V/2.5V CMOS technology. This process has triple-well availability. Triple wells have been used for better SEU performance and SEL immunity.

The first significant step is to define the design platform basis concerning radiation effects (TID, SEL, SEU, SET) mitigation methods.

A. TID hardness.

The most interesting TID measurement results for TSMC 65 nm process have been found in [1] and are shown here below.

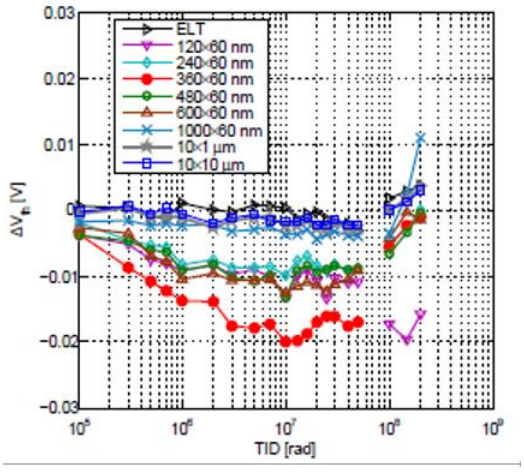

Figure 1: Threshold voltage shift measured for NMOS core (RVt) devices [1]

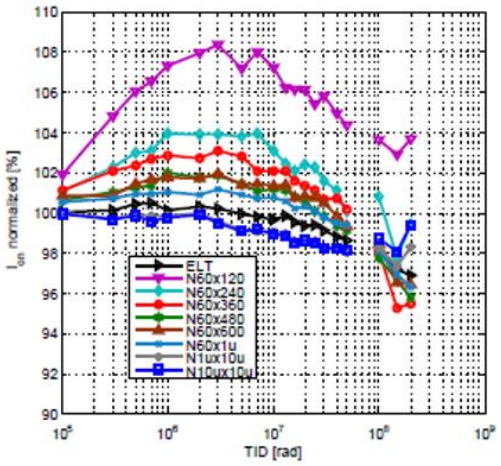

Figure 2: Max. drive current (Vgs=Vds=1.2V) measured for NMOS core (RVt) devices, normalized to pre-rad [1]

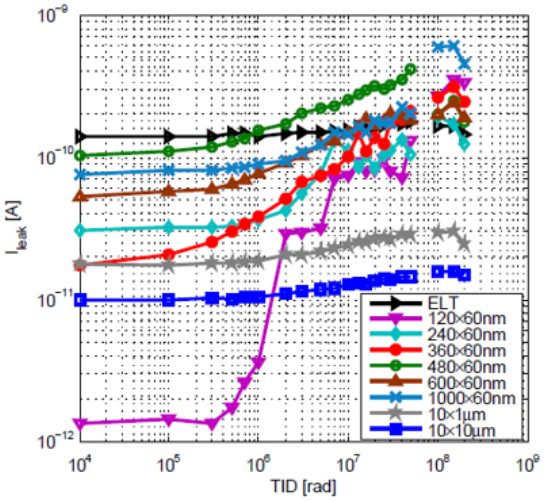

Figure 1: Leakage current measured for NMOS core (RVt) devices. **Error! Reference source not found.**]

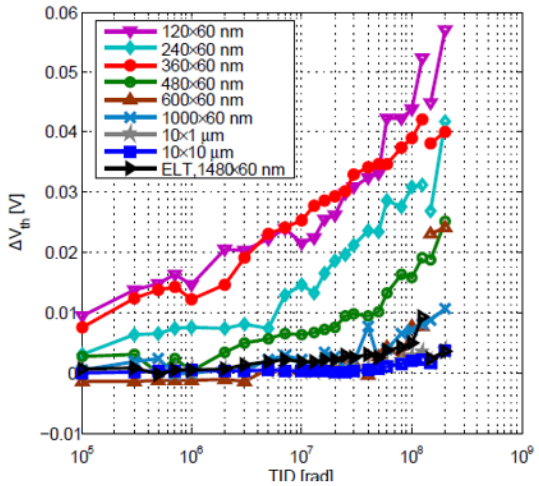

Figure 4: threshold voltage shift measured for PMOS core (RVt) devices [1]

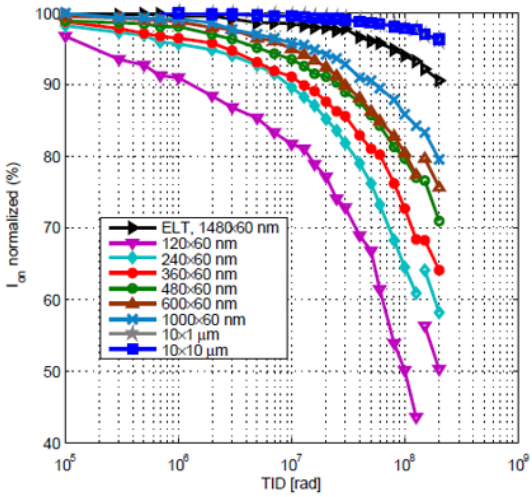

Figure 5: Max. drive current (Vgs=Vds=1.2V) measured for PMOS core (RVt) devices, normalized to pre-rad [1]

From the results shown on Figures above it appears that ELT transistors as TID mitigation method might be replaced with a normal transistors with the limits of the minimum core NMOS and PMOS transistors width. The 2 limitations might be set one is for digital designs and another one (larger W) for analogue designs.

The paper [1] provides also the TID behaviour of IO (2,5V) transistors (PMOS and NMOS). Similar conclusion is made for TID mitigation method for IO transistors.

For the DARE65T library with basic TID requirement of 100krad a minimal specification of core & IO transistors width could be enough to reach the needed TID hardness.

B. SEL hardness.

An n+ diffusion area in the p-substrate next to a p+ diffusion area in n-well forms a parasitic thyristor. Technologies are normally conceived so that parasitic thyristors do not impact circuit performance. Charged particles generated by heavy ion strikes may fire a parasitic thyristor and induce the circuit to go in latch-up. Another paper [2] provides good radiation experimental SEL results of 65nm semiconductor structures with and without guard rings. The experiments were made on 4 different RAM cells:

- "6T" is standard high density block with 6-transistor (6T) cell without any solutions for SEL prevention.
- "6T_GR" is based on 6T cell with N+ and P+ guard rings.
- "DICE_GR" block has solid guard rings
- "DICE" block has intermittent rings

No SEL is found at room temperature in all SRAM blocks at effective LET 60 MeVxcm^2/mg. The SEL occurs in "6T" block only at effective LET 60 MeVxcm2/mg and at elevated temperature.

This effect will be mitigated by introducing guard rings connected to supply or ground voltages. Both n+ and p+ guard rings will be employed in DARE65 libraries. P+ guard rings are also used for mitigating TID induced leakage. Over time, positive charges that are trapped in the STI oxides may shift the threshold voltages of parasitic NMOS field

transistors formed between two n-type regions (n+/n+, n-well/n-well, or n+/n-well). This effect can be mitigated with p+ guard rings in between n-type regions [3].

Additional SEL mitigation method which will be used is a minimum double contact requirements in source/drain areas of transistors.

The article [2] makes also interesting note that not only solid guard rings help to significantly enlarge the threshold LET for the latch-up effect, but also there is no SEL in the block with intermittent guard rings, too. That result will be used for SRAM memory implementation.

C. SEU behaviour.

The paper [2] gives also good description of SRAM structures SEU cross-section. The experiments were made on 4 different RAM cells, described in II.b. Fig. 6 [2] shows SEU cross-section LET dependence for the SRAM blocks. Note that error cross-sections, not event cross-sections, are shown here. One can see from Fig. 6 that high-LET cross-section values for "DICE" and "DICE_GR" are about 3 orders of magnitude lower than cross-sections for "6T" and "6T_GR".

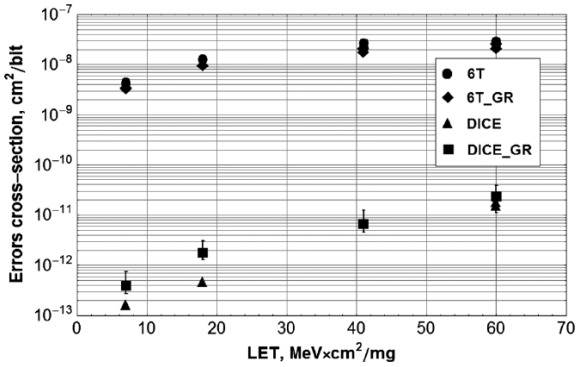

Figure 6: SEU cross-section LET dependence for SRAM blocks in 65 nm [2].

The list of SEU/SET mitigation methods used in DARE65T is provided below:

- Device spacing – to avoid "double hits"
- No Hot MOS (i.e. MOS where the bulk is respectively not connected to GND and VDD).
- Drive Strength Hardening – especially to create SET hardened standard cells.
- SET filters
- DICE FF
- Bit alignment in SRAM blocks – to avoid MBU

III. DARE65T LIBRARIES

As it was mentioned DARE65T is mixed-signal microelectronics platform that will deliver digital libraries, standard and high-speed IO cells, analogue IP and memory blocks suitable for radiation hardened applications.

The DARE65T operating conditions:

Temperature range: minus 55 – plus 125 ^{0}C;

Core supply voltage: 1.2 V ± 10%;

IO supply voltage: 1.8, 2.5, 3.3V ± 10%.

A. DARE65T_ADK

The DARE65T_ADK is radiation hardened extensions of the standard TSMC TS65LP foundry PDK. ADK incorporates and provides automatic checks of all chosen design rules, designers must follow in order to create RH ASICs. The DARE65T_ADK is integrated in Virtuoso (Cadence). ADK consists of 3 main parts:

- Schematic checks
- Layout checks
- SET simulation environment

Schematic and layout checks provide the automatic verification of RH design rules and radiation effects mitigation methods listed in section II. Thus schematic checks provides errors [4] when

- minimal specification of the core transistors width is violated;
- minimal specification of the IO transistors width is violated;
- NMOS transistor bulk net is found;
- Hot NMOS or PMOS is found.

The schematic checks has also several warning. For example, when transistor model without matching is used or unwanted device was placed in the schematic (DARE65 platform has a restriction for device usage).

Layout checks based on Calibre deck highlights the RH design rules violations [4], for example

- Poly crossing NTAP or PTAP
- N-Well regions on different net not separated by P+ guard ring
- N+ Active region(s) with leaky path to N-Well
- P-Well regions not separated by N+ diffusion guard-ring
- etc.

Another important point when doing radiation hardening by design for mixed-signal and analog blocks is simulation of SET events. ADK also provides the environment for such simulations. It is needed to find the SET sensitive nodes in a design and then adapt the design to bring the SET hardness in compliance with the specification. In order for an analog designer to do this efficiently the tools used are integrated in the normal analog design flow [5]. The SET simulation environment consists of several elements[5]:

- SET striker (Verilog-A) – it allows to perform single SET injection during simulation.
- Deepprobe – it removes the need to adapt the design of the DUT for SET simulations.
- Periodic SET striker – it generates events with a specified period and allows to replace all SET strikers with one in a schema.

The article [5] provides detailed description of DARE65T SET simulation environment.

B. DARE65T_CORE library

The digital core library comprises numerous combinational cells, SET-hardened cells, non-hardened and SEU-hardened sequential cells. The library is designed to offer good SEL hardening in a very compact standard cell template. General library figures are listed in Table 1.

Table 1: DARE65T core library figures

Parameter	Value
Number of cells	102
Raw gate density	344 kGates/mm^2
The pitch	0.2 µm
Cell height	12 tracks
Multi Vt support	SVt, HVt, LVt

The DARE65T_CORE library has similar performance to commercial TSMC 65nm LP 9 T library with moderate area increase. For example DARE65 NAND2 cell has similar timing performance and it is 1,5 larger then commercial 9T cell. The EXORD1 cell has similar performance and area figures. DARE65 standard cell library has SEL & TID only hardened FF which are 2 times only bigger then commercial counter pair and SEL&SEU&TID hardened DICE flipflops. DICE FF is implemented with respect to device spacing and thus 2,5 times larger than non SEU hardened FF (with the same performance). The figure 7 provides the visual comparison between DICE and usual FF of DARE65T_CORE lib.

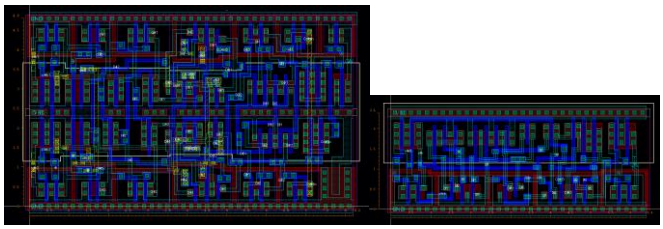

Figure 7: DARE65T_CORE DICE and std FF.

The DARE65T libraries supports all 3 Vt flavours (SVt, LVt, HVt) similar to commercial libraries. There will be 2 kind of standard cell libraries optimized by transistors geometry available:

- Low power consumption (mainly leakage)
- High performance.

Table 2 lists all types of DARE65T_CORE cells.

Table 2: DARE65T_CORE cell types

Type	N
Non-SET hardened combinational cells	52
SET hardened combinational cells - 25 MeVxcm^2/mg	7[1)]
SET hardened combinational cells - 40 MeVxcm^2/mg	7[1)]
SET hardened combinational cells - 60 MeVxcm^2/mg	7[1)]
Non-SET hardened sequential cells	9
SEU hardened sequential cells [2)]	5
ANTENNA cells	1
TIEH and TIEL	2
Non-SEU hardened clock gating cells	1
SEU hardened clock gating cells	3
Filler cells	8

Note: 1) – including SET hardened TMR voter cell
2) – SEU hardened cells has min LETh 60 MeVxcm^2/mg

C. DARE65T_SRAM

DARE65T design platform offers single port SRAM (SPRAM) and dual port SRAM (DPRAM) solutions. The DARE65T_SRAM library is based on custom TID and SEL hardened SRAM cell it is optimized for area and power consumption.

The memory blocks are designed to be insensitive to multi-bit upsets (MBU). This is achieved by arranging the bits of a same word far enough from each other. In this case every two bits of a same word are separated by 16 bits which corresponds to an interleaving distance higher than 15 µm. This way an error detection and correction circuit (EDAC) can be used to mitigate soft errors due to single-bit upsets (SBU).

The SPRAM cell area is 1,9 x 1,85 um^2. As it can be seen on Figure 8 the SPRAM memory cell has closed guard ring around nmos transistors in order to mitigate SEL & TID effects. Based on the experimental results mentioned in section II.B the intermittent guard ring might be used. It will allow to increase the memory density in 1,5 times. The impact on SEL and TID hardness should be acceptable. The HD SRAM memory cell will be introduced based on test vehicle radiation test results.

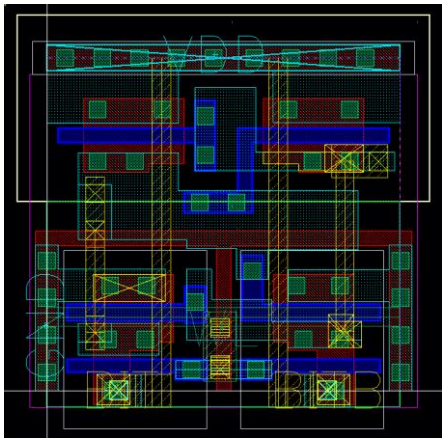

Figure 8: DARE65T SPRAM memory cell.

The DARE65T DPRAM cell area is 1,9 x 2,75 um2.

D. DARE65T_IO

The I/O library includes several digital and analog pad limited I/O cells. As in the core library, all I/O cells are hardened against SEL effects. Digital input I/O cells are also hardened against SET to prevent events from propagating to the core logic. The digital IO cells have the following features:

- cold spare
- slew-rate control
- programmable pullup, pulldown.

An extensive list of tri-state output, bidirectional bidirectional I/O cells with different driving capabilities is available. Power and ground I/O cells as well as breaker cells are available for the definition of multiple I/O power domains.

The DARE65T_IO library is based on 2,5V transistors with overdrive to 3,3 V. It is designed and optimized to work at different supply voltages: 3,3V, 2,5V and 1,8V.

E. DARE65T_SSTL & LVDS

As it was mentioned in the introduction there is great demand on high-speed interfaces. So among standard LVDS IO cells DARE65T platform will offer SSTL IO cells for 1,8V and 1,5V power supply (DDR2 and DDR3 respectively).

The DARE65T_SSTL library contains the following abutable cells, which once assembled, constitute an SSTL ring segment:

- SSTL_VREF - SSTL reference cell
- SSTL_RX_SE - SSTL single-ended receiver
- SSTL_RX_DIFF - SSTL differential receiver
- SSTL15_RXTX_SE - SSTL15 single-ended transceiver
- SSTL15_RXTX_DIFF - SSTL15 differential transceiver
- SSTL15_ZQ - SSTL15 ZQ auto-calibration cell
- SSTL18_RXTX_SE - SSTL18 single-ended transceiver
- SSTL18_RXTX_DIFF - SSTL18 differential transceiver
- SSTL18_ZQ - SSTL18 ZQ calibration cell
- SSTL_VDD1V2 - Core power supply
- SSTL_VSS1V2 - Core ground
- SSTL_VDD1V8 - IO power supply (1,5 and 1,8V)
- SSTL_VSS1V8 - IO ground
- SSTL_POC - Power-on control cell
- SSTL15_DLL – DLL cell

The cells are implemented with respect to the JEDEC standards JESD79-2F (DDR2/SSTL18) and JESD79-3F (DDR3/SSTL15). The target data rate is 800 Mbps.

DARE65T_LVDS library will have transmitter and receiver cells both made on 2,5 V overdrive 3,3 transistors. It will allow them to operate at 2,5 and 3,3 V voltage supply with up to 400 Mbps (200 MHz) data rate.

F. DARE65T first analogue blocks.

As mixed signal design platform DARE65 offers foundation rad hardened analogue IPs. Table 3 lists the analog blocks which will be available on early stage.

Table 3. DARE65T first RH analogue IP.

Analog IP	Main features
DARE65T_PLL	200-1200 MHz output frequency 2,5-32 MHz reference frequency Supply voltage 1,2V.
DARE65_IVREF	1,2V and 2,5 supply voltages 0,6V output reference voltage Reference current output Accuracy (before trimming) ± 2,5 %
DARE65_ADC	10 bit resolution Integrated temperature sensor 10 kHz sampling rate. Supply voltage 1,2V.
DARE65_POR	TBD

IV. Further Work

The next step of DARE65 development is test vehicle design. The test vehicle will include all the platform elements. The electrical and radiation tests of test vehicle will proof the DARE65T design platform concept and solutions.

The further development of mixed signal RH DARE65 design platform is significant point to make it suitable for any high-performance space applications. The next development steps could be:

- RH NVM memory solution (antifuse or similar)
- RH high speed links (for example RapidIO, PCIe, JESD204 multistandard SerDes)
- DDR2 and DDR3 PHY and controller
- High-performance ADC and DAC

V. Summary

This paper introduced the development of a new radiation hardened library platform for mixed-signal space applications. A set of libraries including numerous core cells, I/O pads, SRAM blocks and analog circuits is being developed and will offer a complete solution for high-performance applications that require TID tolerance 100-300 krad.

DARE65 libraries are reliable design platform for competitive high-performance radiation hardened ASICs.

VI. References

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VII. ACKNOWLEDGEMENTS

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