Characterization, Screening and Qualification of the MEDA Wind-Sensor ASIC

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Abstract

This paper describes the final characterization results of the MEDA-WS ASIC, which was described in a previous paper in AMICSA-2016. It describes as well the qualification and the screening processes that have been carried out prior to its integration in the final flying modules of the wind-sensor instrument.

I. INTRODUCTION

The paper describes the final steps of characterization, screening and qualification of the MEDA Wind-Sensor ASIC. This ASIC, whose design and preliminary functional measurements were already reported in AMICSA-2016 [1], is a key component of the wind-sensor included in the MEDA instruments set for the upcoming Mars-2020 mission [2].

In the present days, the ASIC has been fully characterized and has gone through a detailed qualification process. Samples have been screened and a selection has been made for the flight modules. The final integration in the instrument printed circuit board (PCB) and the final instrument calibration procedures are underway.

II. THE MEDA WIND-SENSOR ASIC

The MEDA Wind-Sensor (WS) ASIC is a mixed signal ASIC designed in a standard 0.35µm CMOS process [3]. This CMOS process had been previously characterized by the authors from IMSE with respect to radiation effects and low temperatures [4], [5], including the assessment and evaluation of typical radiation hardening by design (RHBD) techniques like the use of enclosed layout transistors (ELT) and the use of ward-rings around individual n-mos and p-mos sections. A rad-hard digital cells library and several other previous mixed-signal ASICs have also been designed by the authors from IMSE in the same process [6], [7], [8], [9] as part of a long term effort in the field of space microelectronics initially and mainly promoted by the Payloads Electronic Engineering Laboratory of INTA [10].

The functionality of the MEDA-WS-ASIC together with a description of its circuitry, some design details, and preliminary functional test results were already reported in AMICSA-2016 [1] and will not be detailed again. Essentially, it is that of an analogue front-end for sensor signal acquisition and AD conversion, with a number of multiplexed input channels, and a number of temperature-controlling feedback loops which provide and measure the heat power required to hold the temperatures constant. A digital section is in charge of tasks control and communications with the instruments control unit (ICU). Figure 1: shows a photograph of the MEDA wind sensor die.

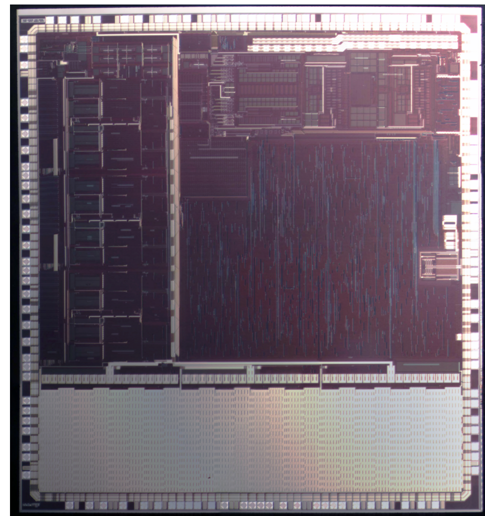

Figure 1: Photograph of the MEDA wind sensor ASIC die.

The wind sensor concept is based on previous work by Universidad Politécnica de Cataluña [11], [12]. The digital control and communication finite state machine (FSM) of the ASIC was designed at high level by CRISA [13]. CRISA was also in charge of the quality assurance control during the design of the ASIC. The design of the full-custom analogue circuitry, as well as the synthesis and back-end of the digital sections was carried out by IMSE. The development of the MEDA instruments set is being coordinated by Centro de Astrobiología (CAB) [14]. Finally, the screening and qualification processes have been defined and carried out by ALTER [15] with measurement set-ups designed by IMSE.

At the time of describing it for AMICSA-2016 [1], the ASIC samples had been received and some preliminary functional tests had been carried out, showing that it was operative and functional. This paper focuses on the works carried out from there on, in particular, on the final characterization results, final packaging, on the screening and qualification processes, and on the integration in the instrument electronics.

III. Characterization results

The ASIC has been found to be functional in every aspect, within a temperature range that goes from -128ºC to +50ºC. The digital control, the command execution, and the communication circuitry are operative, as well as the power-on-reset (POR) circuit, in the whole temperature range. The 16-bits ADC conversion channel, including the instrumentation amplifier and the ADC, has an equivalent input r.m.s noise in the range of 3 V_{LSBs} and a similar integral nonlinearity (INL). Its behaviour is not affected by temperature, apart from the obvious effect of the variations of the reference voltage. The input multiplexer does not affect the measurements, as expected: all channels have the same static transfer characteristic.

The voltage and current references behave as expected as well. The non-calibrated Vref values dispersion among different samples, at nominal temperature, is in the range of ±10mV. This can be calibrated and therefore reduced to values in the range of ±1mV. In any case, the relevant figure is the variation of Vref with temperature. After calibration, the variation within a temperature range of -135 to 50ºC is about ±3mV. Similar variations are observed in the reference current Iref, with a high correlation between Vref and Iref values among samples and temperature.

The several current sources present in the chip for biasing and heating behave as expected, with actual values very close to their nominal values and with the expected programming ranges. Again, the relevant figures are the dispersion among identical sources in a chip sample, among chip samples, and with temperature. As an overall figure, both dispersion at a given temperature and variations within the temperature range of -135 to 50ºC are in the range of 0.4% or lower. Effects of Vref variation are not accounted in that figure.

Concerning the thermal feedback loops, the auto-zeroed comparators have a residual offset of about 0.1Mv. The DACs used to set the prescribed temperatures of the hot dies have an INL in the range of 1 V_{LSB}. The feedback loops are stable and behave correctly, maintaining the temperatures of the hot dies at the prescribed temperature, and providing the count of heating current pulses applied to each die.

Finally, auxiliary blocks like the over-temperature alarms for the external dies and for the ASIC itself behave as expected as well. The same can be said concerning the proportional-to-absolute-temperature (PTAT) circuit used to monitor the ASIC temperature, and the resistive divider (VDD/3) used to monitor the power supply voltage. The internal reference calibration levels have their expected values and dispersions, and the RS-422 driver circuitry is slew-rate limited to about 1V/ms as required.

Summarizing, the ASIC fulfils the specified functionality and the required accuracy and temperature stability levels.

Although individual devices and primitives of the CMOS process had been characterized previously at very low temperatures, showing that their electrical simulation models were acceptable well below the foundry specified temperature range, it was not completely sure that the ASIC would maintain its functionality down to temperatures as low as -135ºC. Therefore, these results represented a significant milestone.

Measurement set-ups and functional tests have been done at IMSE. Low-temperature functional tests have been carried out at INTA facilities. IMSE has recently acquired the nitrogen cooled equipment required for very low temperature tests.

IV. Radiation tests

As already mentioned, the IC process had been previously characterized for space use. This included very low temperature devices characterization (large signal transfer characteristics, mainly), and the analysis of radiation effects from the perspective of total ionizing dose (TID) and single event effects (SEEs). Those previous analyses showed that the devices (3.3V), with specific ELT layouts, could withstand significant amounts of high energy photons without drastic degradations. Levels reached in that characterization were above 300Krads. The specification for the present ASIC was only of 9Krads. Concerning SEEs previous tests has shown that similar mixed-signal ICs, in the same process, using the same RHBD techniques and the specific rad-hard digital library, had a single-event upset (SEU) linear energy transfer (LET) threshold above ~30 MeV/(mg/cm^2) and a single-event latch-up (SEL) threshold above at least 80 MeV/(mg/cm^2). Still, tests were required and were carried out for the formal qualification of the ASIC.

TID tests were performed at the Centro Nacional de Aceleradores (CNA) [16], in Sevilla, using a Cobalt 60 gamma radiation source. Six IC samples were irradiated. They were kept biased at their nominal power supply voltage and at room temperature. The accumulated dose after 50H approx. (in one step) was 10.6Krads at a rate of approximatively 200 [rad(Si)/h]. No appreciable parameters shifts were detected in the subsequent electrical characterization, as expected. Figure 2: shows the TID test PCB.

Figure 2: Photograph of the TID test PCB in the irradiation area.

SEEs teste were performed at the Cyclotron Resource Centre [17] of the Université Catholique de Louvain (UCL). In order to fulfill the required test conditions, the device temperature had to be about 50ºC or larger. This was achieved exploiting the self-heating of the ASIC while in operation, taking temperature lectures from its internal PTAT, and modifying the amount of the heating currents in a controlled loop implemented in the test-set up software. The effective die temperature during the tests was about 65ºC. Two IC samples were tested, each using seven ion and incidence angle

combinations, with effective LET levels ranging from 16 to 81.6 MeV/(mg/cm²). Fluence for each specific ion/angle combination ranged from 1.2M ions/cm^2 for the higher energy combinations to 3.8M ions/cm^2 for the less energetic ones.

No latch-up was recorded up to the maximum effective LET available at the facility: 81,6 MeV/(mg/cm²)) using $^{124}Xe^{35+}$ ions with an incident angle of 40º. Figure 3: shows the SEEs test board with its latch-up detection circuitry, and the vacuum chamber at the UCL cyclotron facility.

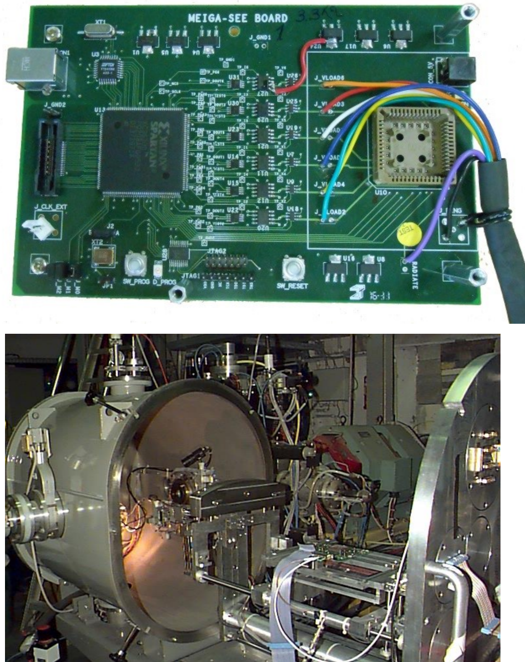

Figure 3: SEEs test board & vacuum chamber at the UCL cyclotron.

Concerning SEUs and single-event failure interrupts (SEFIs), no errors were detected up to a LET of 20.4 MeV/(mg/cm²) with $^{58}Ni^{18+}$. First few errors were observed with a LET of 32.4 MeV/(mg/cm²) with $^{84}Kr^{25+}$. Detailed estimations of upset rates under a geosynchronous orbit condition have been obtained using the procedures described in [18] and [19], resulting in figures lower than 1.5E-9 upsets/bit-day.

Displacement damages (DD) tests using some neutrons irradiation facilities were initially considered as well, but finally considered unnecessary, for a CMOS device, after the TID and SEEs results.

V. Packaging

The development of the MEDA instruments set relies, to a significant extent, on the results of a previous similar mission, REMS, [20], which contained a similar wind-sensor instrument. Much of the reliability issues and qualification processes take advantage of previous experience in REMS. The selected ASIC package, like in REMS, is a ceramic, 100 pins quad-flat package CQFP100. However, at the time of packaging the first ASIC-die samples, for the first functional tests, there were some procurement difficulties concerning the exact same package used in REMS. A CQFP100 from a similar manufacturer was then used for the initial samples, in order to proceed with the functional tests.

After the ASIC was found to be functional and within specs, an additional die lot was ordered from the foundry. These samples were then packaged in the same CQFP package used in REMS, which had been located by that time. This allowed us to skip a long and costly packaging qualification process. Furthermore, this avoided the significant cost of purchasing ASIC carriers and sockets, required for the screening and qualifications processes, since they were available at Alter facilities from the previous REMS ASIC qualification works.

The new dies lot was then packaged under space-use conditions by Optocap [21], and the screening and qualification processes begun on these flight-oriented ASIC lot. Figure 4: one of the final-packaged ASICs.

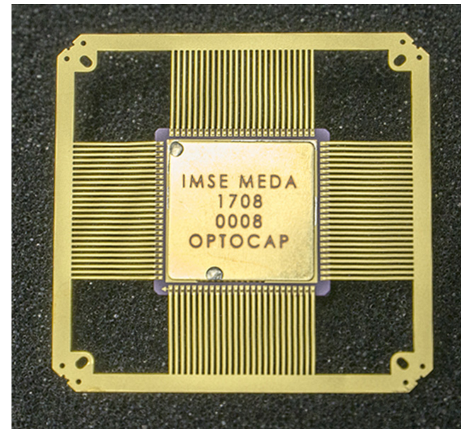

Figure 4: ASIC sample in its final package.

The ASIC function includes heating external silicon dies employed in the wind sensor set-up. The amount of heating power required, which is programmable due to the variable environmental conditions expected along the mission, poses eventual problems with ASIC operating temperature, since part of the “external dies heating power” is dissipated within the ASIC. This is increased by the low density Mars atmosphere, which reduces the heat dissipation capability as compared to that on Earth. Measurements of the junction-to-case thermal resistance θ_{jc} of the packaged samples have been carried out, again exploiting the programmable self-heating capability of the ASIC. The values obtained is in the range of 20ºC/W, which does not represent a problem. An evaluation of the case-to-ambient thermal resistance θ_{ca}, which depends on the final PCB design and the Mars atmosphere conditions, will be carried out for final assessment.

VI. Qualification and Screening

The formal qualification of the ASIC and the screening of the samples for flying-modules (FM) selection have been carried out by Alter TÜV Nord, with the assistance of IMSE concerning the functional electronic measurement set-ups.

The sampled lot consisted of 81 units. After a packaging evaluation test which required five samples, a few samples were dedicated to measurements set-ups development, leads forming validation, and other miscellaneous issues. Finally, 69 samples entered the screening process, which consisted on a sequence of different tests with intermediate functional measurements at room temperature. Specific tests included

constant acceleration, particles impact noise detection (PIND), temperature cycling (-135 to +125ºC), power burn-in (160 hours), and detailed functional and parametric measurements in the operating temperature range (-128 to 50ºC) temperature range for FM units selection. Finally, a seal (fine and gross) test and an external visual inspection were performed. After defining the acceptance limits, 64 samples passed the screening tests. Also, 25 samples were selected as FM samples according to the predefined selection criteria. All tests were made according to their corresponding MIL-STD-883 rules, and/or the previously defined ASIC validation acceptance limits.

The qualification process has consisted in three test groups: environmental, mechanical, and endurance, followed by a destructive physical analysis (DPA) on a few samples. All tests have been performed according to their corresponding MIL-STD-883 methods.

The environmental tests, performed on 15 samples, consisted in a thermal cycling (100 cycles from -135 to +125ºC), and a moisture resistance test. It was followed by electrical measurements at room temperature, a seal test (gross and fine leaks), and an external visual inspection. All samples passed the tests.

The mechanical tests, also performed on 15 samples, begun with a dimensions and lead integrity test, and a seal (fine and gross leaks) test. This was followed by a mechanical shock test (shock response spectrum), random vibration with several variable frequencies, and constant acceleration test. Intermediate electrical measurements were performed. Finally, a seal after mechanical shock test and a final external visual inspection were performed. All samples passed the tests.

The endurance test group was performed on 8 samples. It consisted on an operating life test at a temperature of +70ºC, during 1000 hours, with intermediate electrical measurements after 168 and 500 hours. Again, a seal test followed. All samples passed the tests.

Finally, 5 samples went through a destructive physical analysis. Three of those samples were taken from those that had gone through the endurance test, and one each from the environmental and mechanical tests samples. These DPA consisted in external visual inspection, seal test, radiography, residual gas analysis (RGA), terminal strength, internal inspection, destructive pull test, scanning electron microscopy (SEM) inspection, and die shear test. All DPA tests were successful (the 5 sampled passed) except for the RGA which all samples failed. Excessive moisture was found inside the cavity, possibly due to insufficiently cured epoxy. However, after a specific test was designed and executed to evaluate the possibility of dendrites formation among adjacent pads, the results have been satisfactory and the manufactured lot has been considered qualified.

VII. Conclusions and Summary

The MEDA wind-sensor mixed-signal ASIC [1], designed in a standard 0.35µm CMOS process using RHBD techniques, has been functionally and parametrically characterized, and the manufactured lot has been qualified for space use under the specifications of the Mars2020 mission, including radiation and very-low-temperature effects. A screening process has been used to select the best samples. The ASIC is presently being integrated in the final instrument PCBs. Instrument calibration procedures will follow.

Acknowledgment

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