Multi-Channel Preamplifier IC for IR-Sensor and FPA Readout

J. Ackermann[a], S. Azman[a], C. Gheorghe[a], D. Meier[a], G. Maehlum[a]

[a]Integrated Detector Electronics AS, 0484 Oslo, Norway

joerg.ackermann@ideas.no

Abstract

The IDE1060 is an integrated circuit (IC) with 34 preamplifiers for reading out infrared (IR) sensors and focal-plane imaging arrays (FPA). We designed the circuit under contract with the European Southern Observatory (ESO) where the device shall be used with typical large-format astronomical IR sensors, *e.g.*, Raytheon Aquarius and Teledyne HAWAII-2RG. The IDE1060 is intended to replace the fast readout amplifiers described in [1]. The circuit is designed for extreme environmental conditions: cryogenic to room temperature, latch-up immunity and high energy threshold for single event upsets from ionizing radiation. We expect the circuit to be suitable for space-borne astronomical instruments as well. The device has been manufactured by AMS, and the characterization is planned for this year.

I. Introduction

A. ASIC Requirements and Applications

The requirements for the application specific integrated circuit (ASIC) are derived from the needs in terrestrial IR astronomical instruments. Low noise and operation at cryogenic temperatures are among the most important requirements for this application. In addition, the circuit was designed for space applications, requiring special design measures for latch-up immunity and single-event mitigation. The ASIC covers a wide range of different detectors and it is suitable for both cryogenic and space applications.

B. Design Heritage

The operational amplifier architecture used in the IDE1060 has been used successfully in previous IDEAS products: IDE3466 [2] and IDE3380 (SIPHRA) [3].

II. ASIC Design Specifications

A. Block Diagram

Figure 1 shows a block diagram of the sensor readout circuit IDE1060. The IC contains 34 identical preamplifier channels with input signals `IN[1:34]` and `REF` and differential output signals `OUTP[1:34]` and `OUTN[1:34]`. The channel gain is programmable in 8 steps from 2 to 16 (6dB to 24dB) using `GAIN[2:0]`. Each channel consists of two operational amplifiers (OA), a programmable resistive network and switchable capacitors that can be used to reduce the video channel bandwidth to about 3MHz using `BW-SWITCH`. The differential channel outputs can drive large capacitive loads of several hundred pF. The bias currents for the amplifiers are generated on-chip using an external bias resistor connected to `RBIAS`.

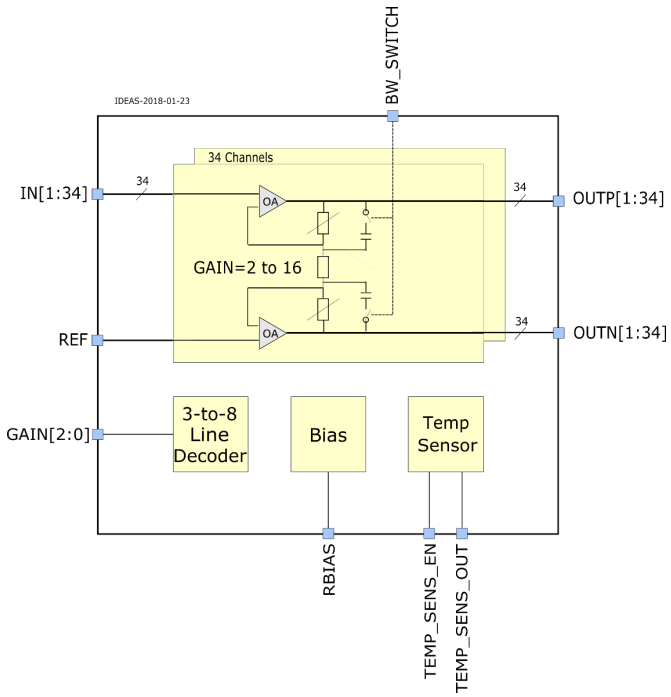

Figure 1: Block diagram of the IDE1060.

B. Key Features

Table 1 summarizes the key features of the IDE1060. The 34 differential voltage-amplifying channels have a programmable gain in 8 steps from 2 to 16 (6dB to 24dB). The differential channel outputs can drive long cables with several hundred pF of capacitance or used with external operational amplifiers and resistors to form classical three-amp instrumentation amplifiers. In addition, the chip contains one standalone amplifier that can be configured externally for different applications or debugging purposes. The chip also provides a temperature sensor. The IC operates at a nominal supply voltage of 3.5V and dissipates about 20 mW per channel at 77K. Various power-down modes are available for applications with less than 34 channels. The IDE1060 is latch-up immune and SEU-tolerant. The IC has been designed in a 0.35-μm CMOS process, and is available as bare die or in a ceramic QFP208 package.

Table 1: IDE1060 key features.

34 differential voltage amplifiers
Programmable gain, 6dB to 24dB 8 settings: 2, 4, 6, 8, 10, 12, 14, 16
Input-referred voltage noise 4.3nV/$\sqrt{\text{Hz}}$ at 10kHz, 6dB, 3.5V, 77K 33μV_{rms} at 1Hz to 50MHz, 6dB, 3.5V, 77K
>50MHz bandwidth at 6dB, 3.5V, 77K, 200pF load
<80ns settling time (0.01%) at 6dB, 3.5V, 77K
2V peak to peak max input swing at 6dB
Rail-to-rail output swing
Single supply voltage 3.3V to 3.6V
Operating temperature cryogenic operation (77K) with R(RBIAS)=174kΩ room temperature (298K) with R(RBIAS)=TBD
Latch-up immune, high threshold for single event upsets
On-chip temperature sensor
Power consumption 20mW per channel at 3.5V and 77K Several programmable power-down modes

1) Channel

A simplified view of one channel is shown in Figure 2. The channel consists of two operational amplifiers (OA) in a balanced non-inverting amplifier configuration with programmable gain. The input signal is applied to IN and a constant reference voltage is applied to REF. The differential output signal can be measured between OUTP and OUTN. The switchable capacitors for video-channel bandwidth reduction are not shown in the figure below.

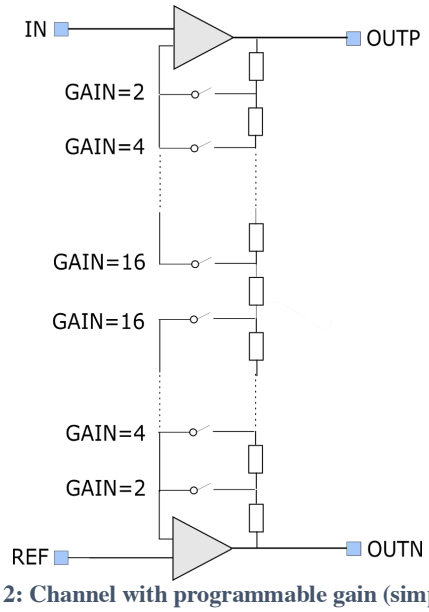

Figure 2: Channel with programmable gain (simplified).

2) Operational Amplifier

Figure 3 shows a simplified schematic of the operational amplifier. The amplifier consists of a folded-cascode input stage and a class-AB controlled output stage [4]. The architecture of the amplifier resembles the simplified schematic shown in the datasheet for OPAx350 [5], which is the amplifier used in the latest revision of the cryogenic preamplifier circuit described in [1]. Since the lowest gain in our application is specified to be 2, a rail-to-rail input stage consisting of parallel PMOS and NMOS differential input stages is not needed. Thus, the class-AB OA has an NMOS-only input stage, which has the advantage of lower input capacitance and less noise and does not suffer from input crossover distortion, a phenomenon commonly observed in rail-to-rail input stages when both input pairs are active.

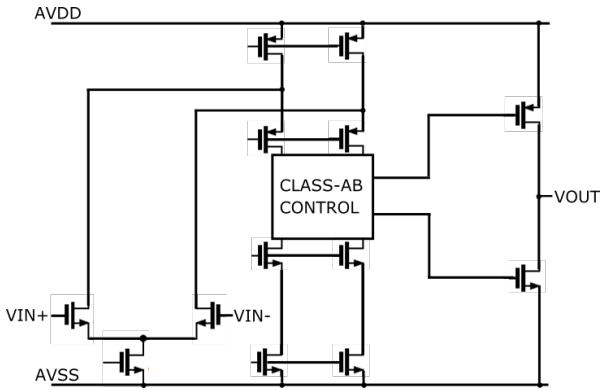

Figure 3: Simplified schematic of the class-AB operational amplifier.

III. ASIC LAYOUT

Figure 4 shows the layout of the chip. The active area is 5.62 mm x 11.64 mm. The area is relatively large, and half of the size is used for routing the output lines. The chip could be designed much smaller depending on package requirements. The IDE1060 has been designed in a 0.35-μm CMOS process and has been manufactured by AMS. All inputs are protected against electrostatic discharge (ESD).

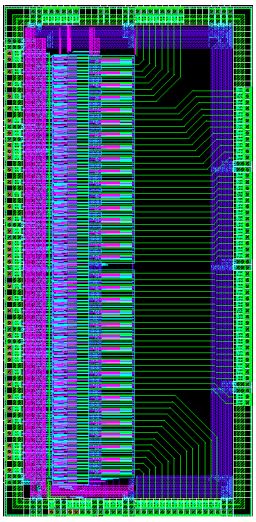

Figure 4: ASIC layout.

IV. ASIC Design Verification

The IC has been designed and verified using Cadence Virtuoso, Spectre, Assura DRC and LVS. All simulations have been run across corners (AVDD=3.3V-3.6V, process variation and Temp=77K-300K). The results shown in this chapter focus on the performance at 77K. Simulation results for both the operational amplifier and for a complete channel will be presented in this chapter.

A. Operational Amplifier

1) DC Characteristics

The typical quiescent current consumption of the operational amplifier is 2.77mA at 77K.

Table 2: Op-amp quiescent current consumption at 77K.

Min [mA]	Typ [mA]	Max [mA]
1.49	2.77	5.79

2) AC Characteristics

Figure 5 shows the open-loop alternating current (AC) frequency response of the operational amplifier at 77K. There are two ordinates: to the left is the output amplitude V from -50dB to +120dB and to the right the phase margin (PM) from -280 to +20 degrees. The abscissa is the frequency from 1Hz to 1GHz. From the figure one can obtain the direct current (DC) gain of 110.6dB and the unity gain-bandwidth (UGBW) of 84MHz with a phase margin (PM) of 63.5° for the nominal load capacitance of 200pF. The corner simulation results for 77K are listed in Table 3.

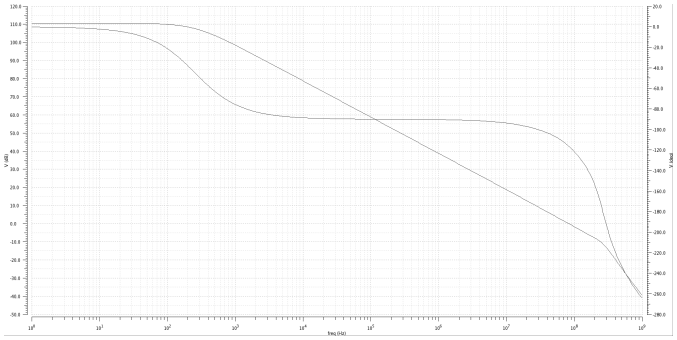

Figure 5: Frequency response of the operational amplifier.

Table 3: Op-amp DC gain, unity-gain-bandwidth (UGBW) and phase margin (PM), load=200pF at 77K.

Parameter	Min	Typ	Max
DC gain [dB]	104.5	110.6	115.8
UGBW [MHz]	59.2	84.0	119.0
PM [deg]	47.7	63.5	70.9

Figure 6 shows the power-supply rejection ratio (PSRR) of the operational amplifier with a capacitive load of 200pF as a function of frequency at 77K. The PSRR is 106.3dB at 1Hz and still 25.0dB at 10MHz. The corner simulation results for 1Hz at 77K are listed in Table 4.

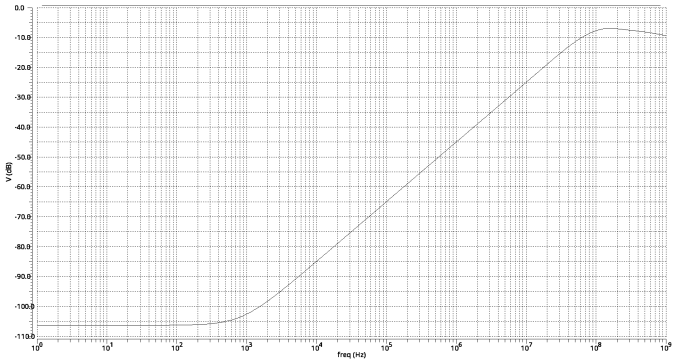

Figure 6: PSRR of the operational amplifier vs frequency.

Table 4: Op-amp PSRR at 1Hz [dB], load=200pF at 77K.

Min [dB]	Typ [dB]	Max [dB]
92.5	106.3	109.2

The input-referred noise of the operational amplifier has been simulated in a unity-gain configuration. Table 5 summarizes the corner simulation results for integrated input-referred noise and spot noise at a frequency of 10kHz at 77K.

Table 5: Op-amp input-referred noise at 77K.

Gain	Integrated (1Hz to 500kHz) [μVrms]	Integrated (1Hz to 50MHz) [μVrms]	Spot noise (f=10kHz) [nV/$\sqrt{}$Hz]
1	1.0	16.7	1.8

3) Transient Characteristics

Figure *7* shows the step response of the operational amplifier in a non-inverting configuration with gain=2 at 77K. The typical slew rate is 47.2V/μs and the settling time to within 0.01% of the final value is 72ns. The corner simulation results for 77K are listed in Table 6.

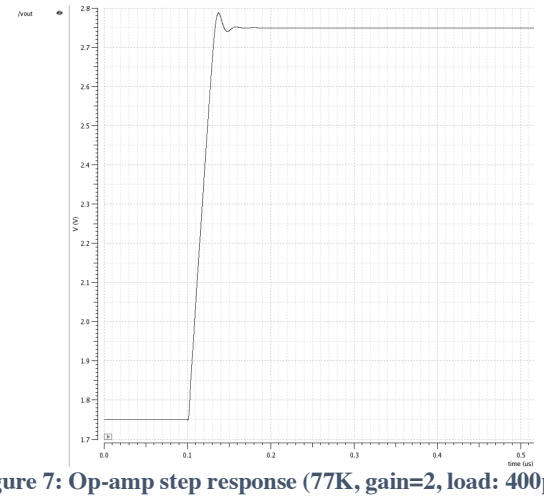

Figure 7: Op-amp step response (77K, gain=2, load: 400pF).

Table 6: Op-amp slew rate and settling time (77K, gain=2, load 400pF).

Parameter	Min	Typ	Max
Slew rate [V/μs]	37.6	47.2	61.4
Settling time (0.01%) [ns]	56.4	72.0	91.5

B. Channel

1) Channel Noise

Low input-referred noise is among the most important design requirements for the IDE1060. Table 7 summarizes the corner simulation results for integrated input-referred noise and spot noise of a complete channel at a frequency of 10kHz at 77K using four different gain settings.

Table 7: Channel input-referred voltage noise (77K, 3.5V).

Gain	Integrated noise (1Hz to 500kHz) [μVrms]	Integrated noise (1Hz to 50MHz) [μVrms]	Spot noise (f=10kHz) [nV/√Hz]
2	2.8	33.2	4.3
4	2.5	30.8	4.0
8	2.1	27.6	3.5
16	1.8	25.6	3.1

2) Channel Bandwidth and Gain

Figure 8 shows the differential output signal of the channel for eight different gain settings from 2 to 16 at 77K. A 100-kHz sinusoidal signal with an amplitude of 100mV is applied to IN, while a constant voltage of AVDD/2 is applied to the reference input.

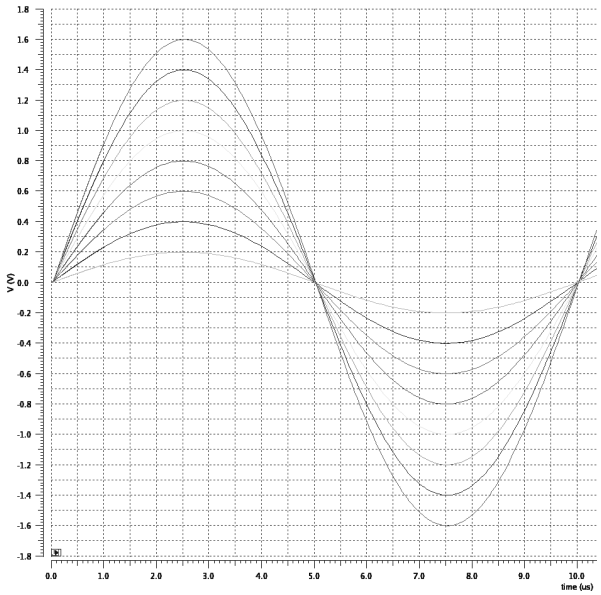

Figure 8: Differential output signal for GAIN=2 to 16 (input signal amplitude: 100mV, frequency=100kHz) at 77K, AVDD=3.5V.

Figure 9 shows the cut-off frequencies of the channel for different gain settings at 77K.

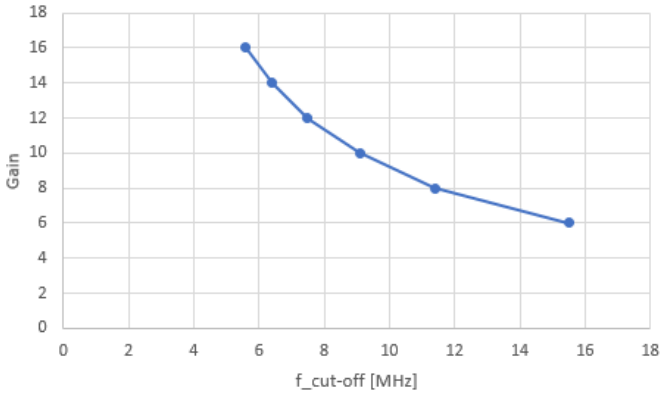

Figure 9: Gain setting vs cut-off frequency at 77K, AVDD=3.5V.

V. ASIC CHARACTERIZATION

The IDE1060 will be packaged in a ceramic 208-pin quad flat pack (QFP) package and mounted on a test board. For specification compliance tests, external signal sources will be connected directly to the test board. For the final tests, comparing the new preamplifier solution with the original design, an HAWAII2RG detector will be placed in the cryogenic chamber and connected to the test board. All tests will be carried out in the cryogenic chamber under vacuum conditions at 77K. Figure 10 shows a photograph of the cryogenic chamber in our lab. A chip is mounted on the circuit board inside the chamber.

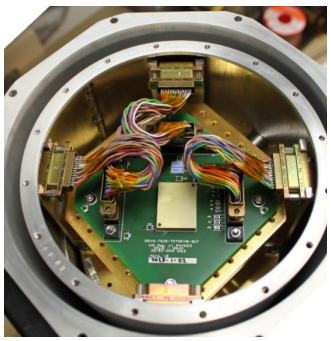

Figure 10: Test board in cryogenic chamber.

VI. SUMMARY

We have designed a 34-channel preamplifier circuit with programmable gain for readout of infrared sensors and focal-plane imaging arrays in cryogenic and space applications. The video-channel bandwidth and the number of active channels can be selected by the user. Simulation results for both the standalone amplifier and for a complete channel have been presented. The circuit has been designed using a 0.35-μm AMS CMOS process. Samples will be available in Q3 2018.

VII. ACKNOWLEDGEMENTS

The authors would like to acknowledge the support from the European Southern Observatory.

VIII. REFERENCES

[1] Ives, D. et al., "Performance evaluation of 5µm cut-off Hawaii-2RG detectors using the fast readout amplifiers", Proc. SPIE 7742 (2010).

[2] Stein, T. et al., "Front-End Readout ASIC for Charged Particle Counting with the RADEM Instrument on the ESA JUICE Mission", Proc. SPIE 9905 (2016), http://dx.doi.org/10.1117/12.2231901

[3] Meier, D. et al.," SIPHRA 16-Channel Silicon Photomultiplier Readout ASIC", Proc. AMICSA&DSP 2016, Gothenburg, Sweden, http://dx.doi.org/10.13140/RG.2.1.1460.8882

[4] Hogervorst, R. et al., "A Compact Power-Efficient 3V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", IEEE Journal of Solid-State Circuits, Dec. 1994

[5] OPAx350 datasheet (Texas Instruments): http://www.ti.com/lit/ds/symlink/opa350.pdf