A rad-hard system-on-chips solution for closed-loop motion control

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Abstract

This paper describes the design and implementation of a system-on-chips solution for closed-loop control of remote-handling robotic tools in radiation environment. Five ASICs have been designed in two commercial CMOS technologies (DARE350ON and DARE65T [1]), including a resolver or LVDT to digital converter, a resistive bridge sensor signal conditioner, a 24V/48V 10-channel limit switch conditioning IC, a 24V/48V10-channel low-side driver IC, and a bus communication ASIC. Several rad-hard and silicon-proven Analog/Mixed-signal IPs on the 65nm CMOS technology have also been developed, e.g., ADC, PGA, LDO, Clock generator, Voltage reference, and PLL.

Radiation-hardened-by-design (RHBD) techniques are used in the design of the ASICs to achieve TID tolerance of more than 100 Mrad and SEL/SET/SEU hardness of higher than 60 MeV•cm^2/mg.

I. Introduction

The original intended application of the development is for remote handling equipment at ITER (a first-of-kind Tokamak fusion nuclear plant). Front-end electronics that located close to sensors and actuators on ITER remote handling systems will face gamma radiation up to a total dose of 100 Mrad, and total neutron fluence up to 10^{15} n/cm^2. Hence those electronics are required to be radiation-hardened against total-ionizing-dose (TID) radiation, as well as single-event effects (SEE) caused by neutrons (14 MeV). In order to broaden the application scope of the system, the chips were also designed to be resistant against higher energy particles (e.g., >60 MeV protons and heavy ions).

A typical closed-loop position sensing and motion control system consists of the following sensor/actuator types:

- Position sensors (resolvers, LVDTs, IMUs)
- Resistive bridge sensors (thermocouples, potentiometers, load-cells, strain gauges, magnetic sensors)
- Limit switches
- Relays (both mechanical and solid-state)
- Motors

Then, a fieldbus is required to connect all sensors and actuators to a motion controller to form a real-time, deterministic control loop. In this development, the BiSS-interface (bidirectional/serial/synchronous) is used as the fieldbus protocol. The BiSS-interface is an open-source protocol. It is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. The BiSS protocol is designed in B mode and C mode (continuous mode). It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort. The BiSS interface physical layer is defined as either RS485 (10 Mbps) or LVDS (100 Mbps). The BiSS interface employs a synchronous method for data transmission, therefore, the overhead (Flag bits + CRC) of the protocol can be minimized, comparing to other fieldbus protocols (e.g., CAN, EtherCAT, and Profibus).

Finally, five system-on-chips have been developed for the closed-loop control system, which are:

- ASIC1: a resolver/LVDT to digital converter that reads out angle information from a resolver or linear distortion information from a LVDT;
- ASIC2: a resistive bridge sensor conditioner to read out RTDs, thermocouples, and strain gauges;
- ASIC3: a 10-channel limit switch conditioning IC to readout the on/off status of 24V/48V limit switches;
- ASIC4: a 10-channel low-side driver chip to drive 24V/48V mechanical/solid-state relays;
- ASIC5: a bus communication ASIC including the BiSS-interface [2] protocol controller, the SPI master protocol controller, and on-chip RS-485 bus transceivers.

The potential space applications of the closed-loop motion control system could be:

- Control of remote handling manipulators and remote operated vehicles;
- Speed control of reaction wheels;
- Control of electrical propulsion system;
- Altitude control of satellites;
- Control of electrical valves.

In the following sections, more details about the ASIC's functionalities and designs are described. Technical specifications of several Analog/Mixed-signal IPs on the 65nm CMOS process will also be given, as well as applied radiation-hardened-by-design techniques.

II. ASIC DESCRIPTION

A. Resolver/LVDT to digital converter

ASIC1 is a Resolver/LVDT to digital converter, which is designed to readout the angular information from a resolver or the linear distortion information from a LVDT. A digital control bit is used to switch between the two functions. A block diagram of the ASIC1 is shown in Figure 1.

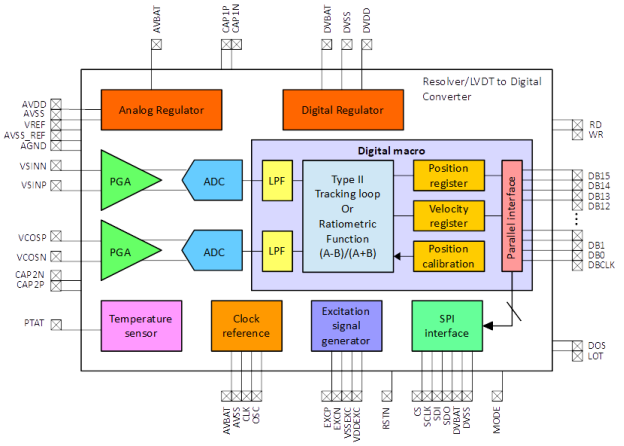

Figure 1: Block diagram of the resolver/LVDT to digital converter

The resolver is read by digitizing both signals coming from the resolver secondary windings (Vcos and Vsin) by the signal conditioning circuits (PGA and ADC) shown in the figure. The output signals of two delta-sigma ADCs are first streamed to two identical digital low pass filters (LPF), which removes high-frequency quantization noise from the ADC output. The Filtered ADC signals are then fed into a digital tracking loop where the angular calculation is performed. The results are kept in the position, and velocity registers accordingly.

An excitation signal generator generates a sine wave signal for the primary winding of the resolver or the LVDT. However, a typical resolver/LVDT requires a low-impedance 3-Vrms to 7-Vrms signal to drive the primary winding. Operating with a 1.2V supply, the RDC can only deliver 1.8V peak-to-peak differential signal on the excitation outputs. This signal might not have sufficient amplitude and drive capability to meet some resolver/LVDT's input specifications. A solution to this problem is to use an off-chip amplifier to amplify the sinusoidal signal sent to the primary winding. A digital format of the excitation signal is needed by the tracking loop for demodulating the sin/cos signals, which will be generated by the on-chip reference.

An example of system-level integration of the ASIC1 is shown in Figure 2. In total five off-chip capacitors would be required. Two of them are used for stabilizing the on-chip power regulators, and the other three are needed by the Analog-to-digital converter.

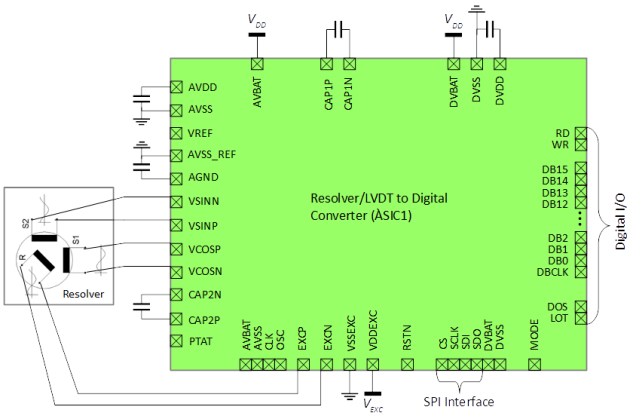

Figure 2: System integration of ASIC1

Major specifications of the ASIC1 are listed in Table 1.

Table 1: ASIC1 Electrical Specifications

Specifications	Unit.	Typical
Supply voltage	V	1.2
Power consumption	mW	20
Resolution	bits	16
Accuracy	arc min	3
Bandwidth	Hz	800
Tracking rate	rps	500
Excitation frequency	kHz	2.5
SPI data rate	Mbps	10

B. Resistive bridge sensor conditioner

ASIC2 is a generic signal conditioning circuit for reading out sensors such as RTD, thermocouple and strain gauge (as shown in Figure 3). An RTD or strain gauge converts a physical value (temperature or pressure) to a variable resistive value. A Wheatstone bridge circuit is often used to measure a variable resistance with great accuracy. The output of a bridge circuit is a small voltage signal, which needs to be amplified by a low-offset, programmable-gain instrumentation amplifier. After the amplification, an ADC converts this signal into a digital bit stream. The same signal conditioning circuit can also be used to readout a thermocouple temperature sensor. However, in this case, a second signal conditioner will be required to readout a reference temperature at the cold junction, which could be done by employing the on-chip silicon temperature sensor.

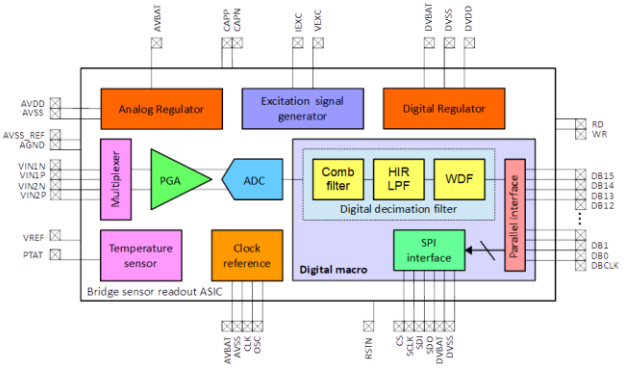

Figure 3: Schematic of the resistive bridge sensor conditioner

A multiplexer with two differential inputs can be used to connect multiple sensors to the same signal conditioning circuits. Furthermore, a clock reference provides the timing signal for the ADCs and all other digital processing blocks. A low-dropout voltage regulator (LDO) is employed to provide supply voltages for all functional blocks. A serial peripheral interface (SPI) is used here to communicate the output results. The DC excitation voltage for the bridge circuit can also be generated from the ASIC.

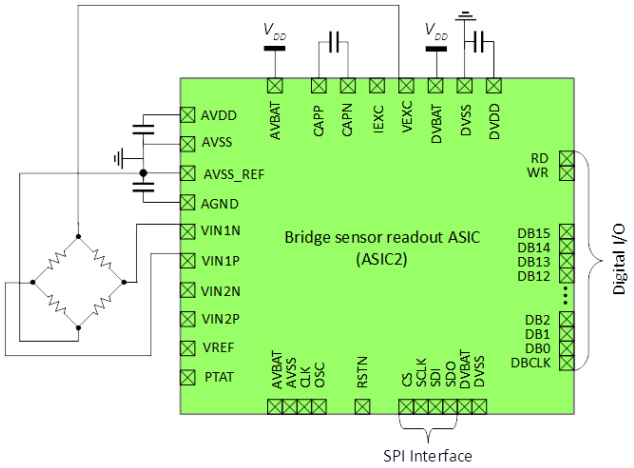

Figure 4: System integration of ASIC2

An example of system-level integration of ASIC2 is shown in Figure 4, and major specifications of the ASIC2 are listed in Table 2.

Table 2: ASIC2 Electrical Specifications

Specifications	**Unit.**	**Typical**
Supply voltage	V	1.2
Power consumption	mW	10
Gain range		1 ~ 256
Gain offset	%	2
Gain error	%	±0.5
Bandwidth	Hz	2.5k
Gain drift	ppm/°C	10
Offset drift	nV/°C	10
Input noise	nV/√Hz	35
Offset	µV	5
ADC resolution	bits	16
Excitation voltage	Vdc	1.2
Excitation current	µA	200
SPI data rate	Mbps	10

C. *Limit switch conditioning IC*

The ASIC3 consists of 10 individual sensing channels. Each of them capable of reading the status of the limit switch connected to it. They are all identical and are a cascading of several level shifters to translate the high voltage output signal of the limit switch to a low 3.3V domain.

The status of the limit switches can be read out via SPI or parallel interface. If the parallel interface is used only 5 of 10 channels at the same time can be read out. The parallel interface is mainly used for test. A readout of the status of all channels at the same time can be done via SPI interface.

The ASIC is designed in such a way that the limit switch needs to be on the high side (see Figure 5). The high output voltage of a limit switch (24V/48V) first needs to be down shifted to a lower level. This is done by a resistive divider. To make the design ESD proof it is necessary to put the upper resistor of this divider off chip.

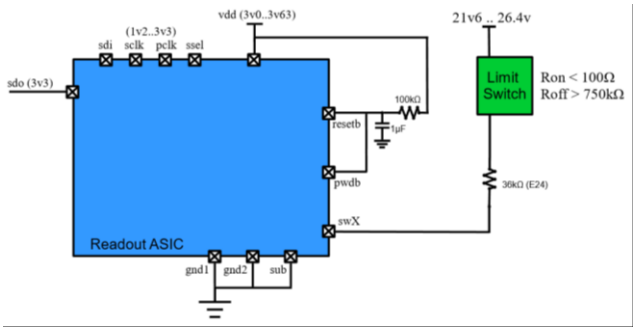

Figure 5: System-level integration of the limit switch conditioning IC

D. *10-channel low-side driver IC*

The ASIC4 consists of 10 individual driver channels. Each of them capable of sinking 130mA through a low-side switch from a high voltage supply of 24V/48V at a maximum switching frequency of 17kHz.

Every of the 10 driver channels has a built-in protection mechanism by means of an over-temperature detection (OTD) and over-current detection (OCD). Those detection blocks can instantly shut down the driver channel in case of an over-temperature or an over-current event.

The OTD block monitors the temperature of the driver channel nearby the output device. If temperature becomes too high, the specific channel immediately goes in a non-conductive state. When temperature drops again to a safe operation region, the normal operation of the channel is resumed. The OCD block monitors the current through the switch device of the channel. If an over-current situation is detected the driver channel goes immediately in a non-conductive state. The non-conductive state after an OCD event is preserved until a reset pulse is send to the driver channel. This reset pulse comes from the digital macro and needs to be initiated by a SPI command. If the over-current situation still exists after a reset, the driver channel goes back in the non-conductive state.

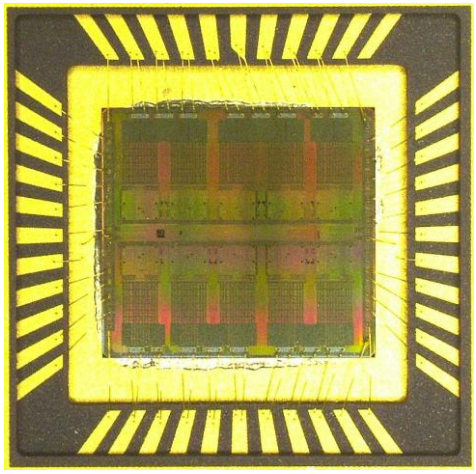

Figure 6: Die photo of ASIC4

To achieve Mrad-level ionizing radiation tolerance, thorough radiation hardness techniques in design and layout are implemented. Also, techniques are used to increase robustness towards SEL and SET/SEU. In design, techniques as triple mode redundancy (TMR), Analog voting and DICE latching are applied. Sizing of all devices is done by simulating them with adapted simulation models to simulate the effect of the ionization. A customized radiation-hardened layout is made for the high voltage output switching DMOS present in every driver channel.

E. Bus communication ASIC

The bus communication ASIC consists of a BiSS-interface controller, a SPI master controller and three RS-485 transceivers. The communication ASIC connects all other four ASICs into the same bus system, as shown in Figure 7. The integrated on-chip RS-485 drivers are capable of transmitting signals over a 150-meter cable at a speed of 5 Mbps. They can handle large ground potential differences along the long communication cable in the bus system. The acceptable input common mode range can vary between -7V up to +7V.

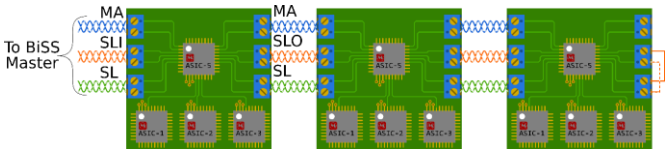

Figure 7: BiSS-interface bus configuration

III. Rad-hard 65nm CMOS Analog/Mixed-signal IPs

Generic rad-hard Analog/Mixed-signal IPs on 65nm CMOS have been developed to enable easier integration of the system-on-chips, including an Analog-to-digital converter (ADC), a programmable gain amplifier (PGA), a clock reference, a bandgap voltage reference, a PTAT temperature sensor, a linear regulator and a Phase-locked loop (PLL). Technical specifications of these IP blocks are summarized in Table 3.

MAGICS Instruments has developed a unique rad-hard IC design environment to achieve high first-time-right rate and high reliability:

- Industrial standard EDA tools: MATLAB for system behavioural model simulation; Cadence Virtuoso design tools for schematic edit, simulation and layout; Cadence Incisive and Innovus for digital design and implementation; Mentor Graphics Calibre for physical verification and sign-off.
- Experimentally verified transistor radiation model for TID (total-ionizing-dose) simulation.
- In-house proprietary TMR (triple modular redundancy) generator and SET simulator for single-event simulation.

The following RHBD techniques are applied in the design of the IPs to improve their radiation hardness:

- use dynamic compensation techniques [3] to mitigate radiation-induced performance drifts;
- use enclosed-layout I/O transistors to reduce radiation-induced leakage currents [4];
- use guard-rings to mitigate inter-device leakage [5];
- use radiation-aware transistor sizing to limit radiation-induced threshold voltage shift;
- use guard-rings and abundant contacts for all wells to mitigate single-event-latchup;
- use triplication and voting for all digital circuits to mitigate single-event-upset;
- use averaging and filtering in analog circuits to reduce single-event-transient.

IV. Conclusion

This work presents a rad-hard system-on-chips (SoCs) solution for position sensing and motion control. An SoC integrates an electronics system into one single chip, and require very few external components, hence significantly reduces the cost and complexity of system-level integration. The deterministic, real-time, low-power, small-size and radiation-hard features of the closed-loop system made it very suitable for applications in the harsh space and nuclear environment.

Furthermore, the reliable rad-hard IC design environment and the IP library greatly enhance the reproducibility, maintainability, and upgradability of the platform.

V. Disclaimer

The views expressed in this publication are the sole responsibility of the authors and do not necessarily reflect those of the ITER Organization or Fusion for Energy. Neither Fusion for Energy nor any person acting on behalf of Fusion for Energy is responsible for the use which might be made of the information in this publication.

VI. References

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[2] BiSS-interface introduction. Available online: http://biss-interface.com/

[3] Cao Y., De Cock W., Steyaert M., Leroux P., "A 4.5 MGy TID-tolerant CMOS bandgap reference circuit using a dynamic base leakage compensation technique," in IEEE Transactions on Nuclear Science, vol. 60, no. 4, pp. 2819-2824, 2013.

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[5] R. C. Lacoe, "Improving Integrated Circuit Performance Through the Application of hardness-by-Design Methodology," IEEE Trans. On Nuclear Science, vol. 55, no. 4, pp. 1903–1925, Aug. 2008.

Table 3: Technical specifications of 65nm CMOS rad-hard Analog/Mixed-signal IPs

Programmable Gain Amplifier	**Phase-Locked Loop**	**Analog-to-Digital Converter**
Gain: 1 ~ 256 Gain error: ±0.5% Gain drift: 10 ppm/°C Offset: 5 µV Offset drift: <10 nV/°C Input noise: 20 nV/√Hz TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Frequency: 2.2 ~ 3.2 GHz Bandwidth: 0.7 ~ 2 MHz RMS jitter: 350 fs Power: 12 mW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (silicon proven)	Resolution: 16 bits Bandwidth: 20 kHz SNDR: 96 dBFS Power: 5 mW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)
Voltage reference	**Clock reference**	**Temperature sensor**
Temperature range: -50 ~ 125 °C Temperature coefficient: 30 µV/°C Power: 80 µW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Frequency: 8 ~ 12 MHz Temperature coefficient: 30 ppm/°C RMS jitter: 25 ps Power: 360 µW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Temperature range: -50 ~ 125 °C Temperature coefficient: 1.5 mV/°C Accuracy: <1 °C Power: 60 µW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)