Common DPU and Basic Software for JUICE Instruments

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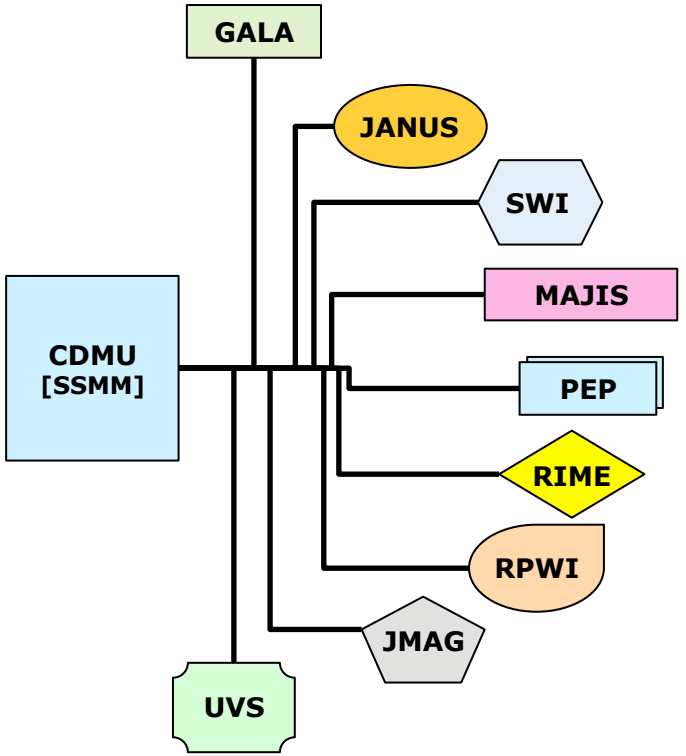
Outline

- Introduction
- Common DPU & BSW activity
- The common DPU
- The common Basic Software
- Lessons learned and conclusions



Introduction

JUICE science and instruments

Science Objectives

- Exploration of the Jupiter system
  - Jovian atmosphere
  - Jovian magnetosphere
  - Jovian satellite and ring systems
- Exploration of habitable worlds
  - Ganymede as a planetary object and possible habitat
  - Europa's recently active zones
  - Callisto as a remnant of the early Jovian system

Instrument suite

JANUS: moons geology, cloud morphology and dynamics

MAJIS: chemistry, atmospheric and surface composition

UVS: atmosphere of moons and aurora of Jupiter

SWI: Jupiter wind, moons atmospheric temperature and composition

GALA: moons shape and topography

RIME: moons surface study

3GM: gravity field and moon interiors

J-MAG: magnetic field

PEP: plasma environment and study of neutral and ion composition of exospheres

RPWI: plasma environment

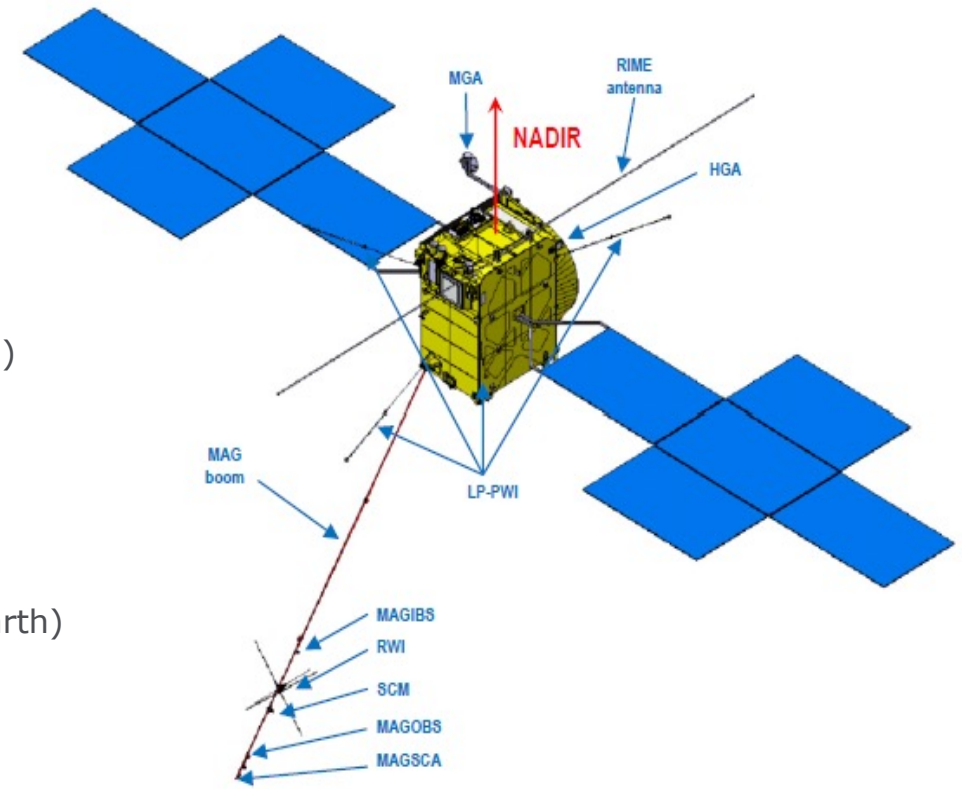
Spacecraft and mission characteristics

Spacecraft

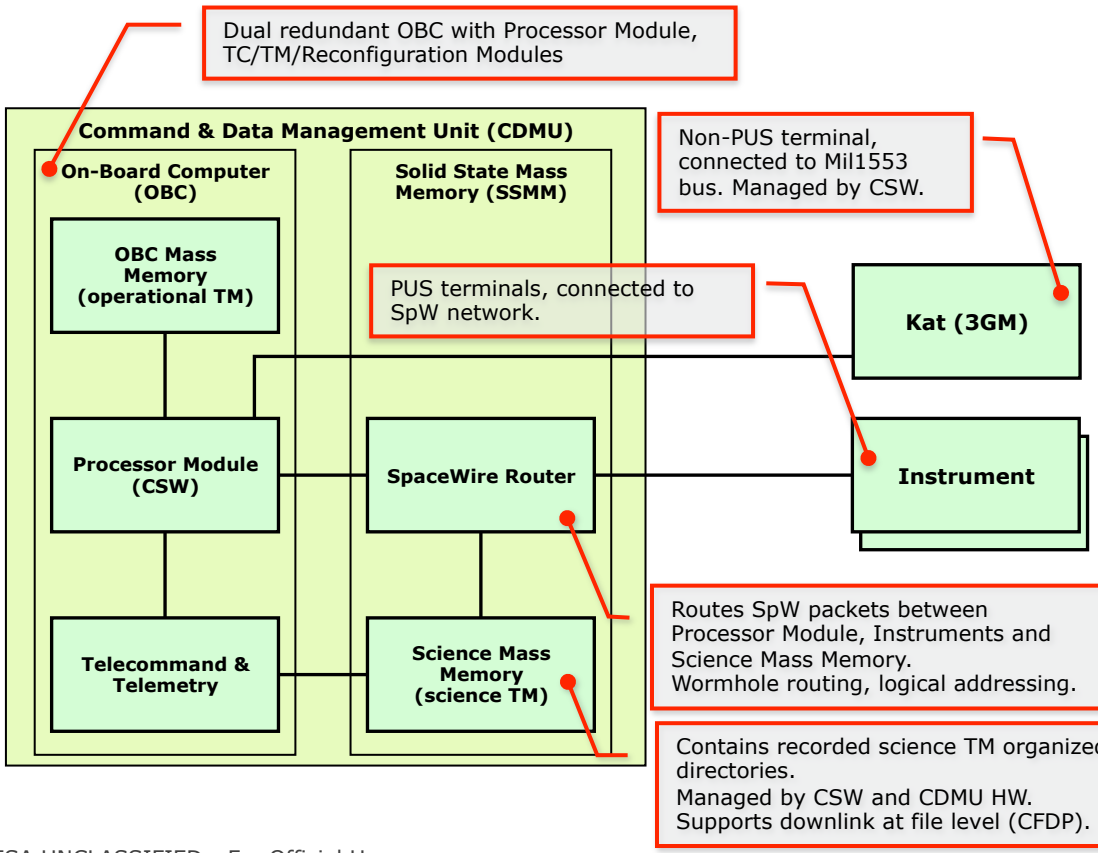
- Mass
  - Dry ≈ 2200 kg
  - Propellant ≈ 2900 kg
  - Total > 5000 kg
  - Instruments = 260 kg
- Power
  - Solar Array ≈ 725 W EOL
  - Instruments GCO500 = 180 W
  - Instruments fly-by = 230 W (360 W for ½ h)
- Memory = 1 Tbit EOL
- Δv ≈ 2400 m/s
- Downlink data rate: 1.4 Gb/24 h

Mission

- Launch date May 2022
- 5 gravity assists (Earth, Venus, Earth, Mars, Earth)
- Cruise phase ≈ 7.5 years
- Science phase ≈ 3.5 years



CDMU & Instruments



CDMU:

- OBC: processor, TM/TC, mass memory (and reconfiguration)
- SSMM: SpW router, science mass memory

Instruments (SpW):

- GALA, JANUS, MAJIS, RPWI, UVS, J-MAG, RIME, PEP-Lo, PEP-Hi, SWI and HAA (3GM)

Instruments (Mil1553):

- Kat (3GM)

Common DPU & BSW activity

Instruments at B1 phase

- **10 Instruments** developed by different institutes (PIs) at Instrument Consolidation Review (ICR)
  → **10 different designs** for the Digital Processing Unit (DPU).

Similar scenario observed also in **Bepi-Colombo** and **Solar Orbiter** where a similar suite of instruments is present,

In particular:

- Only partial reuse of **Boot SW** or other SW libraries from previous missions
- **very different level of quality** of SW data packages between instruments
- In some cases, **RTEMS OS included in Boot SW** (mission critical, category B)!
- **Delays** and **cost overruns** also due to DPU and SW development/validation

JUICE instr. status at ICR

Instr	CPU	MIPS	Memory	SpW
GALA	UT699	20	- 512 kB EEPROM - 128 MB SDRAM	100
JANUS	GR712RC	<80	- 32 MB Flash - 256 MB SDRAM	-
JMAG	LEON3FT-RTAX	20	- EEPROM - SRAM	10
MAJIS	AT7913E	<45	- EEPROM - SRAM	10 Rx, 100 Tx
PEP	OR1200	20	- 8 MB Flash - 16 MB SRAM	10
RIME	LEON3 RTAX4000	~20	- EEPROM - SRAM	10
RPWI	UT699	<60	- 2 MB MRAM - 32 MB SRAM	-
SWI	Custom RTAX	~20	- 512 kB SRAM	-
UVS	8051	<5	- 128 kB EEPROM - 128 kB SRAM	10 Rx, 40 Tx

How to improve?

- **Focus on the commonalities:**:
  - Interface to the OBC/SSMM (i.e. SpW)
  - Redundancy scheme (i.e. 2 cold redundant DPUs, 2 SpW links)
  - Processor (i.e. LEON 2 or 3) and memories
  - EEE parts
  - Basic SW libraries (i.e. Boot SW, RTOS, Driver SW, PUS library)
  - SW Validation Facility
- **Flexibility & configurability**
  - CPU performance and memory size
  - Form factor and mechanical interface
  - Instrument-specific functions and interfaces
- **Constrains**
  - Power consumption
  - Radiation tolerance
  - Generic vs. specific

How the problem was addressed in JUICE

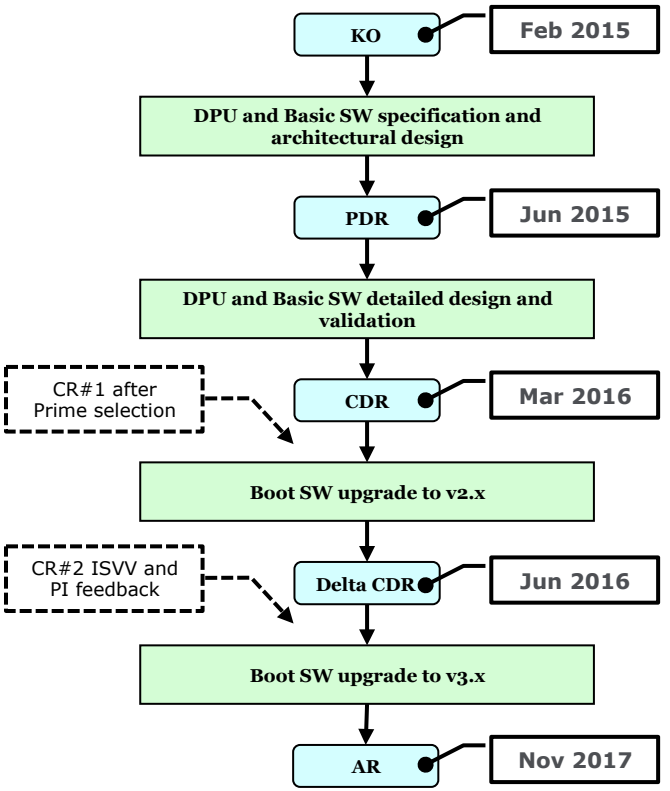
- **EXPRO** contract *(ref. 4000113396/15/NL/BW)*

  Common development of:

  → **DPU processor section design (CPU, SpW, memories)**: schematics, EEE parts list, analyses, verification tests, HW prototype

  → **Basic SW (Boot, Standby & Drivers)**: source code, unit/integration/validation tests, ECSS documentation

- PI <u>still</u> responsible for:
  - → procurement of EEE parts
  - → instrument-specific DPU functions
  - → instrument DPU manufacturing and test
  - → Boot & Standby SW validation in context



Deliverables 1/2

Document Id	Title
BOOT-SW-RS	DPU Boot SW Requirements Specification
BOOT-SW-ADD	DPU Boot SW Architectural Design Document
BOOT-SW-ICD	DPU Boot SW Interface Control Document
BOOT-UT-PLAN	DPU Boot SW Unit Test Plan
BOOT-VT-PLAN	DPU Boot SW Validation Test Plan and Specification
BOOT-SW-VCD	DPU Boot SW Verification Control Document
BOOT-SW-BUD	DPU Boot SW Budget Document
HDSW-SW-RS	DPU HW Driver SW Requirements Specification
HDSW-SW-ADD	DPU HW Driver SW Architectural Design Document
HDSW-SW-ICD	DPU HW Driver SW Interface Control Document
HDSW-UT-PLAN	DPU HW Driver SW Unit Test Plan
HDSW-VT-PLAN	DPU HW Driver SW Validation Test Plan and Specification
HDSW-SW-VCD	DPU HW Driver SW Verification Control Document
HDSW-SW-BUD	DPU HW Driver SW Budget Document
PSEC-HW-RS	DPU Processor Section Requirements Specification
PSEC-HW-ADD	DPU Processor Section Architectural Design Document
PSEC-HW-ICD	DPU Processor Section HW/SW Interface Control Document
PSEC-HW-LIST	DPU Processor Section EEE Parts List
PSEC-VV-PLAN	DPU Processor Section Verification Test Plan
PSEC-HW-VCD	DPU Processor Section Verification Control Document
PSEC-HW-PSA	DPU Processor Section Parts Stress Analysis
PSEC-HW-RAD	DPU Processor Section Radiation Analysis
PSEC-HW-WCA	DPU Processor Section Worst Case Analysis
PSEC-HW-FMECA	DPU Processor Section FMECA

Deliverables 2/2

Document Id	Title
BOOT-SW-DD	DPU Boot SW Design Document
BOOT-UT-REP	DPU Boot SW Unit Test Report
BOOT-SW-CF	DPU Boot SW Configuration File
BOOT-SW-UM	DPU Boot SW User's Manual
BOOT-VT-REP	DPU Boot SW Validation Test Report
HDSW-SW-DD	DPU HW Driver SW Design Document
HDSW-UT-REP	DPU HW Driver SW Unit Test Report
HDSW-SW-CF	DPU HW Driver SW Configuration File
HDSW-SW-UM	DPU HW Driver SW User's Manual
HDSW-VT-REP	DPU HW Driver SW Validation Test Report
PSEC-HW-DD	DPU Processor Section Design Document
PSEC-HW-SCH	DPU Processor Section Schematics
PSEC-HW-CF	DPU Processor Section Configuration File
PSEC-HW-UM	DPU Processor Section User's Manual
PSEC-VV-REP	DPU Processor Section Verification Test Report
DPU-FP	Final Presentation/Final Report

ISVV reports:

- *JUI-ISVV-DPU-RDVR - DPU Req. and Design Verification Report*
- *JUI-ISVV-DPU-CVR - DPU Code Verification Report*
- *JUI-ISVV-DPU-TVR – DPU Test Evaluation Report*
- *JUI-ISVV-DPU-V300VR – DPU Boot Software V3.0.0 Verification Report*

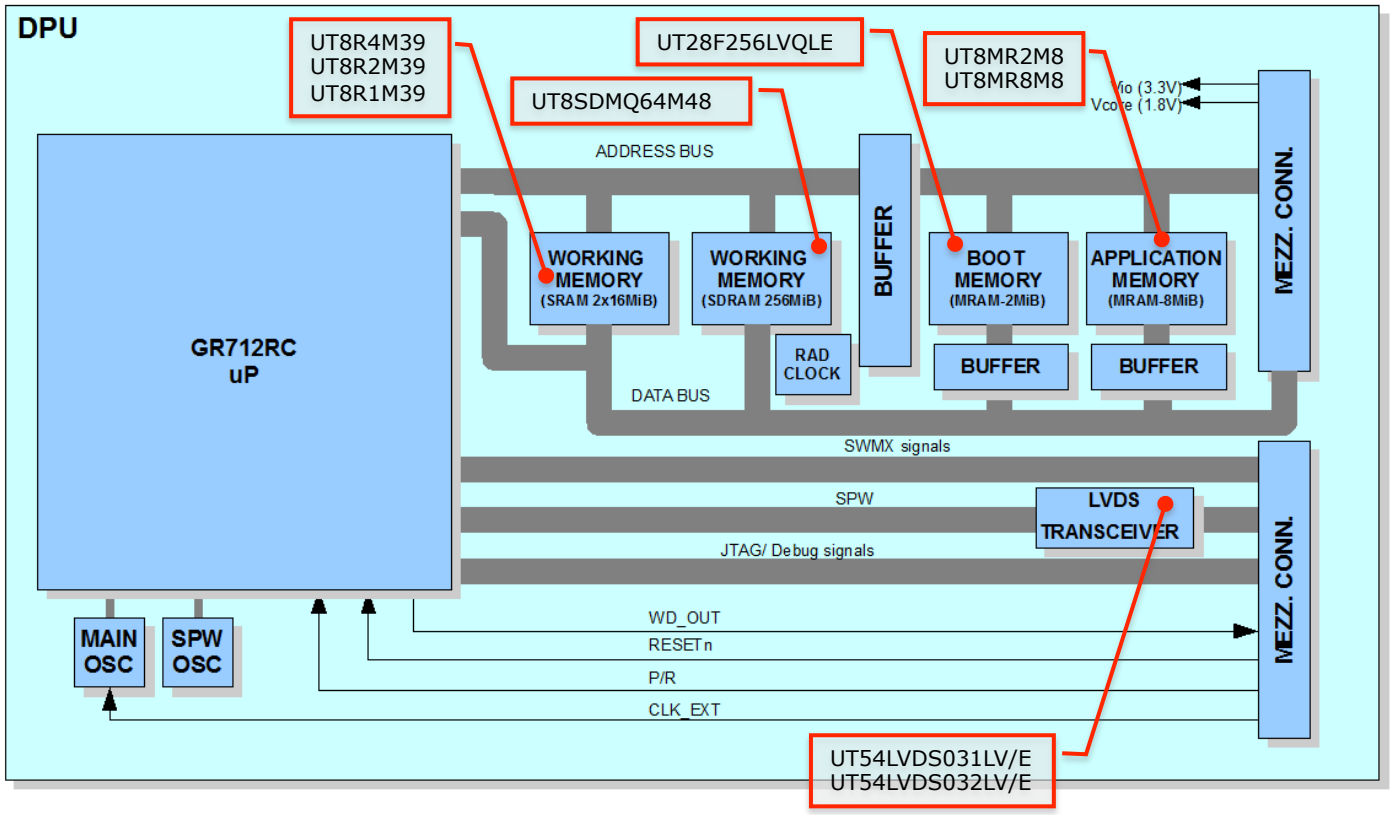
ESA complementary documents:

- *JUI-EST-SYS-MX-001 - BOOTSW-SGICD compliance*
- *JUI-EST-SYS-RP-027 - AUTOMATIC ASW START*
- *JUI-EST-SYS-RP-030 - PUS6 ADDRESSING*
- *JUI-EST-SYS-RP-031 - ACK FLAGS*
- *JUI-EST-SYS-RP-033 - ANOMALY IN SpW TDP*
- *JUI-EST-SYS-RP-034 - PUS 6 MEMORY ID 2*
- *BOOT-SW-RFD-001, 002, 003*

Item identifier	Description
BOOT-SRC-SW	DPU Boot SW Source Code (including make/link files and any other files needed to build the SW) and Executable
BOOT-UT-SW	DPU Boot SW Unit Test Scripts/SW Source Code
HDSW-SRC-SW	DPU HW Driver SW Source Code (including make/link files and any other files needed to build the SW) and Binary Library
HDSW-UT-SW	DPU HW Driver SW Unit Test Scripts/SW Source Code
BOOT-VT-SW	DPU Boot SW Validation Test Scripts/SW Source Code
HDSW-VT-SW	DPU HW Driver SW Validation Test Scripts/SW Source Code
PSEC-HW-HW	DPU Processor Section Prototype Hardware

The common DPU

DPU – [Prototype] block diagram



CPU

- GR712RC dual LEON3FT
- Clock freq. 20..100MHz

Memory

- PROM: 32KiB
- MRAM: 2 or 8 MiB
- SRAM: 4, 8, 16 or 32 MiB
- SDRAM: 256 MiB

SpaceWire

- Redundancy: 1 or 2 links
- Link speed: 40 or 100Mbps

Instrument specific companion FPGA/ASIC

- Memory mapped I/O
- SpW RMAP

Key EEE components

Dual LEON3-FT (CPU)

- GR712RC
- Total dose: 300 kRad (Si)/106 MeV/cm2/mg
- 240-pin CQFP package

SRAM (working memory)

- UT8R4M39,UT8R2M39,UT8R1M39
- 100 krad(Si), SEL Immune: <110 MeV-cm2/mg, SEU error rate = 7.3x10-7 errors/bit-day
- 32-bit data, 7-bit BCH EDAC

SDRAM (working memory)

- UT8SDMQ64M48 3.0-Gigabit SDRAM
- 100 krad(Si), SEL Immune 111 MeV-cm2/mg, SEU Event Rate: 1.3E-10 events/bit-day
- 64Mx48-bit, allows 16-bit Reed-Solomon EDAC
- Single configuration: 256MiB effective size

PROM (Boot memory)

- UT28F256LVQLE - 32KiB PROM
- Total dose: 1Mrad (Si),
  Onset LET: 40 MeV-cm2/mg,
  SEL Immune > 110 MeV-cm2/m

MRAM (Application Storage Memory)

- UT8MR2M8, UT8MR8M8
- Total dose: 1Mrad (Si),
  SEL Immune: 112 MeV-cm2/mg @125C
  SEU Immune: Memory Cell 112 MeV-cm2/mg @25C

SpW interface (TM/TC interface)

- Aeroflex UT54LVDS031LV/32LV
- Total-dose: 300 krad(Si) and 1Mrad(Si)
  Latchup immune (LET > 100 MeV-cm2/mg)
- Redundant SpW transceivers for SpW0/1

Performance & size

SRAM 4 MiB

- Max clock freq. 100MHz
- Max clock freq. without ws 40MHz
- 50MHz clock freq. with 1 ws

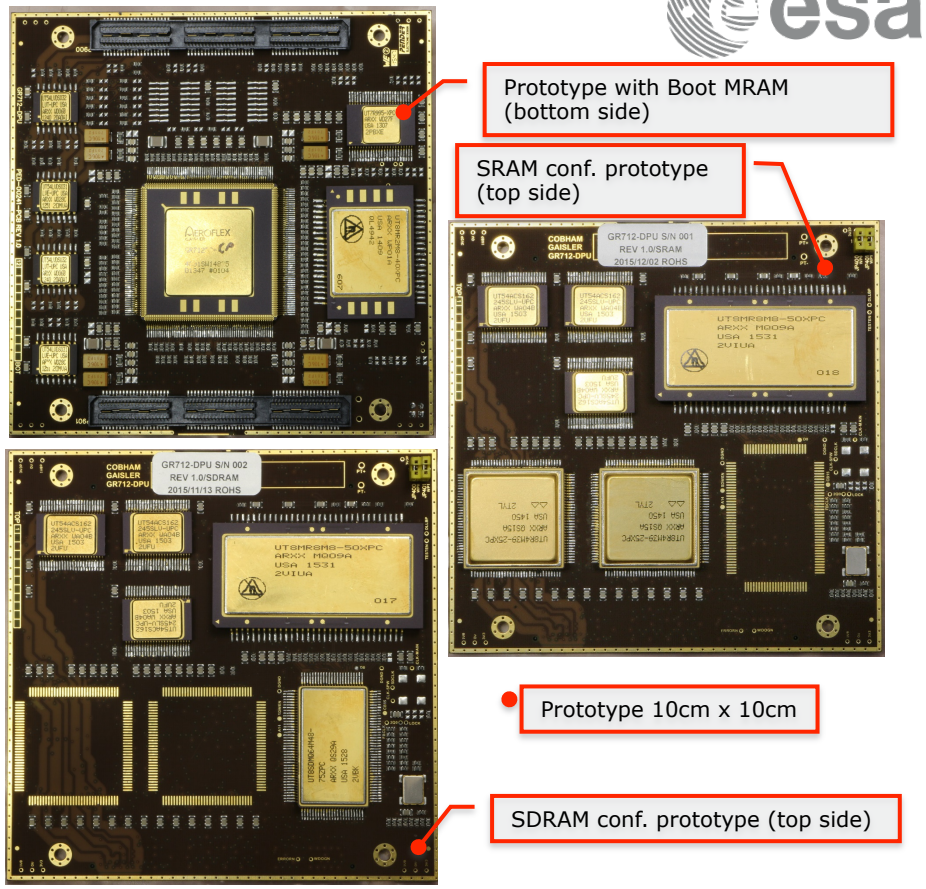
SRAM 32 MiB

- Max clock freq. 72MHz
- Max clock freq. without ws 29MHz
- 50MHz clock freq. with 2 ws

SDRAM 256 MiB

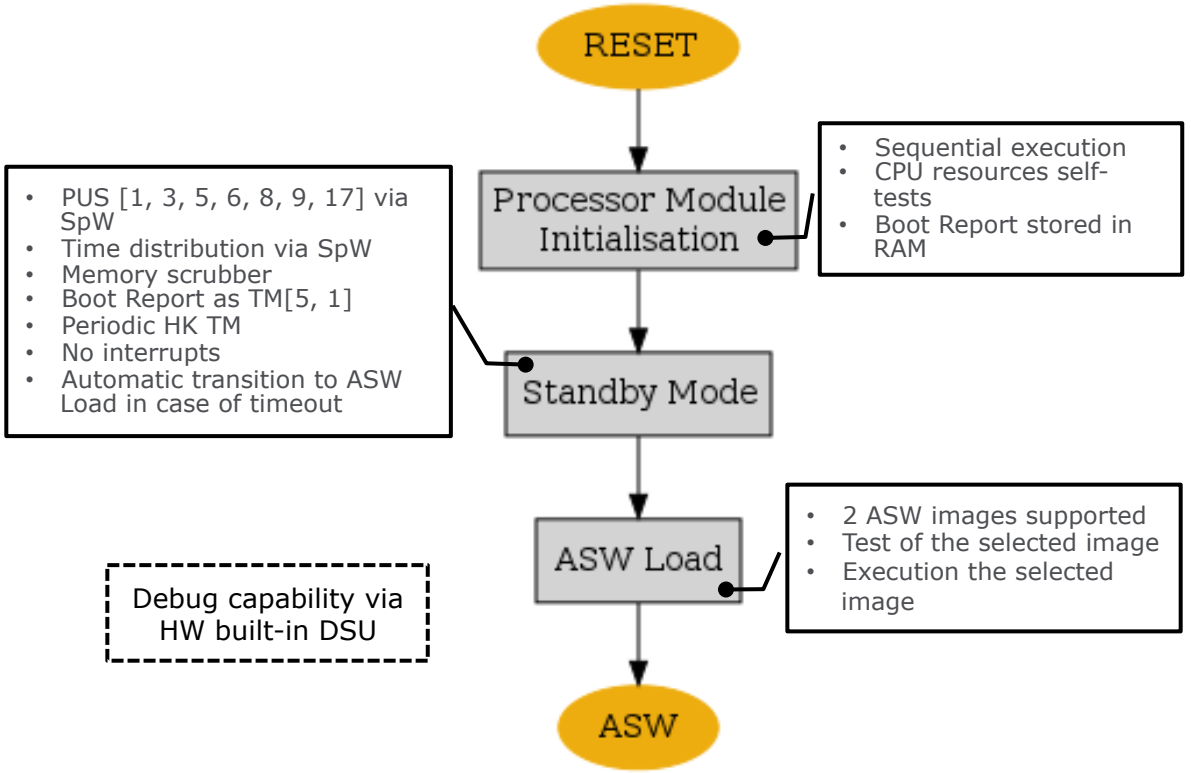
- Max clock freq. 44MHz

Data obtained from Hyperlinx simulations on prototype PCB → worst case, **conservative**



The common Basic Software

Boot & Standby Software

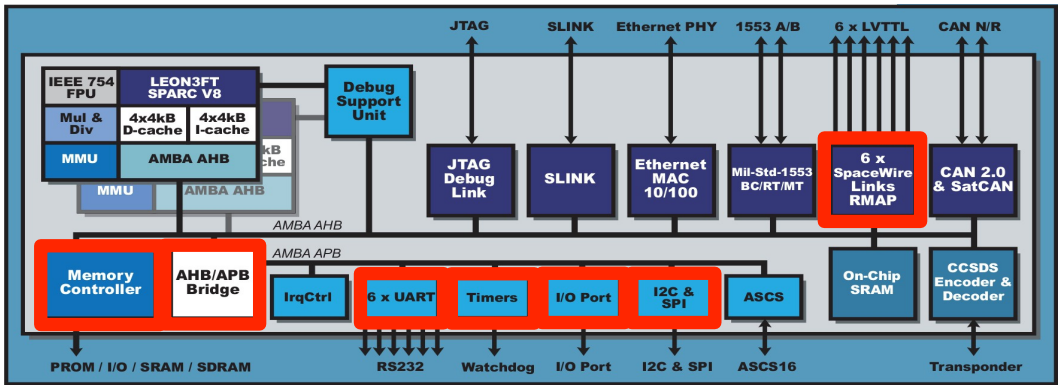


- SUN SPARC and Linux kernel coding style conventions
- GNU Make automatic build
- Statically allocated RAM
- No OS or externally developed SW
- Drivers SW common to the HW Drivers SW library
- Minimal CPU resource utilisation
  [no FPU, interrupts, IU mul/div]
- GR712RC internal device addresses hardcoded
  [no AMBA PnP]
- Unused GR712RC resources are disabled
  [clock gated]
- Instrument-specific parameters configurable at compile-time

Hardware Drivers Software

- Operating System Abstraction Layer (OSAL)
- Low level and callback functions

- Interfaces supported:
  - SPI
  - UARTs
  - SpaceWire
  - Timers
  - AHB status
  - Watchdog
  - Clock gating
  - Memory controller



- RTEMS 4.10 used for the HW drivers SW validation

Basic Software validation

SW Unit Tests

- GRMON2 and TSIM2
- Instruction code decision coverage on object files from TSIM2
- Unit test each component separately
- Fully automated test suite
- Code coverage also available with GRMON2

→ 98% code coverage on unit-tested code

→ 15-20% of the code tested by validation instead

SW Validation Tests

- GRMON2 and GRESB
- TCL scripting and GRMON2 scripting
- Unit test each component separately
- Fully automated test suite
- Test suite also ported to S/C Interface Simulator (SIS)

→ Black box tests checking TM

→ White box tests checking internal registers or traces with GRMON2

Lessons learned and conclusions

Results

- Despite the initial skepticism, **7/8 out of 12 JUICE units** use the provided DPU design and/or Basic SW
- **Test suite** developed by ESA/Airbus for the DPU/Boot SW is used as basis for the **instruments Full Functional Tests** (FFT)
- **Uniform, efficient and effective support** to the instruments thanks to the common design and SW
- **Uniform OBC-instrument TM/TC interface** for basic PUS services
- Resources in the **PI teams focused** on SW **science and performance** requirements
- Instruments **EM deliveries** so far have only **minor delays**
- SW bugs discovered by a PI team are reported to all the teams and solution distributed to all at once using a shared GITLAB environment
- **Tools and SW test suites** developed for one instrument can be **shared with other teams** with small adaptation effort

- In comparison, PEP-Lo instrument not using the common DPU design is facing important cost and schedule overruns

Instr	DPU	Boot SW
GALA	**YES**	**YES**
JANUS	**YES**	**YES**
JMAG	**YES**	**YES**
MAJIS	**YES**	**YES**
PEP-Lo	NO	**YES**
PEP-Hi	NO	NO
RIME	NO	NO
RPWI	**YES**	**YES**
SWI	**YES**	**YES**
UVS	NO	NO
RADEM	**YES**	**YES**
HAA	NO	NO

Conclusions

- While in JUICE the common DPU and Basic SW were introduced after instruments selection (end of phase B1) and only recommended to the PIs for adoption, **future missions with multiple instruments should require the use of common DPU and Basic SW** since the early study phase.
- System engineering early effort can prevent the use of custom FPGA in favor of GR712RC built-in interfaces
- Developing HW and SW "products" in advance is key to safeguard instruments schedule

- Other instruments elements with commonalities could be studied for a similar common development, e.g.:
  - Power Supply Unit
  - ASICs for recurrent functions
  - Common IP cores for FPGAs
  - Common SW libraries