A NASA GN&C Viewpoint on On-Board Processing Challenges to Support Optical Navigation & Other Autonomous GN&C Critical Functions

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Presentation Overview

- Acknowledgements
- Introduction
  - Presentation Objective
  - Autonomous GN&C Drivers for High Performance On-Board Computing
- Some Current NASA Use Cases of Optical Navigation
  - OSIRIS-REx Asteroid Sample Return
  - Restore-L Spacecraft Servicing Example
  - Mars 2020 Entry, Decent, and Landing (EDL) Example
  - Europa Lander Example
- Two Current NASA On-Board Computing Solutions Paths
  - SpaceCube Reconfigurable Multi-Processor Platform
  - High Performance Computing (HPC) Technology Development Initiative
- Summary

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Ben Reed
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Introduction

Presentation Objective

Our objective is to provide our colleagues that are architecting, designing and developing the next generation of space qualified flight processors our view of the landscape from a big-picture purely GN&C view of the world. There is a critical need to modernize on-board computing capabilities to support higher levels of GN&C Autonomy. In our view improved spaceflight computing means not only enhanced computational performance, energy efficiency, fault tolerance, but also ***ease of programming, affordability, reconfigurability, and availability****.*
All in the right balance.

System-level autonomy will be required to enable multiple NASA missions: Autonomous GN&C provides the foundational situational awareness and mission management capabilities

What time is it? Where am I ? How do I maneuver to get to my destination?

Humans to Mars/Mars Moons (including surface mobility)

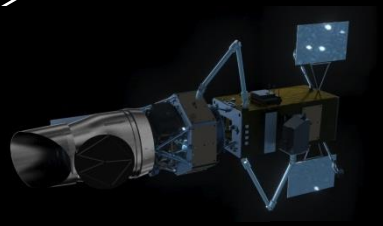
Human Exploration

Small Body Exploration

In-orbit Assembly

Supportive of Commercial Space Enterprises

Infrastructure Inspection and Maintenance

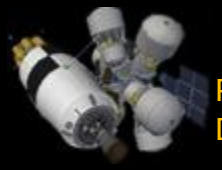


Science Observatory Servicing

Reduced Operations Burden for LEO Spacecraft

Lunar Exploration

Autonomous Space Systems Capability



Propellant Depot

Planetary Defense

Orbital Debris Mitigation

“Autonomy”: Where Does GN&C Fit?

Level 1

Level 2

Collaboration and Interaction	Situational/ Self Awareness	Reasoning and Acting	Engineering and Integrity
Knowledge and Intent Conveyance and Understanding	Sensing and Perception	Mission Planning	Verification & Validation
Prediction of Agents’ Behavior	State Estimation and Monitoring	Activity and Resource Planning	Test and Evaluation
Goal and Task Negotiation	Knowledge/ Model Building	Motion Planning	Operational Assurance
Operational Trust	Hazard Assessment	Execution and Control	Modeling and Simulation
	Event/Trend Identification	Learning and Adapting	Architecture and Design
	Anomaly Detection	Diagnosis and Prognosis	Communication Infrastructure
		Fault Response	

GNC

Partially GNC

Two Stretch Goals for Which Autonomous GN&C Will Be Required

Robotic Science Mission Stretch Goal:

- Capability for autonomous rendezvous, proximity operations, and scientific interactions (e.g. sampling) with unknown, uncharacterized and uncooperative natural body targets of interest at deep space distances without reliance on Earth support

Human Spaceflight Stretch Goal:

- Capability for autonomous in-space assembly and servicing of crewed vehicles, power and propulsion modules, long term habitats, multi-purpose space platforms in cislunar and deep space regimes

Building Autonomous GN&C Capabilities will Enable Robust and Reliable NASA Science and Exploration Missions Anytime/Anywhere

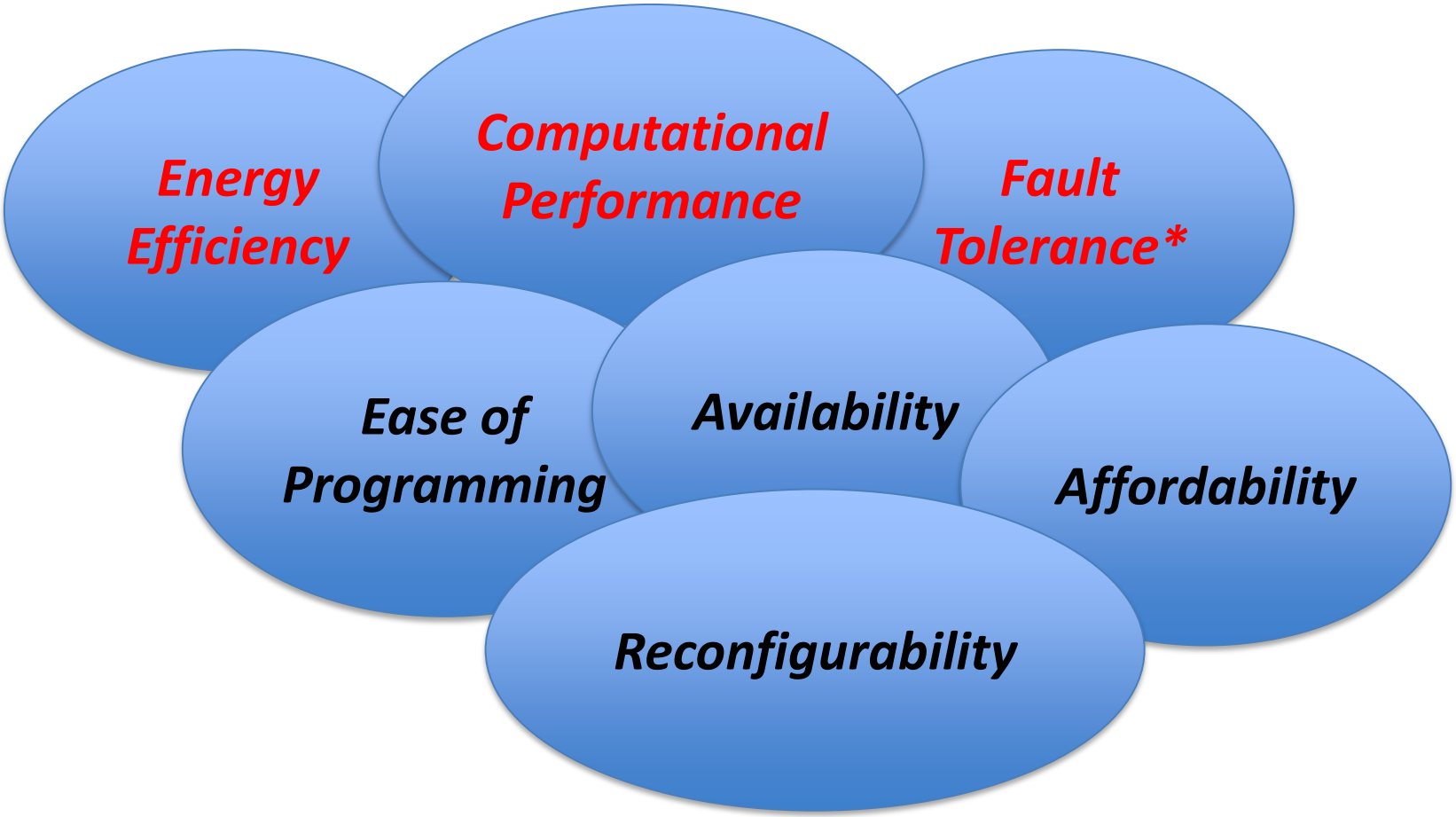
High Performance On-Board Computing is Required for this level of envisioned Autonomous GN&C Functionality

Selected Critical Functional Elements of Autonomous GN&C

- **Sensor Technologies (Inertial, Optical, RF (e.g., GNSS), etc.)**
- **Onboard Realtime System State Estimation**
- **Onboard Multi-Sensor Data Fusion**
- **Onboard Navigation (both relative and absolute)**
  - Terrain-Relative Navigation
  - Hazard Detection and Avoidance (HDA)
- **Onboard Optimization for path/trajectory planning**
- **Agile maneuvering**
- **GN&C Fault Management**
- **Embedded vehicle/component sensors and instrumentation (and associated data processing algorithms) for vehicle/subsystem health monitoring**
- **GN&C Diagnostics/Prognostics for onboard trending and health/performance situational awareness**
- **End-to-End Simulation and Modeling**
- **Autonomous GN&C System Verification and Validation Testbed Development**
- **Next-Generation Actuator Technologies**

High Performance On-Board Computing is Required for Executing these Autonomous GN&C Functions

Key Factors that All Need to be Balanced for a Next Generation Flight Processor



* Radiation tolerance/radiation hardness is included here

Performance vs Power Space Has Been Surveyed for CPU, DSP and FPGA based Processors

This excellent study has provided insights into the flight processor architectural trades between CPUs, GPUs, DSPs, and FPGAs

Table 1 CPU-based processors for space with rad-hard (RH) and rad-tolerant (RT) devices

Device	Process node	CPU frequency	DMIPS	Power dissipation	Radiation tolerance
			PowerPC		
RT RAD750 (BAE Systems)	0.25 μm radiation-tolerant	110–130 MHz	260 at 133 MHz (80 MFLOPS)	14 W at 133 MHz	TID: 200 krad (Si); SEU: $<1.6 \cdot 10^{-10}$ err/bitday; latch-up immune
RH RAD750 (BAE Systems)	0.15 μm radiation-hardened	200 MHz	400 at 200 MHz	14 W at 133 MHz	TID: 1 Mrad (Si); SEU: $<1.6 \cdot 10^{-10}$ err/bitday; latch-up immune
SCS750 SBC (3 PPC750FX) (Maxwell)	0.13 μm SOI (TRP)	400–800 MHz	1800 at 80 (200 at 400		
RAD5545 64-bit four-core (BAE Systems)	45 nm SOI	TBD	5200 MS (3700 MFL		
			Hardcore LEO		
AT697E SPARC V8 (Atmel)	0.18 μm CMOS	100 MHz	86 at 100 M		
TSC695F SPARC V7 (Atmel)	0.50 μm SOI	10–25 MHz	20 at 25 M		
GR712RC dual-core SOC (RamonChip)	180 nm CMOS	100 MHz	140–200 D (200 MFL		
			Softcore LEON		
GR-PCI-XC5 V SPARC V8	65 nm	50 MHz	70 DMIPS (50 MFLOPS)	TBD	RH by design (Virtex5QV tolerance)
LEON3FT-RT3PE on RT ProASIC3 (Gaisler, Actel)	130 nm	20–25 MHz	20 DMIPS	0.2 W	TID: 15–25 krad (Si); SEU: >6 (MeV · cm^2)/mg;
P4080 Board Intel Atom TMR board High reliable processor board (Airbus, SPARC V8 LEON4, Virtex-5 I/O, PikeOS) GR740 (four-core LEON4FT+2 FPU) OCE E698PM (RH, four-core 32-bit SPARC v8, MAC/UMAC DSP 64-bit double precision FPU)					

Table 2 DSP-based processors (space-grade and COTS)

Device	Process node, nm	CPU frequency	Power dissipation, W	DMIPS, GFLOPS	Radiation tolerance
MPPB/SSDP (TAS-I and Recore, LEON2 + 2/4 Xentium DSPs)	90	80 MHz	1.5 (min)	TBD	TBD
TI SMV320C6727B (C67x + single-core VLIW DSP)	130	250 MHz	TBC	1.5	TID 100 krad (Si) and SEL immune up to LET = 117 (MeV · cm^2)/mg
TI 66AK2H12 SOC (four-core ARM Cortex-A15 + eight-core C66x DSP)	28	1.4 GHz	10	160	Commercial device, not characterized for radiations
MACSPACE RC64 Manycore (GR712RC dual-core LEON3 + 64x CEVA X1643 DSP cores)	65	300 MHz	10	38	Targeting space (300 krad TID and SEL immune)

Table 3 FPGA-based processors (space-grade and COTS)

FPGA	Logic	Memory	DSPs	Power	Technology	Radiation tolerance
Xilinx Virtex-5QV	81,920 LUT6	596 RAMB16	320	5–10 W	65 nm SRAM	SEE immune up to LET 100 MeV/(mg · cm^2) and 1 Mrad (Si) TID
Microsemi RTG4	151,824 LE	5.3 Mbit	462	1–4 W	65 nm flash	SEE immune up to LET 110 MeV/(mg · cm^2) and TID > 100 krad
Microsemi ProASIC3	35,000 LE	0.5 Mbit	— —	~2 W	130 nm flash	40 krad TID
Microsemi RTAX	4 million gates (~37,000 LUT)	0.5 Mbit	120	TBD	150 nm antifuse	SEL immune up to 117 MeV/(mg · cm^2) and 300 krad TID
ATMEL ATFEE560	560,000 gates (28,800 LUT4)	0.23 Mbit	— —	TBD	180 nm SRAM	SEL immune up to 95 MeV/(mg · cm^2) and 60 krad TID
NanoXplore NG-MEDIUM	34,272 LUT4	56 RAMB48	112	TBD	65 nm SRAM	SEL immune at 60 MeV/(mg · cm^2) and 300 krad TID
Xilinx Zynq7000 SOC	277,400 LUT6	1510 RAMB18	2020	3–6 W	28 nm SRAM	Not space-qualified
Microsemi SmartFusion2 SOC	146,124 LE	4.5 Mbit	240	~2 W	65 nm flash	Not space-qualified
Xilinx Zynq Ultrascale+ SoC	523,000 LUT6	70.6 Mbit	1968	TBD	16 nm SRAM	Not space-qualified

From Reference 3, George Lentaris, et al

Some Current NASA Use Cases of Optical Navigation

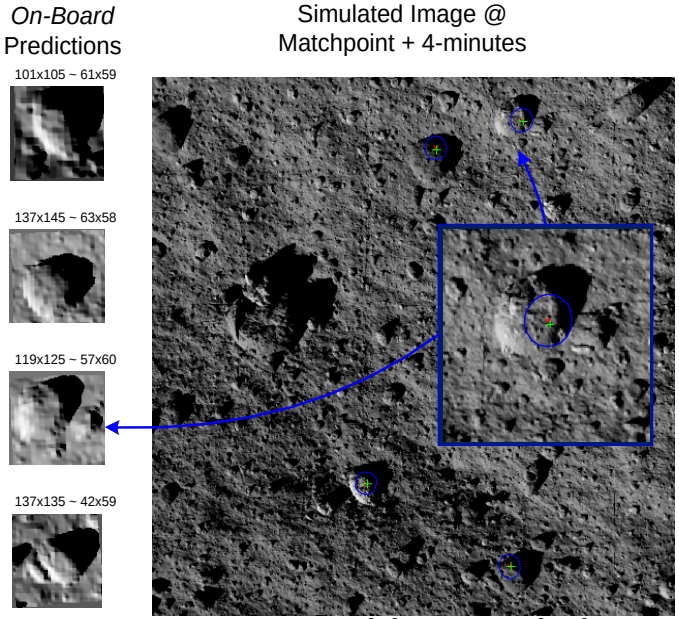
OSIRIS-REx/Restore-L

Mars 2020/Europa Lander

OSIRIS-REx Mission Example

- Natural Feature Tracking (NFT) capability added late (at CDR) as an alternative, dissimilar, autonomous navigation system to serve as risk mitigation for the baselined GN&C Lidar relative navigation sensors which experienced hardware development challenges
- NFT is an onboard optical navigation system that compares observed images to a set of asteroid terrain models which are rendered in real-time from a catalog stored in memory on the flight computer.
- NFT can perform the necessary autonomous navigation functions in support of Touch and Go (TAG) maneuver
- Was fortunate that the NFT flight software algorithms were able to be accommodated in the baseline OSIRIS-Rex flight computer
- However only 3-4 NFT images can be processed in last few seconds prior to contacting the Bennu asteroid surface due to flight processor computational constraints

OSIRIS-Rex Spacecraft at Bennu



NFT Feature Matching Depiction

RESTORE-L Mission Example

- Restore-L mission objective is to service (Re-Fuel) the Landsat-7 spacecraft
- Requires high-performance on-board processing capabilities to perform autonomous optical sensor based Relative Navigation (RelNav) functions to enable autonomous rendezvous and proximity operations
- This mission presents the challenge of running complex realtime vision processing algorithms and robot motion control algorithms
- Developing methods to parallel process algorithms to accelerate hardware
- Technologies that make it possible:
  - Relative Navigation Sensor suite (Visible/Infrared cameras and Lidar sensors)
  - Relative Navigation Algorithms (range, bearing, pose estimation)
  - **SpaceCube processor**

Restore-L Servicing Spacecraft in Proximity Operations with the Landsat-7 Client Spacecraft

Even with the relatively high performance SpaceCube accommodating the Restore-L RelNav functions such as GNIFR and FPOSE is challenging. Low margins for these applications.

What do OSIRIS-Rex and RESTORE-L Have in Common?

- **Both OSIRIS-REx and Restore-L employ optical relative navigation algorithms to estimate critical spacecraft dynamic state parameters**

- **Both have relatively slow, carefully planned step-by-step mission operations cadence at critical event times which is completely unlike Mars/Planetary Entry Descent and Landing (EDL) operations**

- **Both have built-in contingency and safe abort options allowing for multiple engagements with the asteroid Bennu (OSIRIS-REx) and the Landsat-7 client (Restore-L). Trouble shooting work can be performed in a safe state in between critical engagements.**

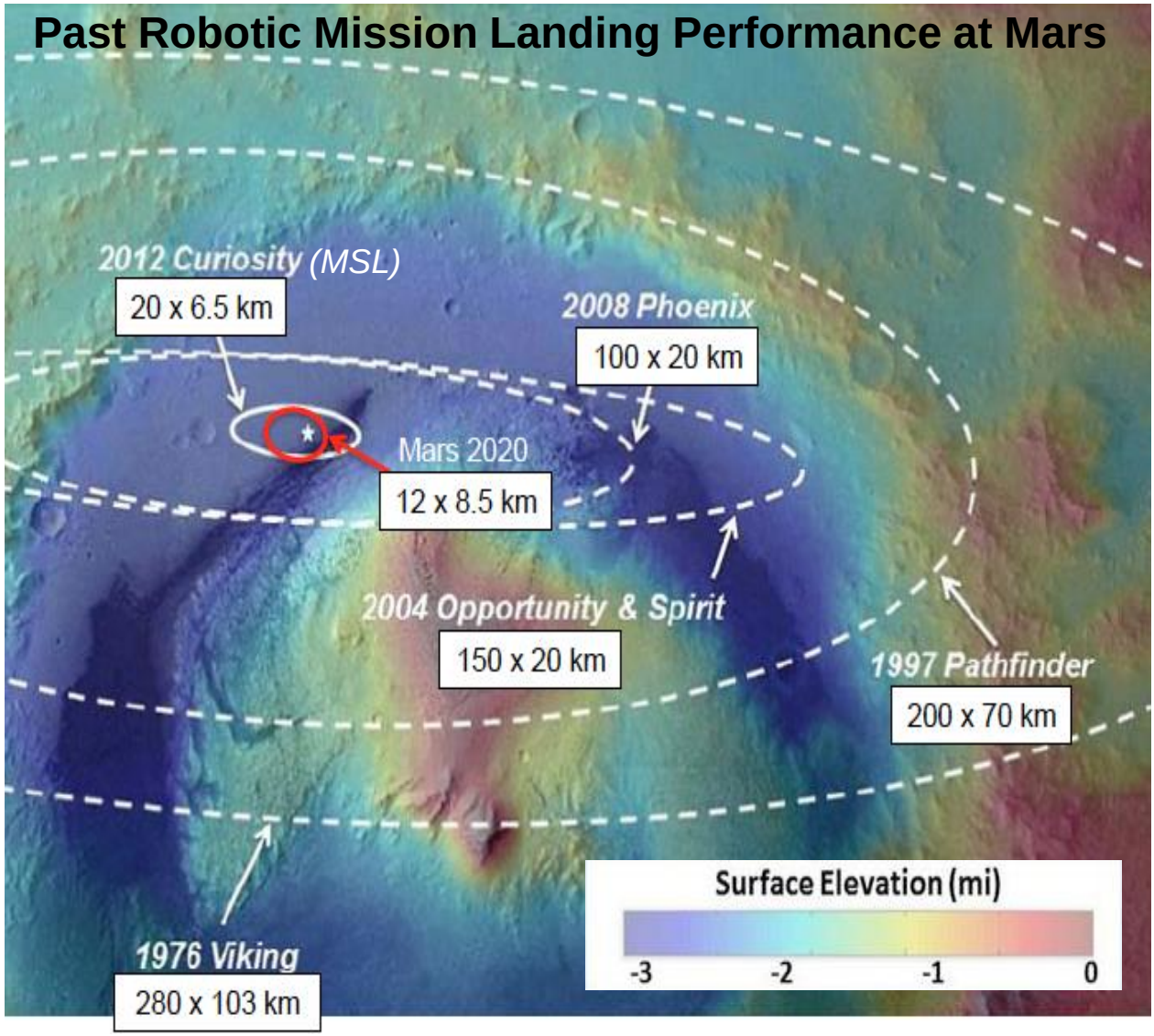
These types of missions are therefore not ultimate drivers for advanced on-board High Performance Computing (HPC) capability in the way that Mars/Planetary EDL is. These types of missions will however benefit from HPC advancements.

The Need: Future Human Mars Missions

Landing Precision Requirements:

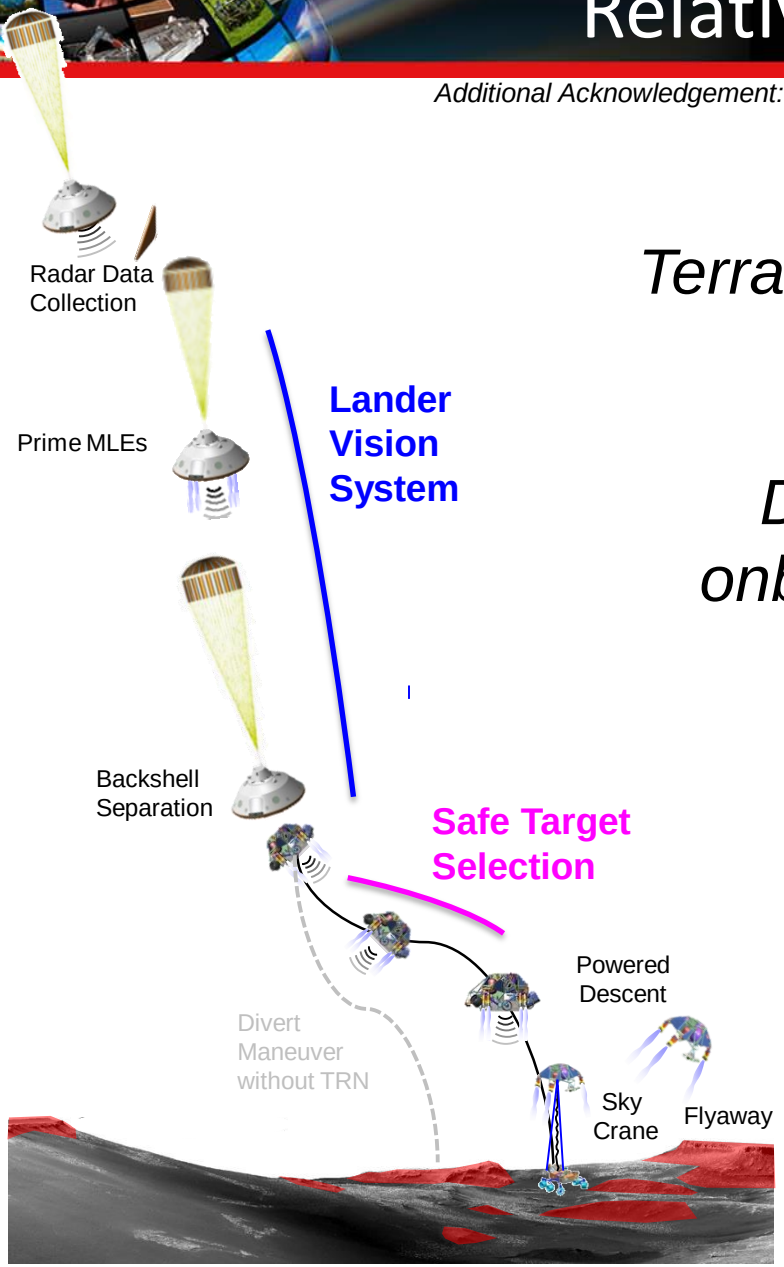
	MSL	Human Mission
Payload (t)	1	20
Landing Footprint (km)	20 x 6.5	0.05 x 0.05
Landed Altitude* (km)	-4	0

* relative to Mars Orbiter Laser Altimeter (MOLA) Elevation Model



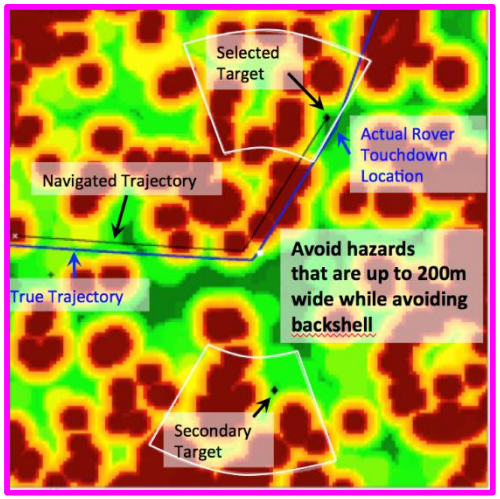
Mars 2020 Terrain Relative Navigation (TRN)

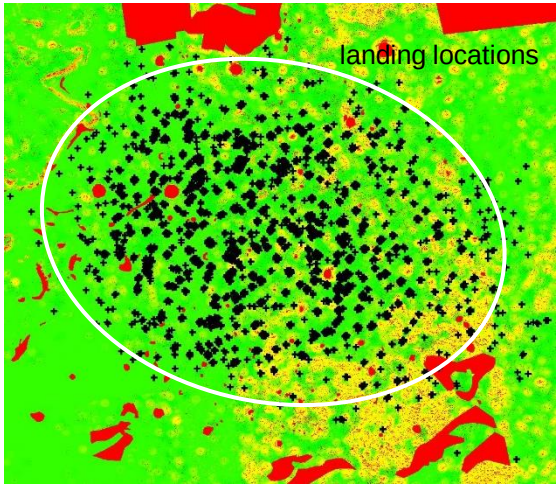
Additional Acknowledgement: Seth Aaron, Hugh Ansari, Paul Brugarolas, Jordi Casoliva, Andrew Johnson, Swati Mohan, Jim Montgomery, Nik Trawny, Geoff Vaughan, others



Terrain Relative Navigation (TRN) used to select safe landing site

Descent images are correlated to onboard map constructed from orbital reconnaissance imagery





Mars 2020 Lander Vision System (LVS)

Descent Stage

Descent IMU

Descent IMU

422

422

Descent Motor

Control Assembly

422

422

M2020 flight HW
M2020 flight SW
LVS flight HW
LVS flight SW
LVS firmware
data

5/8" Cutter

422

Y

422

Y

IMU data

RAD-750 CPU + FPGAs

422

422

Rover Compute Element

EDL/GNC FSW w/ Safe Target Selection

Safe Target Map

s/c state, cmds

positions, tlm

Rover 1553

LVDS (ITC/ICC)

Vision Compute Element

VCE FSW

IP firmware

LVS map

cmds

images

LVDS

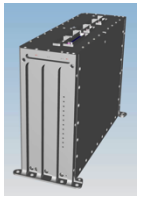
+5V

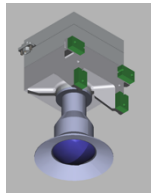
Rover

LVS Camera

Rover Power

28V





JPL adopted a "Bolt-on" LVS architecture to minimize impact to Flight System Computer

Vision Compute Element FPGAs

- **HK FPGA (Housekeeping)**
  - Burn once RTAX 2000
  - Design and V&V complete
  - FPGA installed on flight CVAC
- **VP-E FPGA (Vision Processing – EDL)**
  - Reprogrammable Virtex-5 (SIRF)
  - Design and verification complete
  - Final Design Review complete
  - Implemented image processing optimizations to speed up LVS time-line
    - Normalize Image: 1660 MIPS, 20ms/image
    - Feature Selection: 7025 MIPS, 4ms/image
    - FFT Correlation: 5187 MIPS, 740ms/image
    - Image Warp: 3550 MIPS, 134ms/image
    - Spatial Correlation: 6775 MIPS, 457ms/image

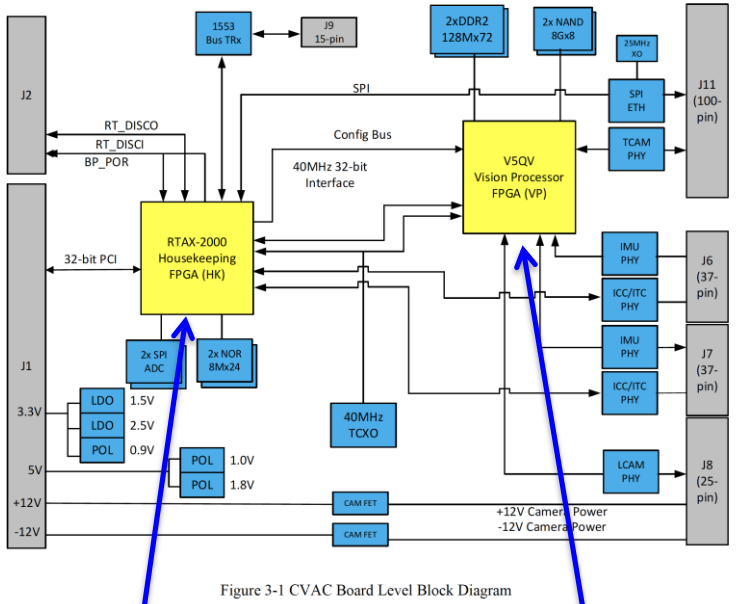
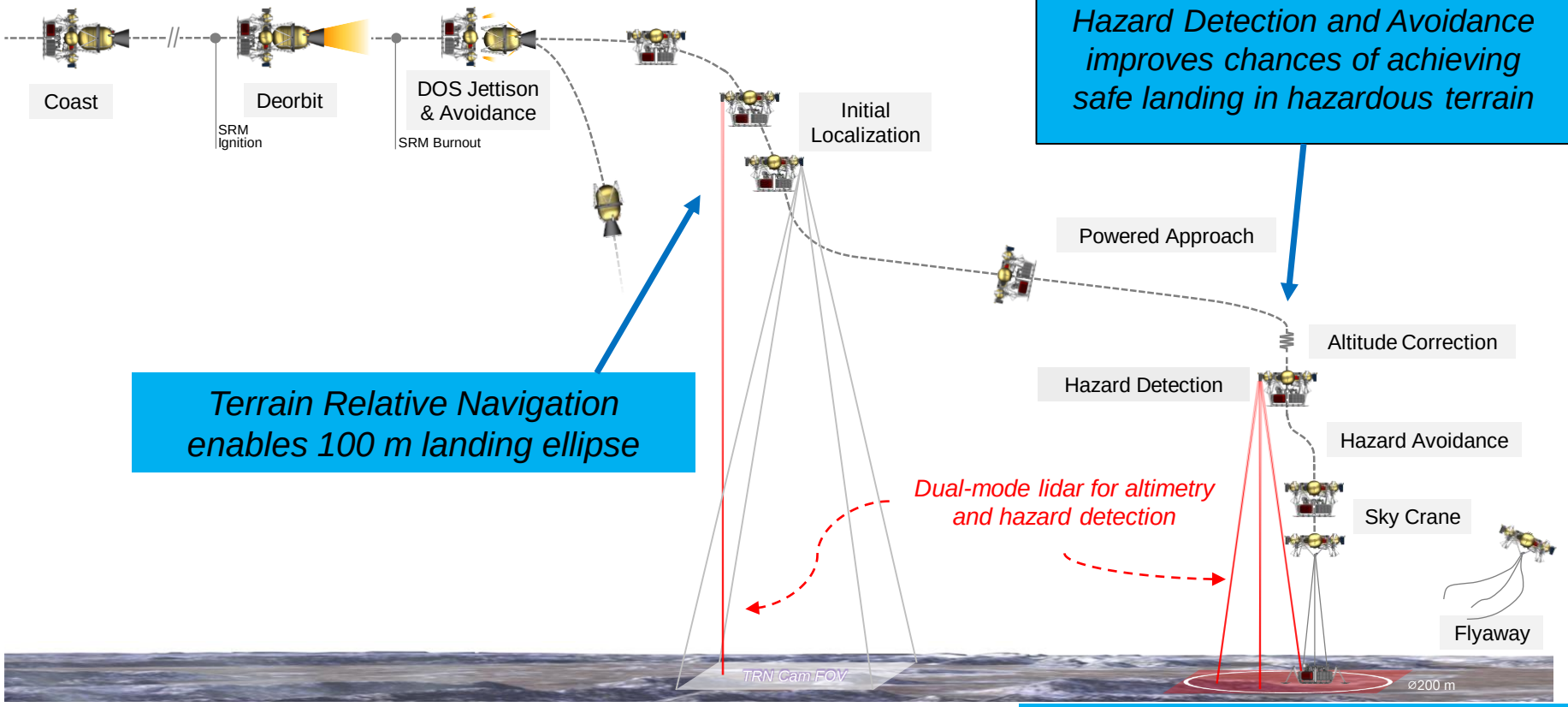


Figure 3-1 CVAC Board Level Block Diagram

HK FPGA (RTAX2000)
- Time sync
- VP configuration
- NOR memory
- 1553
- ICC/ITC
- ADC
- Ethernet

VP-E FPGA (Virtex5)
- DDR2 memory
- NAND memory
- Image Processing
- LCAM interface
- IMU interface

Europa Lander Concept: Deorbit, Descent and Landing Architecture

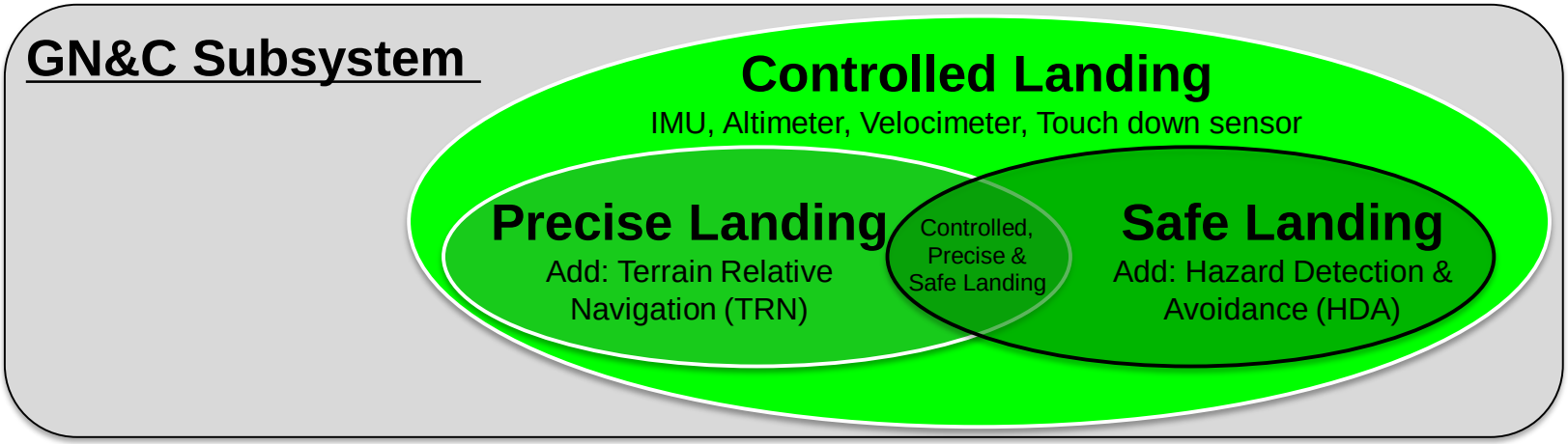


Hazard Detection and Avoidance improves chances of achieving safe landing in hazardous terrain

Terrain Relative Navigation enables 100 m landing ellipse

Sky Crane architecture minimizes site alteration and contamination

Envisioned Evolution of GN&C Landing System Capabilities: Controlled => Precise => Safe



Controlled Landing

- Minimize vertical descent rate and lateral velocity to ensure a soft (or controlled) touchdown
- No knowledge of global position – "blind" landing

Precise landing – Terrain Relative Navigation (TRN)

- Global navigation through onboard matching of real-time terrain sensing data with *a priori* reconnaissance data
- Enables efficient maneuvering to minimize landing error and avoid large hazards identified in *a priori* analyses

Safe Landing – Hazard Detection & Avoidance (HDA)

- Real-time terrain sensing to identify sites safe from lander-sized hazards that are undetectable in *a priori* data
- Enables a hazard avoidance maneuver to the identified safe site
- Can be leveraged for subsequent Hazard Relative Navigation (HRN) – similar to TRN

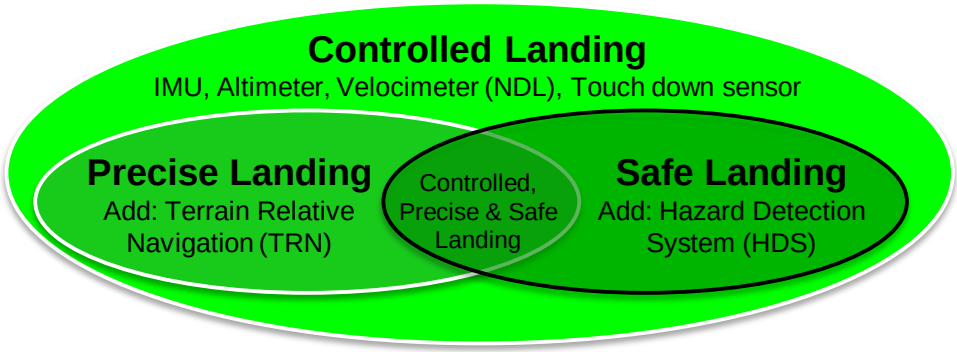
HPSC-based Avionics For Planetary Landing and Hazard Avoidance (PL&HA)

Status Quo for Landing GN&C

Controlled Landing
IMU, Altimeter, Velocimeter*, Touch down sensor

Future Capabilities Needed for PL&HA

(NASA EDL Technology Roadmap)



TRL Objectives	Existing TRL	TRL Plan
NDL – Controlled Landing	4/5 (via COBALT)	6
Multi-Mission HDS – Safe Landing	2	4
PL&HA HSPC-based Avionics	2	4
6DOF PL&HA G&N Algorithms	2	5/6

Two Current NASA On-Board Computing Solutions Paths

SpaceCube

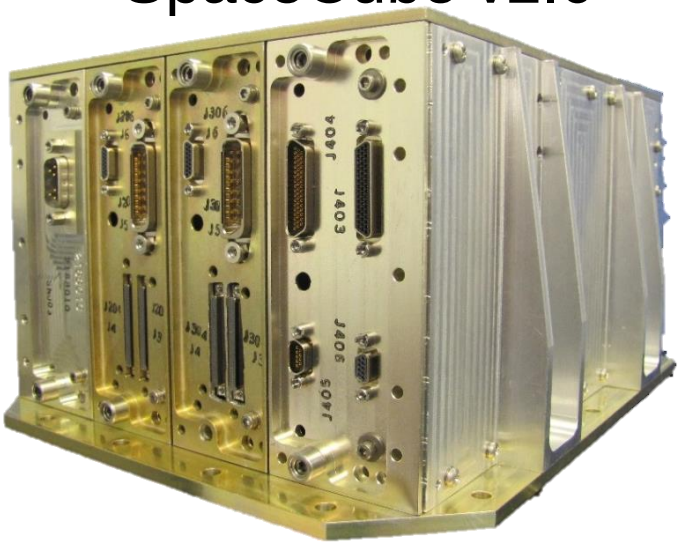
High Performance Spaceflight Computing (HPSC) Technology Development

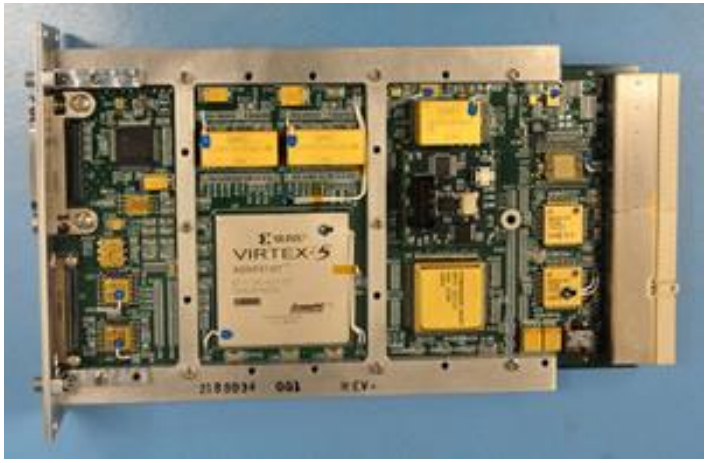
NASA's SpaceCube

- **Small, light-weight, reconfigurable multi-processor platform for space flight applications demanding extreme processing capabilities**
- **Hybrid processing using FPGA, CPU, DSP computing nodes with hardware accelerated computing**
- **Currently TRL-7**
- **Leverages 10 years of design heritage and operation experience**
- **Baselined as Payload Control Computer (PCC) on Restore-L spacecraft to run complex vision processing algorithms and robot motion control algorithms in real time**

Reference:
https://spacecube.nasa.gov/Introduction.html

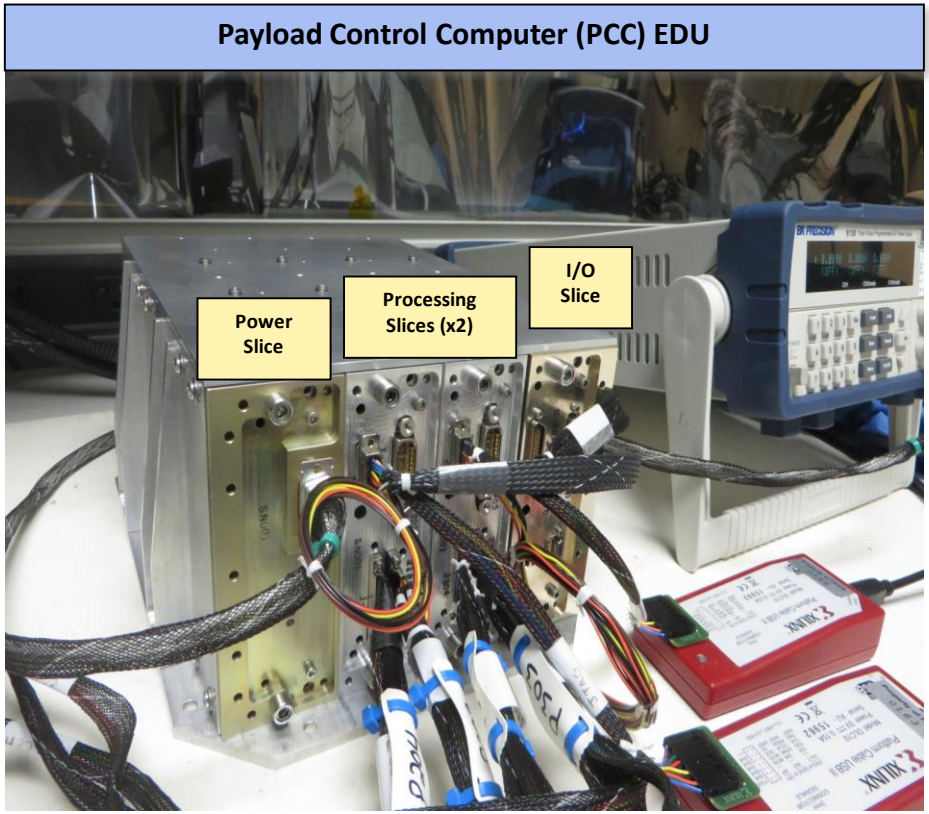
SpaceCube v2.0





SpaceCube v2.0 Processor Card

Restore-L Payload Control Computer (SpaceCube)



The PCC enables blended FPGA / FSW system-on-a-chip solutions to facilitate advanced on-board Restore-L payload data processing and control.

High Performance Spaceflight Computing (HPSC) Overview

- The goal of the HPSC program is to dramatically advance the state of the art for spaceflight computing
- HPSC will provide a nearly two orders-of-magnitude improvement above the current state of the art for spaceflight processors, while also providing an unprecedented flexibility to tailor performance, power consumption, and fault tolerance to meet widely varying mission needs
- These advancements will provide game changing improvements in computing performance, power efficiency, and flexibility, which will significantly improve the onboard processing capabilities of future NASA and Air Force space missions
- HPSC is funded by NASA's Space Technology Mission Directorate (STMD), Science Mission Directorate (SMD), and the United States Air Force
- The HPSC project is managed by Jet Propulsion Laboratory, and the HPSC contract is managed by NASA Goddard Space Flight Center (GSFC)

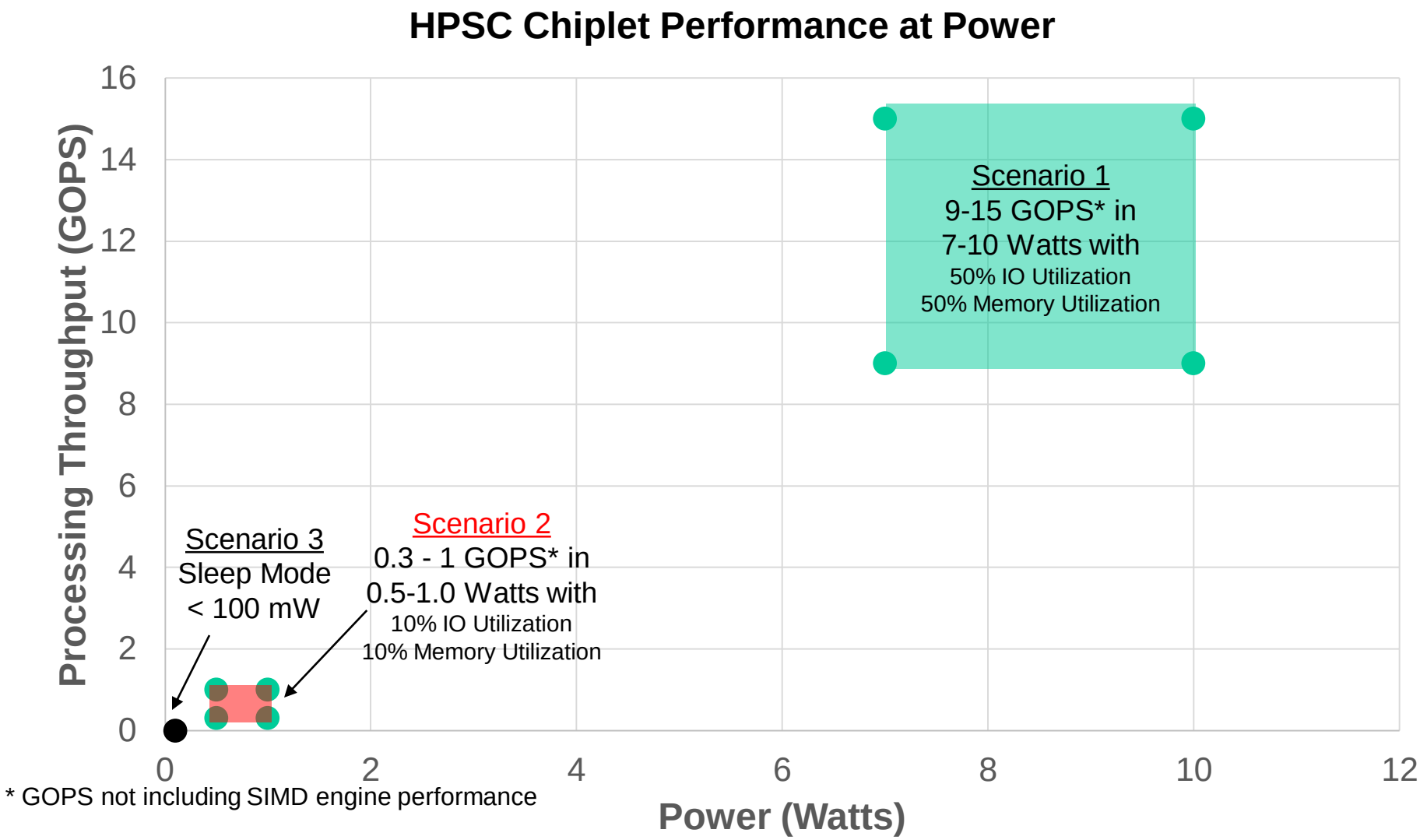
From Reference 4, W. Powell

Key Requirements Summary

Processor Cores	• HPP Subsystem: 8 ARM 64-bit Cortex-A53 cores with floating point & Single Instruction Multiple Data (SIMD) engine. Performance & power on next slide. • Realtime Processing Subsystem (RTPS) with single A53 and dual Cortex-R52 cores
Memory Interfaces	• 3 DDR3/4: 2 for A53 clusters, 1 for RTPS • 4 SRAM/NVRAM • Enhanced error correction (ECC) to operate through bit upsets and whole memory device failures
IO Interfaces	• 6 SRIO 3.1, 2 PCIe Gen2 serial IO • Ethernet, SpaceWire, TTE, SPI, UART, I^2C, GPIO
Power scaling	Able to dynamically power down/up cores, subsystems, & interfaces via software control
Fault tolerance	Able to autonomously detect errors & log errors, prevent propagation past established boundaries, and notify software
Trust & Assured Integrity	• DMEA-accredited Trusted supply chain • Free of malicious insertions / alterations
Temperature	-55C to 125C

From Reference 4, W. Powell

Performance @ Power Requirements



* GOPS not including SIMD engine performance

From Reference 4, W. Powell

HPSC Program Chiplet Development Approach

- **Develop Chiplet using Boeing's RHBD 32nm SOI design & fabrication flow, which provides:**
  - High-performance library and mixed-signal macros
  - Strategic radiation hardness
  - Single-Event-Effects (SEE) mitigations optimized for power efficiency
  - Assured integrity
- **Employ core competencies of team comprised:**
  - Boeing Solid-State Electronics Development (SSED)
  - Boeing Secure Computing Solutions (SCS)
  - Boeing Space & Launch
  - USC Information Sciences Institute (ISI)
  - University of Michigan ARM Research Center
- **Utilize silicon-proven IP:**
  - ARM, Globalfoundries, Synopsys, Praesum, and Uniquify
- **Leverage tens of millions of dollars of Government and Boeing investments in related technology areas:**
  - DTRA RHBD3, AFRL/NASA NGSP, MAESTRO, DARPA PERFECT, etc.

From Reference 4, W. Powell

HPSC Use Cases: Rovers and Landers

Lander

Compute Needs
- Hard Real time compute
- High rate sensors w/zero data loss
- High level of fault protection/ fail over

- **System Metrics**
- >10 GOPs compute
- 10Gb/s+ sensor rates
- Microsecond I/O latency
- Control packet rates >1Kpps
- Time tagging to microsecond accuracy

The "Lander" is the driving Use Case for HPSC.

The HPSC architecture studies have leveraged Hazard Detection algorithms from NASA's ALHAT Project as benchmarks for future NASA mission computing needs and the development of the HPSC specifications.

From Reference 4, W. Powell

HPSC Use Cases: Rovers and Landers

Rover

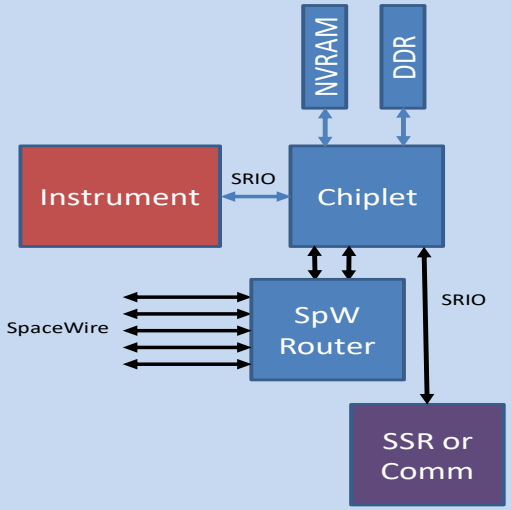
Compute Needs
- Vision Processing
- Motion/Motor Control
- GNC/C&DH
- Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault detection/recovery

- **System Metrics**
- 2-4 GOPs for mobility(10x RAD750)
- >1Gb/s science instruments
- 5-10GOPs science data processing
- >10KHz control loops
- 5-10GOPS, 1GB/s memory BW for model based reasoning for planning

Smallsat

Compute Needs
- Hard and Soft real time
- GNC/C&DH
- Autonomy and constellation(cross link comm)
- Sensor data processing
- Autonomous science

- **System Metrics**
- 2-5Gbps sensor IO
- 1-10GOPs
- 1GB/s memory bandwidth
- 250Mbps cross link bandwidth



From Reference 4, W. Powell

Summary

Summary (1 of 2)

- Improved spaceflight computing means not only enhanced computational performance, energy efficiency, and fault tolerance but also ease of programming, reconfigurability, affordability and availability. All in the right balance.

- NASA has and is currently finding ways to perform Optical Navigation (e.g. Mars 2020 TRN) with the available State-of-the-Art flight computing resources

- Critical need to modernize on-board computing capabilities to support higher levels of GN&C Autonomy.
  - Not only for Optical Navigation but other autonomous functions such as on-board trajectory optimization, agile maneuvering, and fault management, for example.

- NASA's SpaceCube and HPSC technologies will enable new mission concepts and capabilities for high-priority robotic science missions and simultaneously mature technologies critical to human Mars missions
  - The HPSC-surrogate avionics for PL&HA applications will achieve TRL4 by FY2020 and be ready for rapid infusion of the upcoming HPSC

Summary (2 of 2)

- Collaboration would be fostered by establishing a set of common algorithmic* functional benchmarks (e.g. a generic pose estimation algorithm, hazard detection algorithm. or a TRN image processing algorithm) for use by both NASA and ESA in their respective studies of advanced high performance on-board computing technology

- Advancing the on-board high performance computing technology is more a driver for highly dynamic Mars/Planetary EDL than it is for Asteroid/Small Body encounters and Rendezvous/Proximity Operations applications, both of which operate at a slower pace

* Versus the typical algorithmic building blocks such as matrix multiplication, matrix addition, matrix convolution, etc.


Questions?

Some References

1) **Mission Use of the SpaceCube Hybrid Data Processing System**, David Petrick/NASA Goddard Space Flight Center/Code 587, Presentation at 2017 Military and Aerospace Programmable Logic Devices (MAPLD) Workshop, 22 – 25 May 2017
2) **https://spacecube.nasa.gov/Introduction.html**
3) **High-Performance Embedded Computing in Space: Evaluation of Platforms for Vision-Based Navigation,** George Lentaris, et al, Journal of Aerospace Information Systems, Vol. 15, No. 4, April 2018
4) **High-Performance Spaceflight Computing (HPSC) Project Overview**, Wesley Powell/NASA Goddard Space Flight Center/Code 560, Presentation at Radiation Hardened Electronics Technology (RHET) Conference, Phoenix, AZ, November 5-8, 2018
5) **Lessons Learned from OSIRIS-REx Autonomous Navigation Using Natural Feature Tracking**, David A. Lorenz, et al, Goddard Space Flight Center, 2017 IEEE Aerospace Conference
6) **The Restore-L Servicing Mission**, Benjamin B. Reed, Goddard Space Flight Center, Presentation to the NAC Technology, Innovation and Engineering Committee, 29 March 2016
7) **Benchmarking Analysis of Space-Grade Central Processing Units and Field-Programmable Gate Arrays,** Tyler M. Lovelly, et al, Univ. of Pittsburg, Journal of Aerospace Information Systems, Vol. 15, No. 8, August 2018

Acronym List

AFRL	Air Force Research Laboratory	GB/s	Gigabytes Per Second	RTOS	Real Time Operating System
AMBA	ARM Advanced Microcontroller Bus Architecture	GNC	Guidance Navigation and Control	S/C	Spacecraft
ASIC	Application Specific Integrated Circuit	GOPS	Giga Operations Per Second	SCP	Self Checking Pair
BW	Bandwidth	GSFC	Goddard Space Flight Center	SMD	Science Mission Directorate
CFS	Core Flight Software	HEOMD	Human Exploration and Operations Directorate	SpW	SpaceWire
CPU	Central Processing Unit	HPSC	High Performance Spaceflight Computing	SRAM	Static Random Access memory
C&DH	Command and Data Handling	JPL	Jet Propulsion Laboratory	SRIO	Serial Rapid I/O
DDR	Double Data Rate	KHz	Kilohertz	SSR	Solid State Recorder
DMR	Dual Modular Redundancy	Kpps	Kilo Packets Per Second	STMD	Space Technology Mission Directorate
DRAM	Dynamic Random Access memory	Mbps	Megabits Per Second	TTE	Time Triggered Ethernet
EEPROM	Electrically Erasable Programmable Read-Only Memory	MCM	Multi Chip Module	TTGbE	Time Triggered Gigabit Ethernet
FCR	Fault Containment Region	MRAM	Magnetoresistive Random Access Memory	TMR	Triple Modular Redundancy
FPGA	Field Programmable Gate Array	NASA	National Aeronautics and Space Administration	TRCH	Timing Reset Configuration and Health
FSW	Flight Software	NVRAM	Nonvolatile Random Access memory	XAUI	10 Gigabit Media Independent Interface)
Gb/s	Gigabits Per Second	PCB	Printed Circuit Board	VMC	Vehicle Management Computer

Backup

Status Quo Versus Precise & Safe Soft Landing (Enabled by HPSC)

Status Quo
(Blind Soft Landing)

Phases: Initial Entry (mission-dependent deceleration method) → Final Targeting Burn → Powered Descent → Terminal Descent → Landing Ellipse

Sensors: Radar Velocimeter; Altimeter; IMU

(Precise & Safe Soft Landing)

Phases: Initial Entry → Final Targeting Burn → Intelligent Powered Descent → Hazard Detection (Find Safe Site) → Local Divert → Terminal Descent → Precise Ellipse

Sensors: TRN; HDS; NDL (Velocimetry & Range); Altimeter; IMU

TRN: Global Position Knowledge
already baseline on Mars2020 and RP

HDS: local terrain knowledge
avoid hazards, other payloads or sample caches

NDL: Precise Velocity and Range
critical to soft landing and precise navigation

Advanced G&N Algorithms
precise state knowledge and intelligent maneuver logic