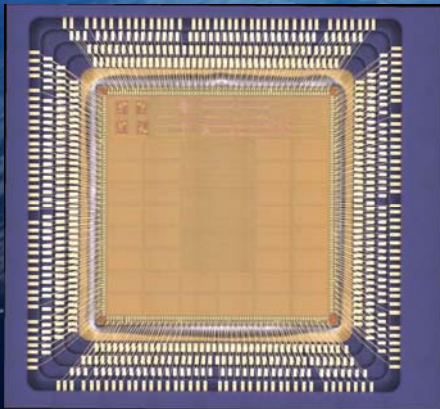# HPDP-40

High Performance Data Processor –
A New Generation Space Processor in
Demonstration
OBDP, ESTEC, February 25-27, 2019

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Constantin Papadas, Integrated Systems Development SA (ISD SA)

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- HPDP-40 Architecture / SW Development
- HPDP-40 Demo Kit
- HPDP-40 Test Status & Power Measurements
- Application Demonstrations
- HPDP-40 Chip Industrialisation
- Conclusion and Outlook

Introduction

Introduction

The development of **HPDP** has been initiated by the European Space Agency (ESA) and DLR to address the need for a flexible and re-programmable high performance data processor.

It is being implemented in the 65nm radiation hardened technology of ST Microelectronics (C65SPACE).

Key Advantages of HPDP-40 device:
- Ability to meet the increasing requirements of future payloads regarding flexibility, processing power and re-programmability
- Radiation robustness for all earth orbit and planetary exploration missions
- Low power consumption

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HPDP Architecture & Software Development Flow

HPDP-40 Architecture (1/2)

HPDP-40 implements the eXtreme Processing Platform (**XPP**), a runtime reconfigurable data processing engine developed by PACT XPP Technologies AG. XPP configuration:

- 40 ALU Processing Array Elements (16b) running at 250MHz
- 16 columns RAM blocks for memory
- 2 VLIW processor cores (FNC PAE) running at 125MHz
- Connected by a reconfigurable data and event network
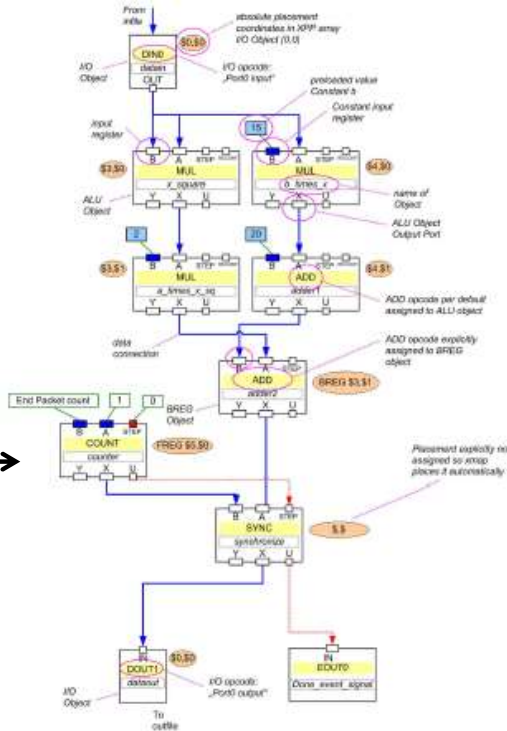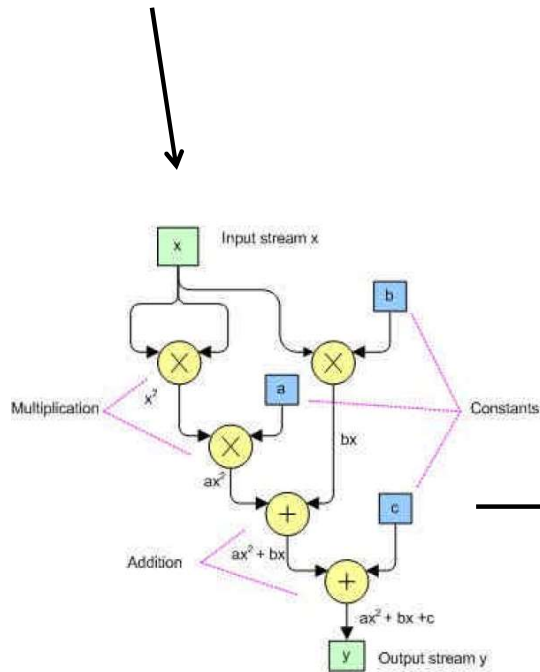
The device provides:

- 40Gops of arithmetic operations through parallelism
- 4x 1.1Gbps Streaming Ports
- >4 Mbyte on-chip SRAM
- Memory protections, Watchdog

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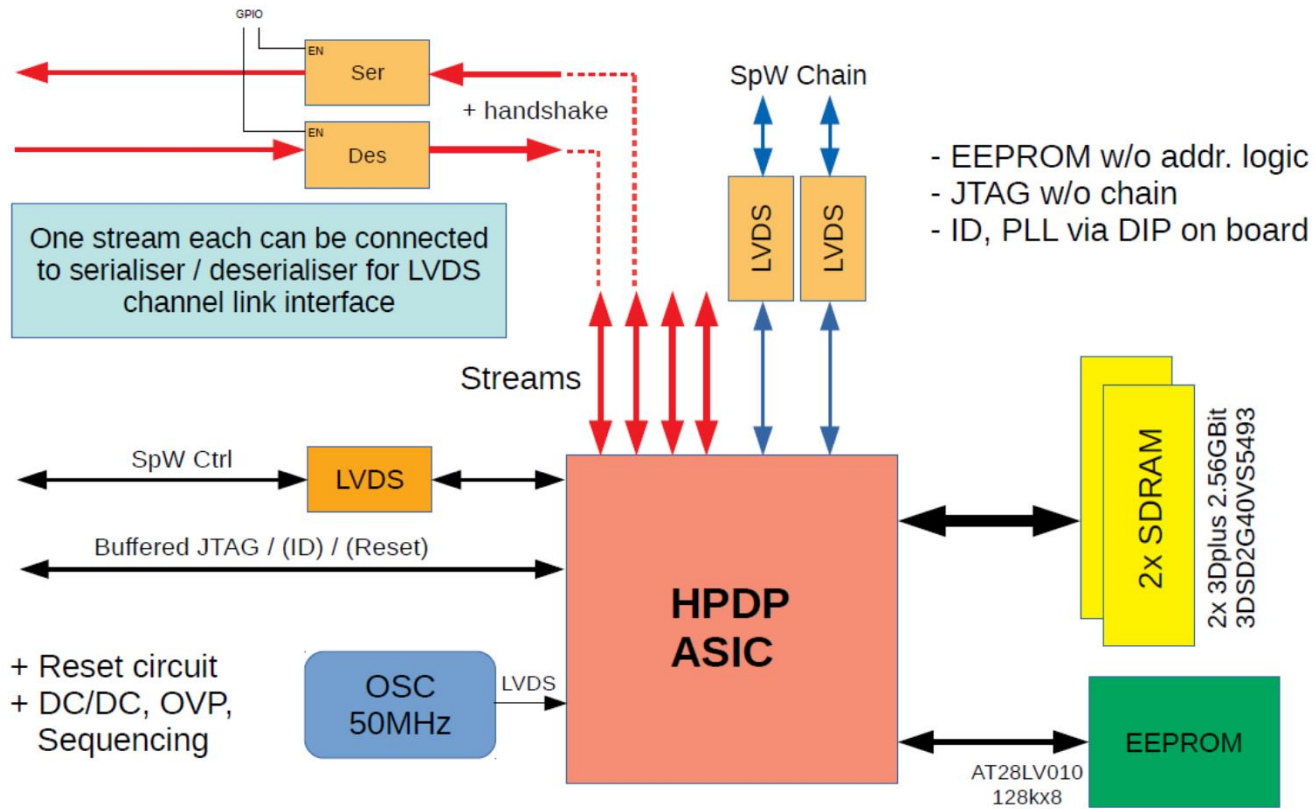
HPDP-40 Architecture (2/2)
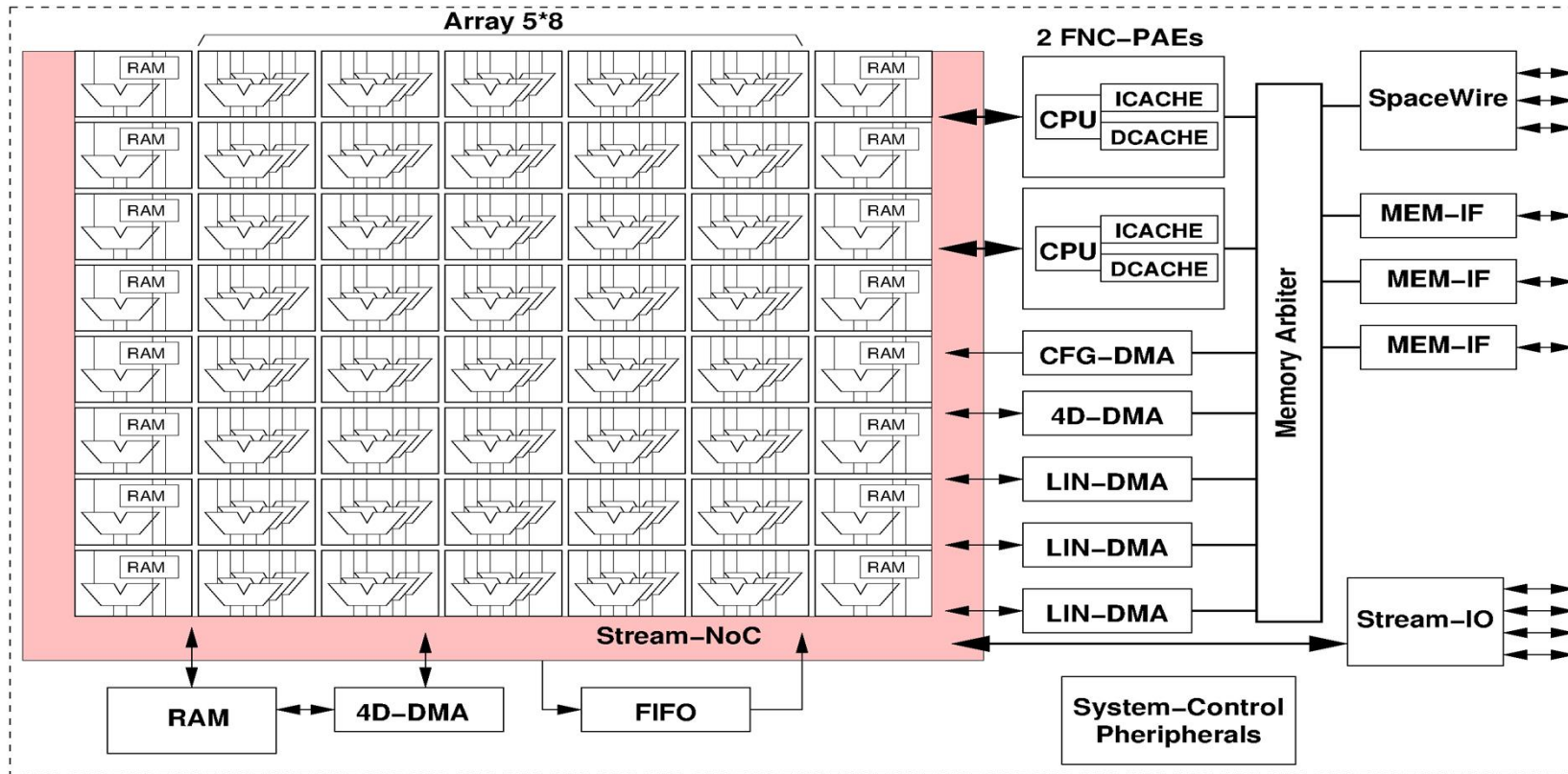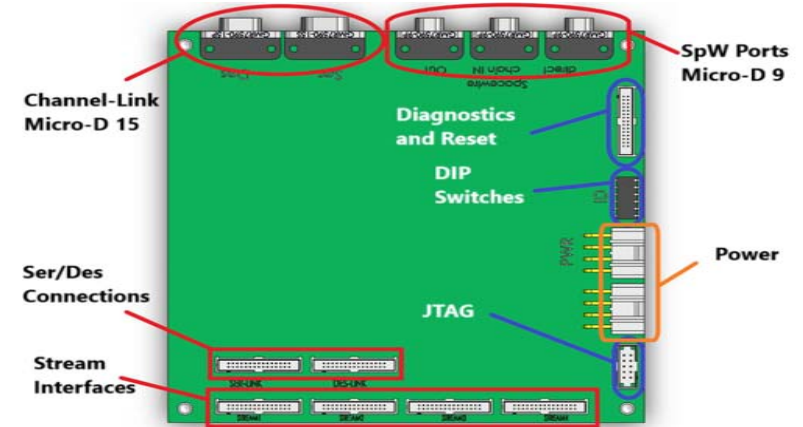
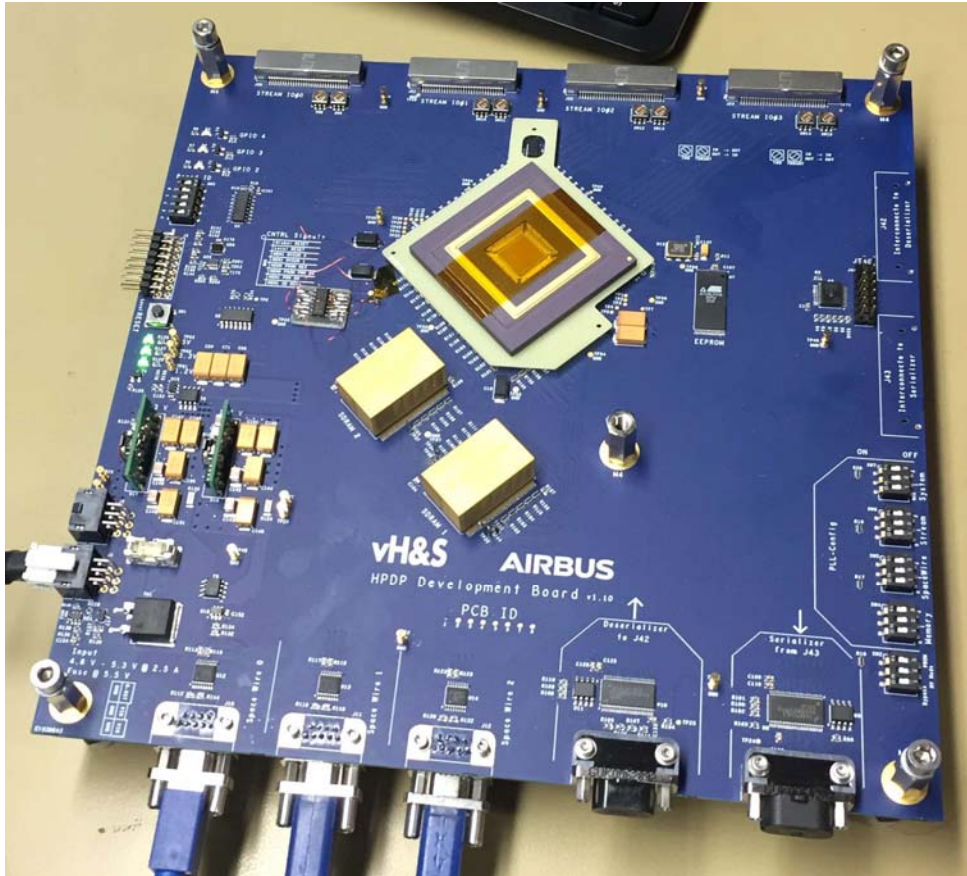# HPDP-40 Software Development Flow
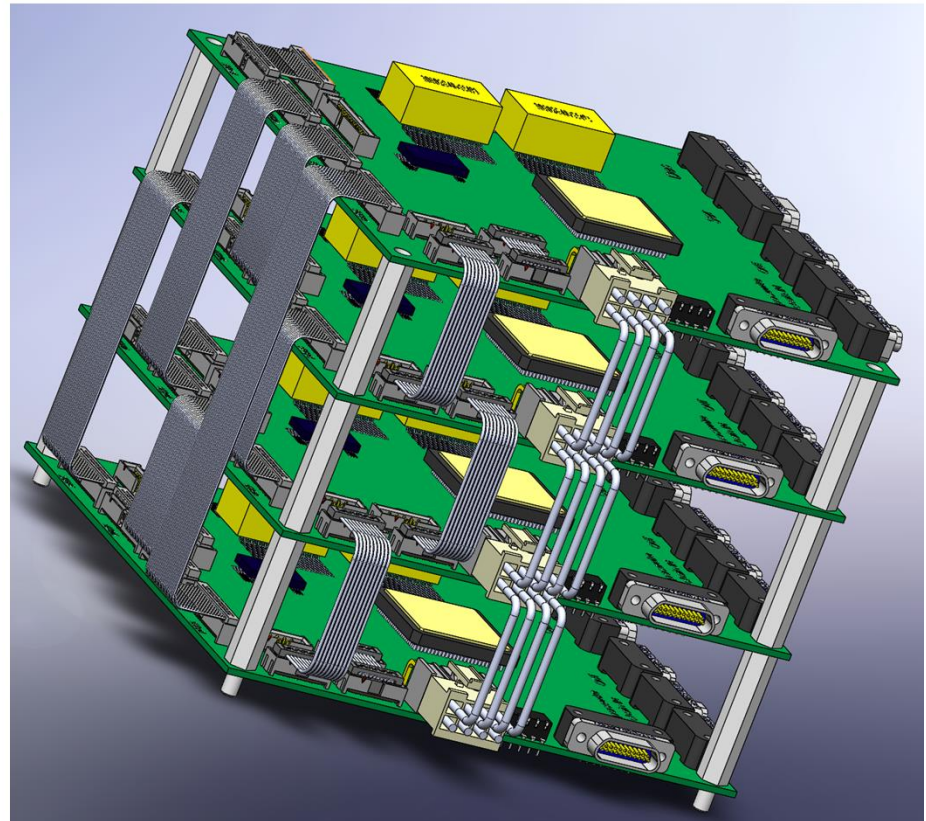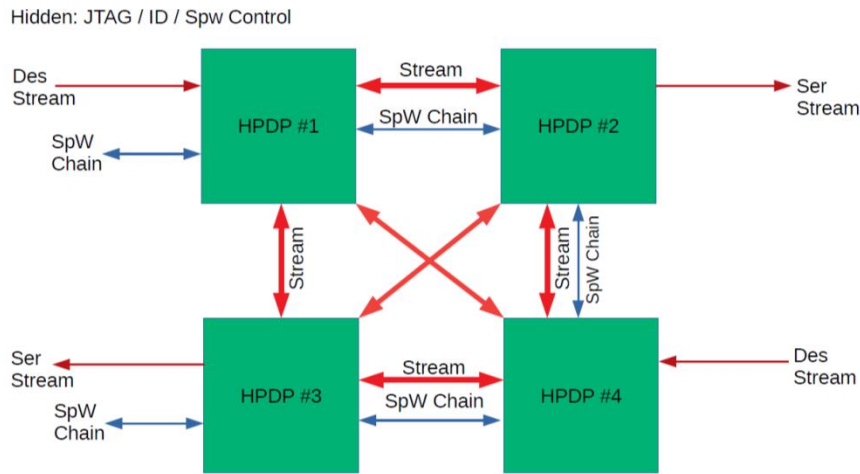

$$y = ax^2 + bx + c.$$

HPDP-40 Demo Kit

Demokit (1/3)

Demokit (2/3)

Demokit (3/3) - Cascading

Test Status & Power Management

HPDP Test Status & Power Measurements (1/2)

Tests are being carried out involving the following sub-systems:

- √ SpW Interface (for Remote Booting)
- √ 2 FNC Execution @125MHz
- √ Port 0 Memory Interface (Non-Volatile Memory)
- √ Port 1 Memory Interface (SDRAM)
- √ On-Chip SRAM
- √ Array Configuration @250MHz
- √ DMAs channels activated

The preliminary power consumption data of the board:

- √ 3.3V domain: stand-by 752mW, running 1.82W
- √ 1.2V domain: stand-by/running 670mW

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HPDP Test Status & Power Measurements (2/2)

Other Preliminary Tests that have been successfully performed:

- √ Stream I/O
- √ Array configuration capability
- √ Array computational capability
- √ EEPROM R/W capability

What Remains to be Tested:

- ☐ Array Operation/Demonstrations;
- ☐ Streaming-I/Os with full speed and with external SERDES devices
- ☐ Multi-Board Operation
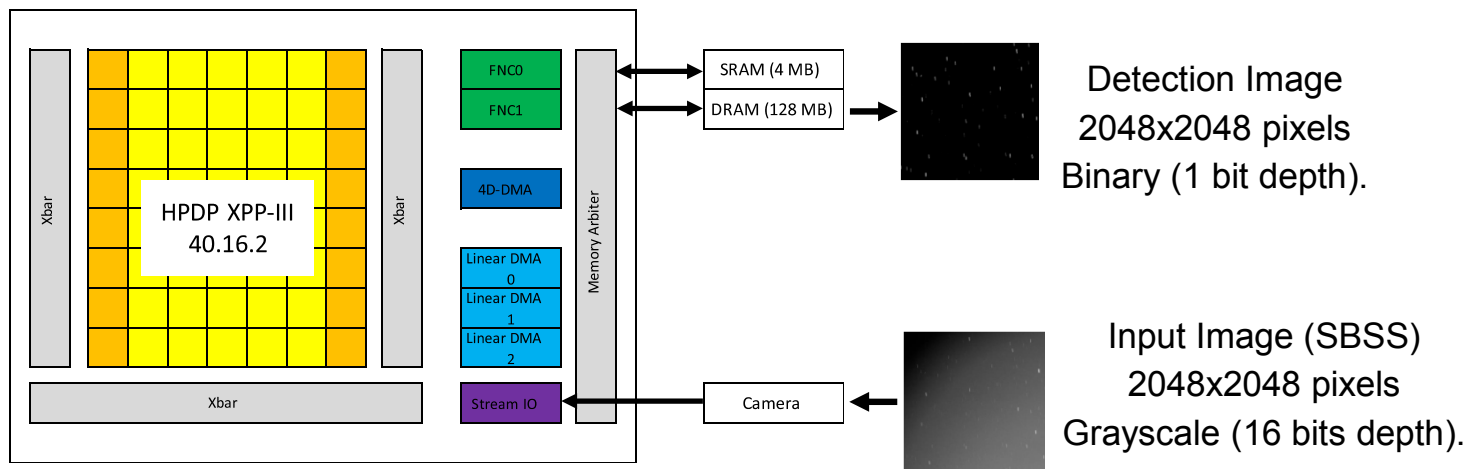
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Application Demonstrations
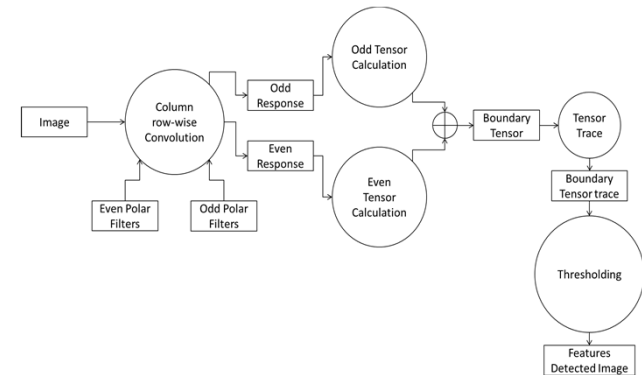
Streak observations algorithms to detect space debris (1)

✓ **Objective:**

- ❑ *Performance:* process one image in one second or less.
- ❑ *Portability:* suitability to implement data-flow. .

FNC0	SRAM (4 MB)
FNC1	DRAM (128 MB)

Detection Image
2048x2048 pixels
Binary (1 bit depth).

HPDP XPP-III
40.16.2

Xbar · Xbar · Memory Arbiter · Xbar

4D-DMA

Linear DMA 0
Linear DMA 1
Linear DMA 2

Stream IO · Camera

Input Image (SBSS)
2048x2048 pixels
Grayscale (16 bits depth).

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Streak observations algorithms to detect space debris (2)

Total memory access Time for the complete algorithm			
Task	Time [sec]	Origin	Destination
transfImg_StreamIOtoDRAM	0,02097	Stream IO	DRAM
transfSubImg_DRAMtoSRAM	0,02097	DRAM	SRAM
boundaryTensor	0,67109	SRAM	SRAM
transfRes_SRAMtoDRAM	0,02097	SRAM	DRAM
Total [sec]	0,734		

Boundary Tensor Flow Block Diagram

⇒ Real-time requirement is met.

Platform	Performance
HPDP	1 image in 0.7s
Desktop PC[1] with algorithm written in C	1 image in 12s

[1]Intel Core i5 Processor clocked at 2.5 GHz with 4 Mbytes of L3 cache

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Autonomous Navigation for Lander Units and Rovers (1)

✓ **Objective:**

❑ *Performance:* Processing Chain per image within one second or less

❑ *Portability:* suitability to implement data-flow. .
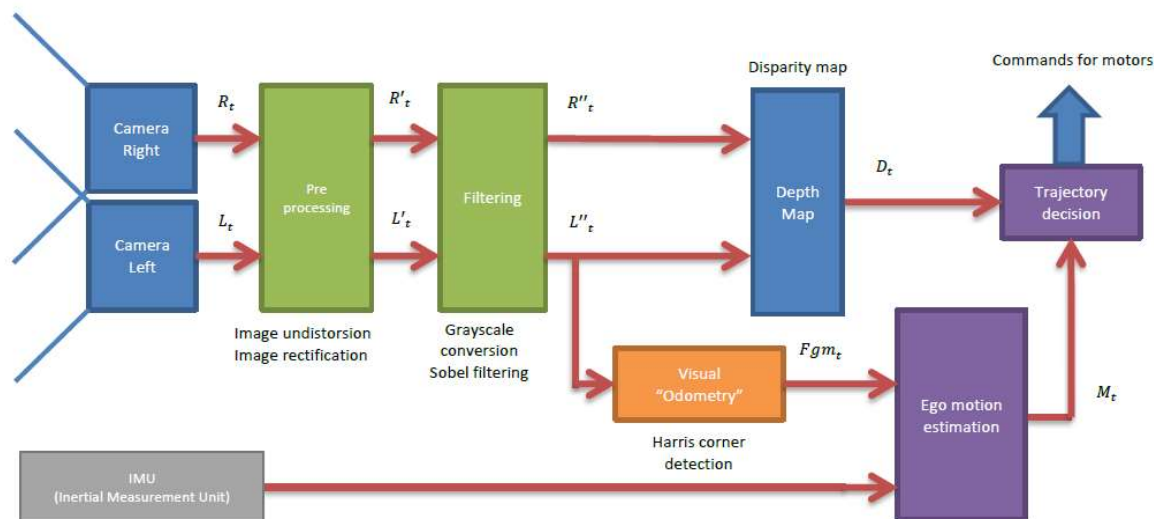
Autonomous Navigation for Lander Units and Rovers (2)

✓ **Implementations:**
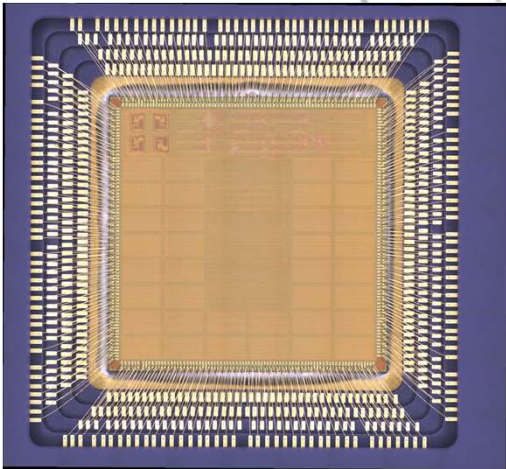
    ❑ *Image Processing Chain executed on HPDP simulator with images of "equivalent" Martian soil*

    ❑ *Pre-processing and Visual Odometry (Harris Corner Detection) can be processed within one second*

✓ **Next Steps:**

    ❑ *Depth Map computation*

    ❑ *Execution on real hardware*

    ❑ *Image compression CCSDS 122.0-B1*

HPDP-40 Chip Industrialisation

HPDP-40 Industrialisation

Aiming industrialization and QML-V plus delta ESCC qualification the following activities currently carried out or planned within current projects:

- A dedicated exhaustive test plan has been elaborated

- ATPG Test covering >95% coverage

- Burn-in board in development to test at 125C ambient temperature and under worst case bias conditions. The devices will be operational during the test with a sample code running in a loop and the test will last about 1000h.

- Radiation Tests covering both total dose (up to 300krad Si) and heavy ion (up to 88 MeV-cm2/mg) experiments

- The device is housed in a 625 ceramic PGA package.

Conclusion & Next Steps

Conclusion

❑ The High Performance Data Processor for Space Applications developed under DLR and ESA contracts is now under commissioning tests in Airbus Ottobrunn and ISD Athens laboratories.

❑ Applications have been implemented on the simulator and showed suitability of the architecture.

Next Steps

❑ Porting of applications on the demokit to demonstrate the performance in hardware and show the very efficient power consumption of this architecture.

❑ Enforce the industrialization of the chip to fit with the next mission requiring high data processing performance

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Contributors

- Laurent Hili, ESA Technical Officer in the frame of KIPSAT activities (ST 65nm rad hard technology)

- Thierry Scholastique and Francois Martin, STM , HPDP Backend Design

- Felix Hormuth, Tobias Disch, von Hörner&Sulgar, DemoKit Development

- Daniel Bretz, Simon Klugseder, Volker Baumgarte, Diego Suarez, Airbus GmbH, HPDP Applications & Test

- George Dramitinos, Yiannis Katelouzos, Olga Dokianaki, Panagiotis Vagiannis, Manolis Lourakis ISD SA

- Vincent Perel, CPE Lyon, Master Student

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Thank you

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