Reliable signal processing

Design examples
We cover the complete system:

- Electronics Design (Analog & Digital)
- Programmable Logic
- Embedded Software
- System Control
- User interaction
- User app development
TEM – Electron microscope imaging

- 16 M pixel 40 fps analog acquisition
- flex technology
- 10 Gbit/s data rate
- vacuum environment & feedthrough
Electrons from the source (primary electrons)

Reflected electrons

Transmitted electrons

Sample

Projection image

Camera Control Unit

Camera Support Unit

Sensor Package PCB

Cooler

Data

Power

User Link to TEM controller (GbE)

I/O link (GbE)

Positioning

Power
- CMOS 2D pixel sensor
- Analog read-out

- Vacuum
- Cooling
  - < -10°C Celsius
- Controlling analog sensor electronics, timing, modes
- Digitizing read-out electronics
- Pixel correction
- Ethernet packetization
• Controlling settings, position, cooling, safety
• Digital image (pre-) processing & compression
• Buffering
Multi-disciplinary design

- Systems Engineering
- Analog & digital electronics
- Mechanical / Thermal design
- Vacuum
- Software
Imaging in Space

• Tropomi instrument on Sentinel 5-P
  • 4 spectrometers: UV / UVIS / NIR / SWIR
  • Generates Level-0 data:
    • Unprocessed instrument measurement & housekeeping data
    • Data sorted by instrument mode/application process

• Payload on Astrabus AS250 Platform
  • LEON3 OBC / RTEMS OS
• Tropomi instrument
- High-throughput data
- Pre-process & compress
- Distributed & scalable
  Analog ↔ Digital
  Hardware ↔ Software
- Standardization
- Modularity
ESA’s next-generation DSP for Space
Need for high-speed data processing in Space

- To match sensor improvements
- Increased data rates and data volume
- Pre-process & filter data in space
- Send useful information to earth

Demand for European fault-tolerant high-performance processing technology:
  - Radiation-hard multi-core DSP System-on-Chip
  - Fault-tolerant Network-on-Chip architecture
Scalable DSP systems

Fault-tolerant DSP subsystem combined with proven Leon subsystem:
• NoC-based multi-core DSP
• Heterogeneous and scalable

MPPB: Multi-core DSP FPGA prototype
XentiumDARE: Rad.-hard prototype IC
SSDP: Rad.-hard multi-core DSP IC
scalable DSP subsystem
Xentium0
Xentium1
ADC/DAC bridge
I/O
SDRAM 1

scalable GPP subsystem
SpW0
RMAP
GPIO
UART
Flash
LCD
SDRAM0

GPP subsystem

timers
RTC

Scalable SoC
/
XentiumDARE

IP validated under radiation:
• Xentium IP
• NoC router
• NoC interfaces (Master/Slave)
• NoC-SpW interface
• NoC-ADC/DAC interface

/ Radiation-hard prototype IC
Rad.-hard prototyping in DARE180

- ASIC Prototype
  - DARE180 CMOS technology
    - Available area: 5x10 mm²
- Architecture
  - 1 Xentium core @100MHz
  - Network-on-Chip
  - SpW-RMAP interface
  - Interface to external ADC/DAC
  - Small memory tile
Programmable high-performance DSP core

- High instruction-level parallelism
  - 10 parallel execution units
- Data precision
  - 32/40-bit fixed-point datapath
  - Single-Precision floating-point
  - 16-bit SIMD
- Features
  - Single-cycle latency Data Memory
  - Single-cycle latency Instruction Cache
  - Short 3-cycle pipeline
  - Hardware debug infrastructure
- Efficient complex MAC execution:
  - 2 16-bit complex MACs/cycle
- Register bypass (latency, energy, code size)
  - Loop buffer (energy, code size)
Software Development Environment

Xentium C compiler (LLVM/Clang)
- ANSI/ISO-standard C
- Built-in functions for Xentium specific operations
- Mix C and assembly function calls

Xentium assembler
- Clean and readable
- Extensive built-in preprocessor
- Standard assembler directives

Compile, assemble & link a program in a single step

Xentium ISS (Instruction Set Simulator)
- Trace program execution
- Interactive debugging
- Program profiling
Fault-tolerant NoC

- 32-bit packet-switched 2D-Mesh
- XY-routing, deadlock free
- 5-port routers featuring 4 prioritized services (QoS)

- Fault-tolerance
  - Adaptive XY-routing to provide data rerouting in the NoC
  - Flit-level flow control
  - Enable the insertion of EDAC on data links to increase robustness
IP availability

• Xentium DSP and NoC will become available as ESA IP cores
• IP validated under radiation in rad.-hard XentiumDARE IC (TRL 6)

• Contact Technolution for licensing & support
  • Xentium SDE
  • FPGA-based evaluation options

www.recoresystems.com/products
**FreNox-E**

*Embedded processor*
- hardware
  - RV32I(M)
  - 32bits, mul/div
  - 5 stages - Harvard arch
  - cache or internal RAM
  - IO space
- software
  - Bare metal
  - FreeRTOS
  - ThreadX

**FreNox-S**

*Application processor*
- hardware
  - RV32IMAS
  - 32bits, mul/div, atomic, supervisor
  - 5 stages - Harvard arch
  - iMMU, dMMU (1 - 128 entries)
  - 8 way associative cache (4 - 32k)
  - cache coherency (DMA)
  - IO space
- software
  - Linux
  - Buildroot
Our services for customers

- Continuous Integrated Development
  - Programmable Logic / FPGA design
  - VHDL design / ASIC front-end design
  - Electronics Design (Analog & Digital)
  - Embedded Software
  - Application Software / Algorithms

- Multi-disciplinary Project Management
  - Mission-, safety-, security-critical

- Xentium DSP, FreNox RISC-V and Network-on-Chip IP reuse
  - IP licensing & support
Our unique IP

- Powerful Digital Signal Processor
  - Xentium DSP IP
  - Software Development Environment

- Reliable general purpose processor
  - FreNox RISC-V IP
  - Software Development Environment

- Fault-tolerant on-chip interconnect
  - Network-on-Chip IP
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