

On-Board Payload Data Processing requirements and technology trends

European Workshop on On-Board Data Processing (OBDP2019)
ESA/ESTEC, Noordwijk, The Netherlands, 25/2/19

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On-board Data processing expert

AIRBUS Defence and Space – Engineering/Space Systems

February 2019

On-Board Payload Data Processing requirements and technology trends

- Vision
- Targets
- Technologies
- Developments

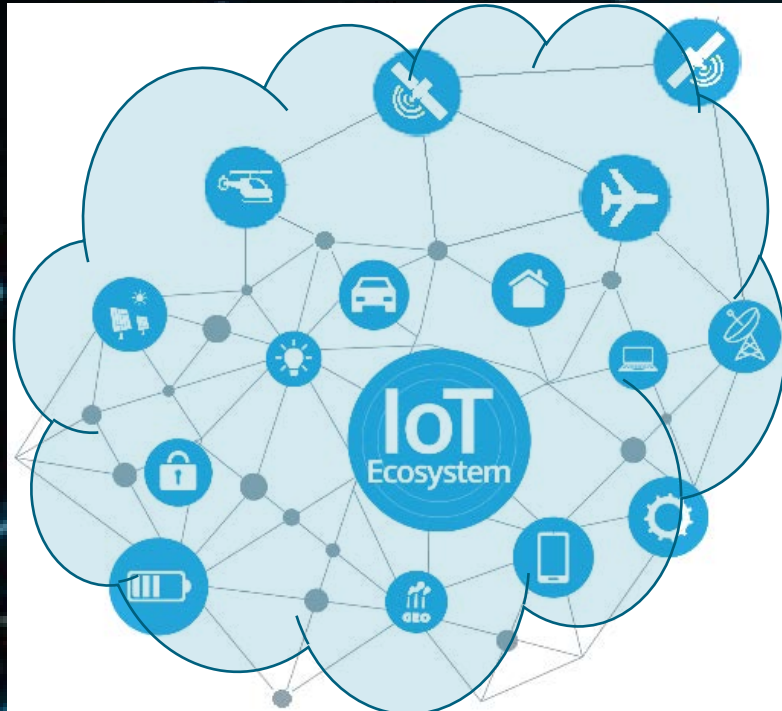


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Our future is IoT @ any-time everywhere

Connected smart machines

Smart vehicles and robots in smart cities
Autonomous and **Everywhere Connected**



Machine learning Big Data Cloud Artificial intelligence
SOFTWARE Data Processing
Electronics

Today **IoT**

Tomorrow
Vehicles
Robots
Autonomous
Connected



AIRBUS

On-Board Payload Data Processing requirements and technology trends

Vision

Targets

Technologies

Developments



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Targets

Computing Performance

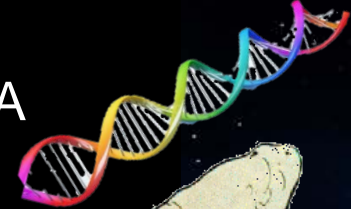
GFlops x Gbps / Watt / Kilo / cm³...



OPEN

Flexibility

Software, reprogrammable FPGA
interoperability, modularity



Robustness

Technology
Fault tolerance
Technology Independence



Determinism

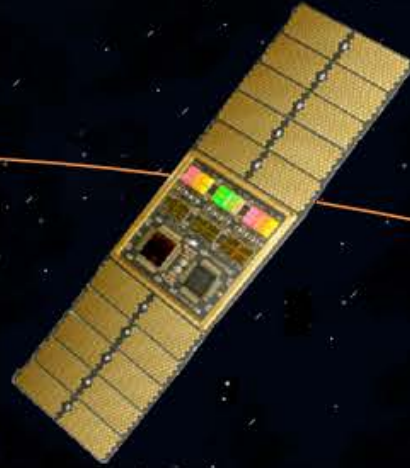
Functional correctness
Time predictability

Programming efficiency

Portability
Testability TOOLS
Easy programming



On-Board Data Processing



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Technologies



OPEN

Multi-cores

Performance

Challenges

Game change



Is not a requirement

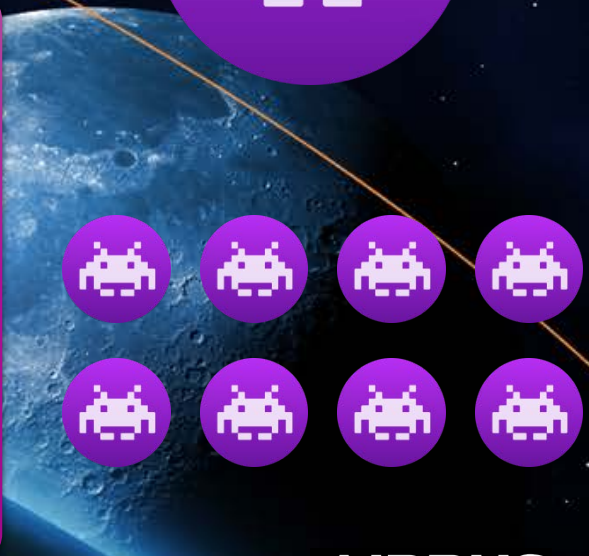
Is an enabling Technology for more Performance & Integration

Size
180nm
150nm
90nm
65nm
28nm
24nm
16nm

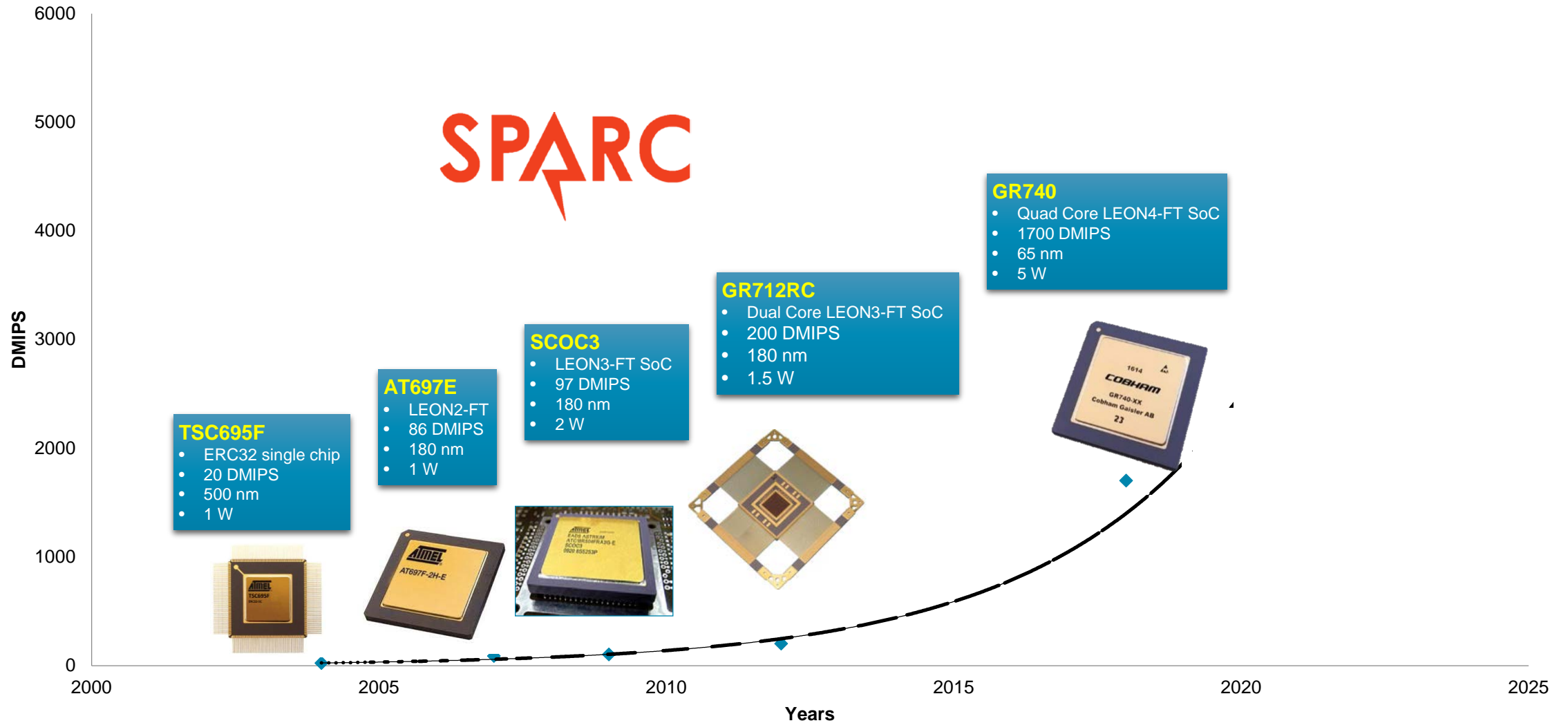
Power
more GHz
Gbit/s
GFLOPS per Watt

Resources sharing
Memory caches
I/Os
FPU

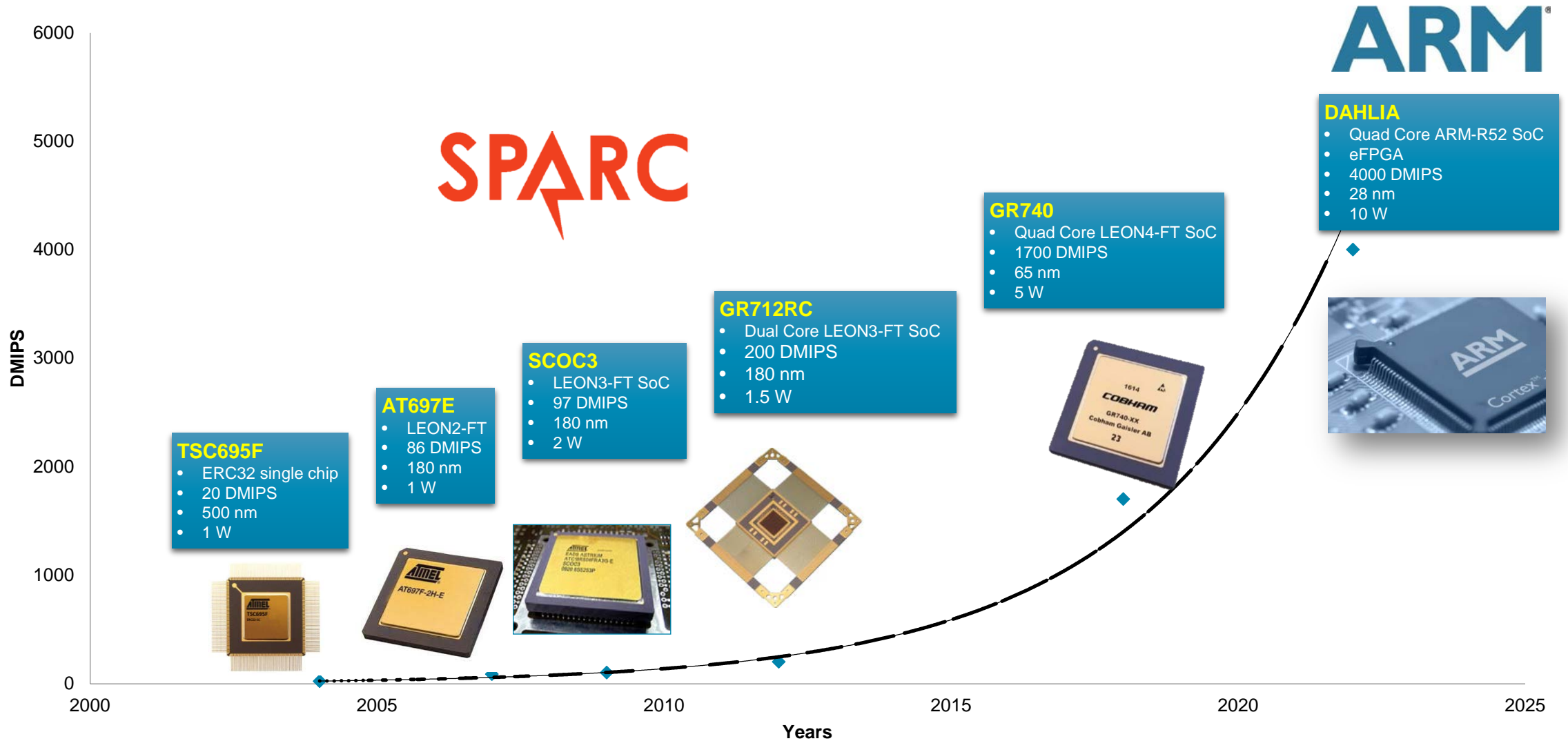
Software Parallelism
SMP
AMP
MTAPI
OpenMP
OpenCL



Space Processors



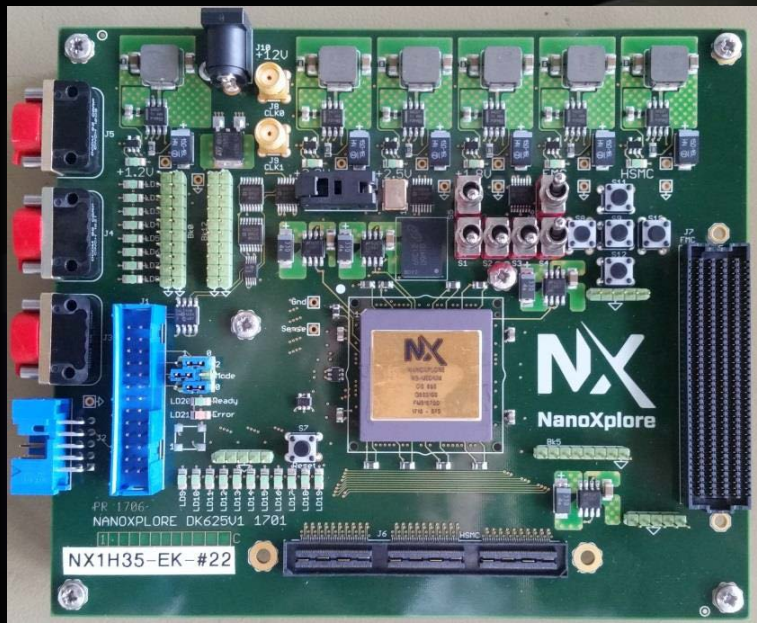
Space Processors



ARM

- DAHLIA**
- Quad Core ARM-R52 SoC
 - eFPGA
 - 4000 DMIPS
 - 28 nm
 - 10 W





Exhibition area



ST 28nm FD-SOI Technology

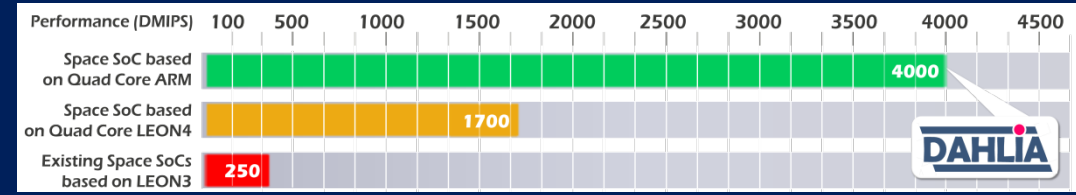
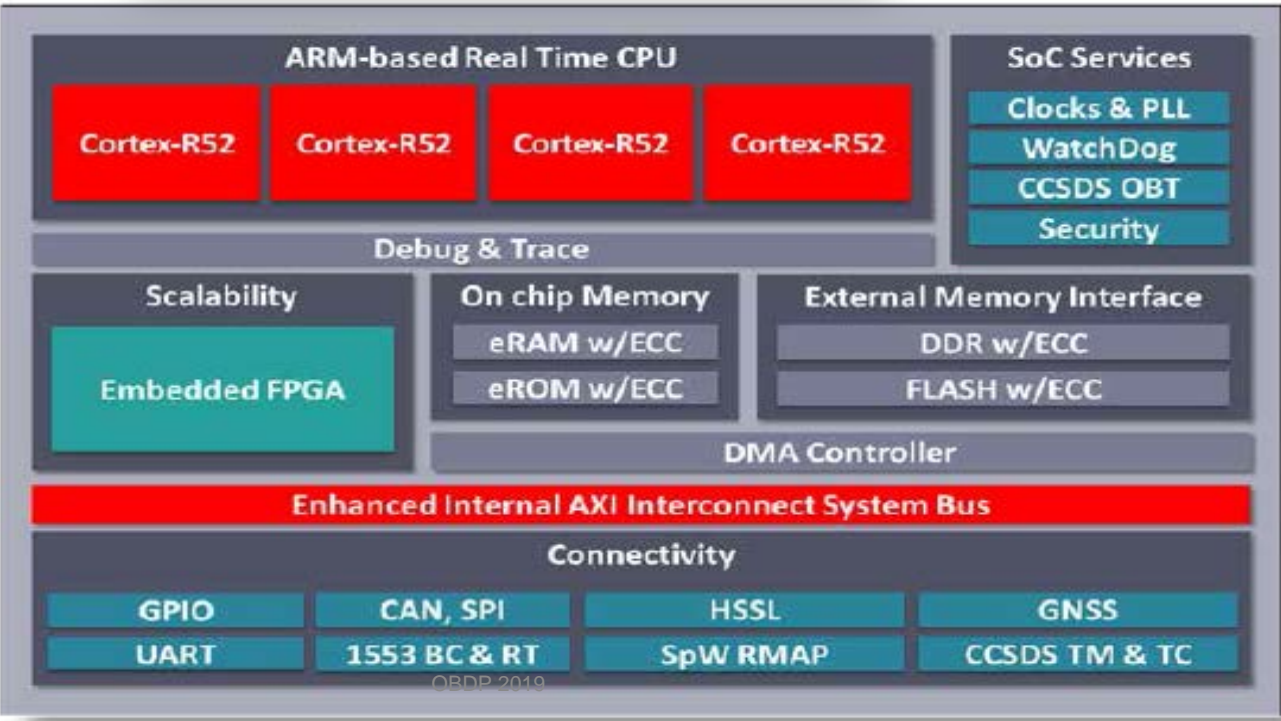
- ▶ High performance with low power consumption
- ▶ High robustness in radiation environment



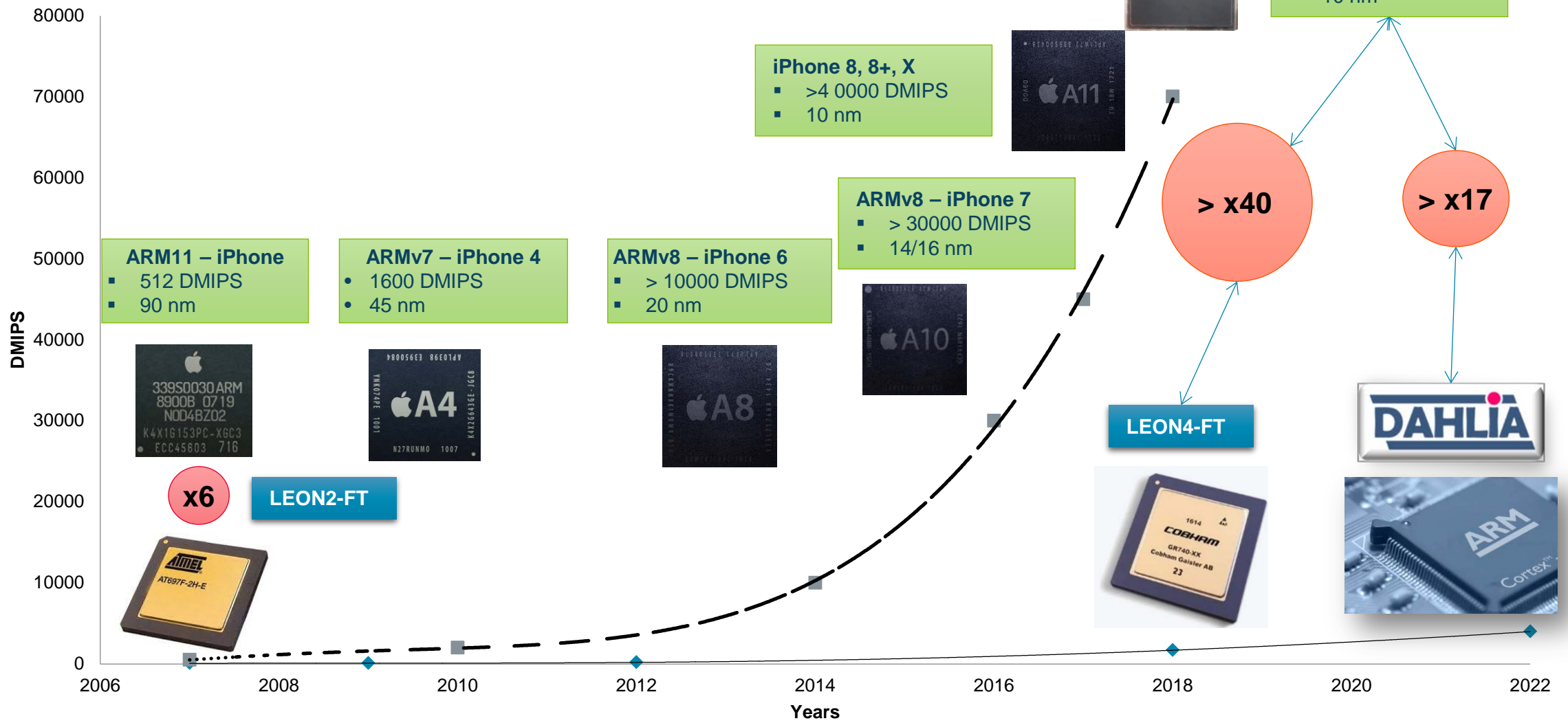
a powerful combination of innovative technology adapted for Space

4 x ARM Cortex-R52

- ▶ ARM's most advanced processor for safety
- ▶ Flexible on Chip Hardware functions with eFPGA

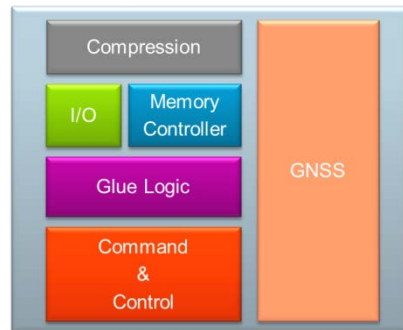
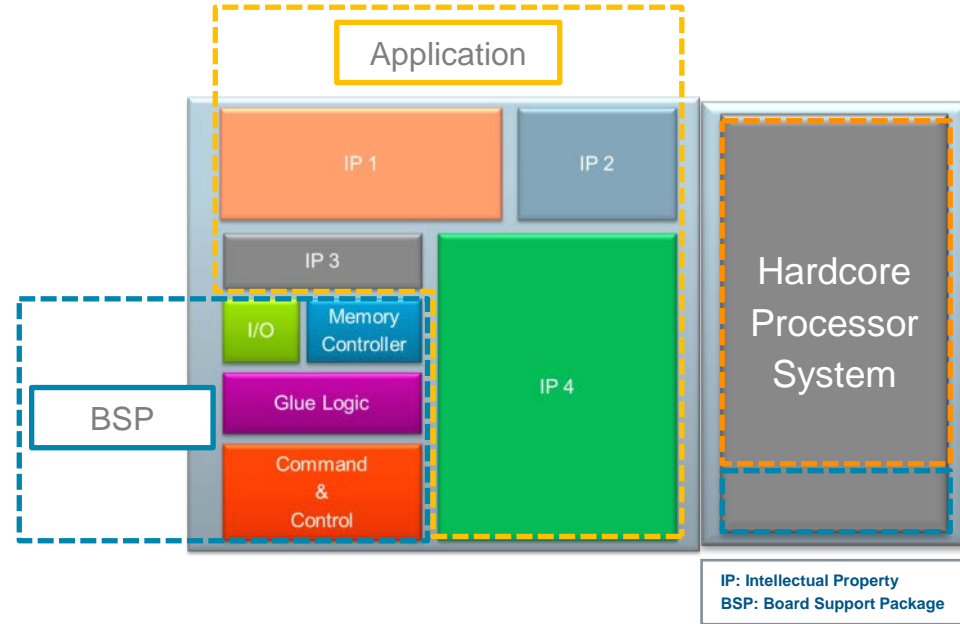
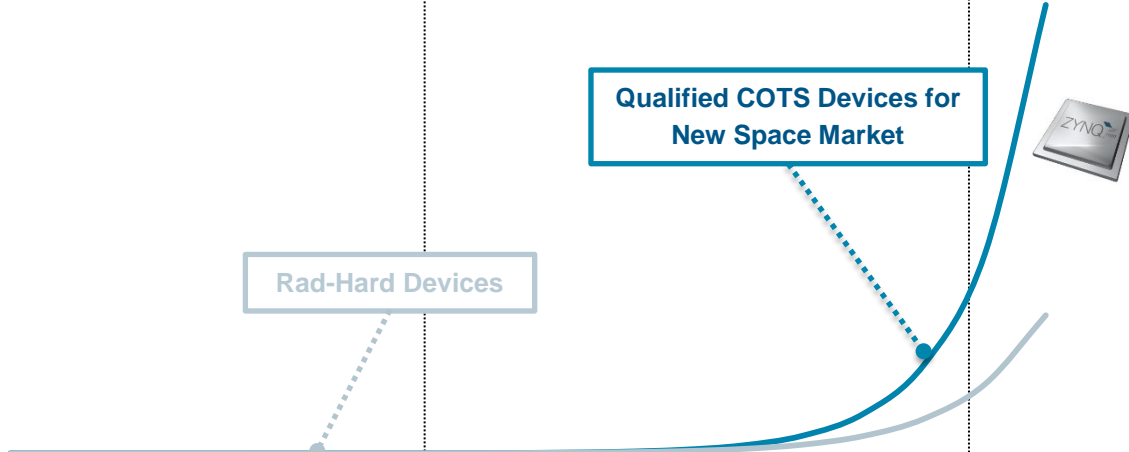


Space Processors technology gap



Space FPGA → more processing performance

Complexity / Performances



SoC FPGA

High Capacity FPGA

Multi Processor SoC (MPSoC)

Reconfigurable FPGA

BRAVE DAHLIA

COTS products

Past

Present

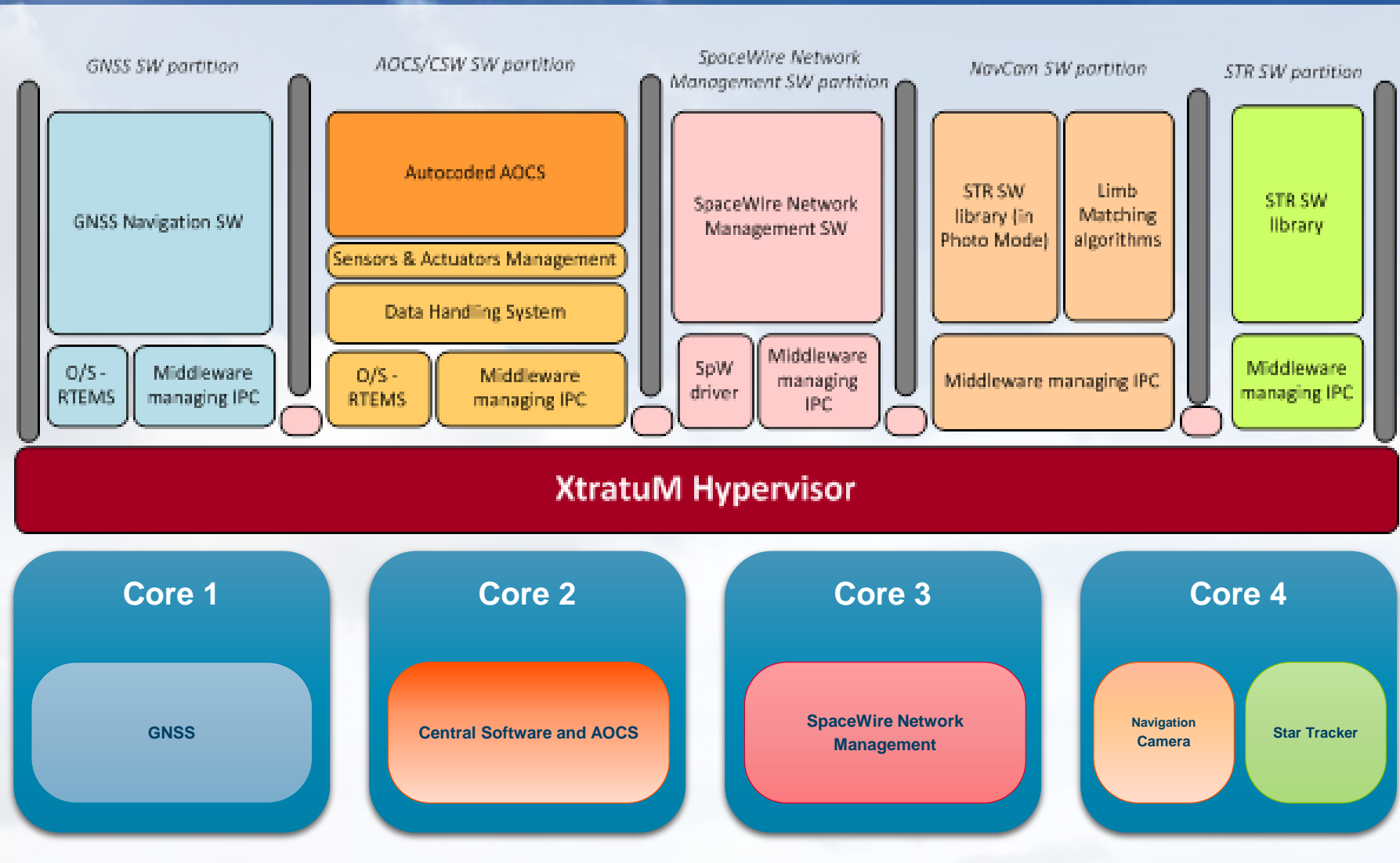
Future





Software: Integrated Spacecraft Data Handling – IMA style

From ESA Study Prototyping a SpaceWire AOCs



Satellite Central Software

- TSP Hypervisor
 - Xtratum / PikeOS
- Operating Systems
 - RTEMS or others

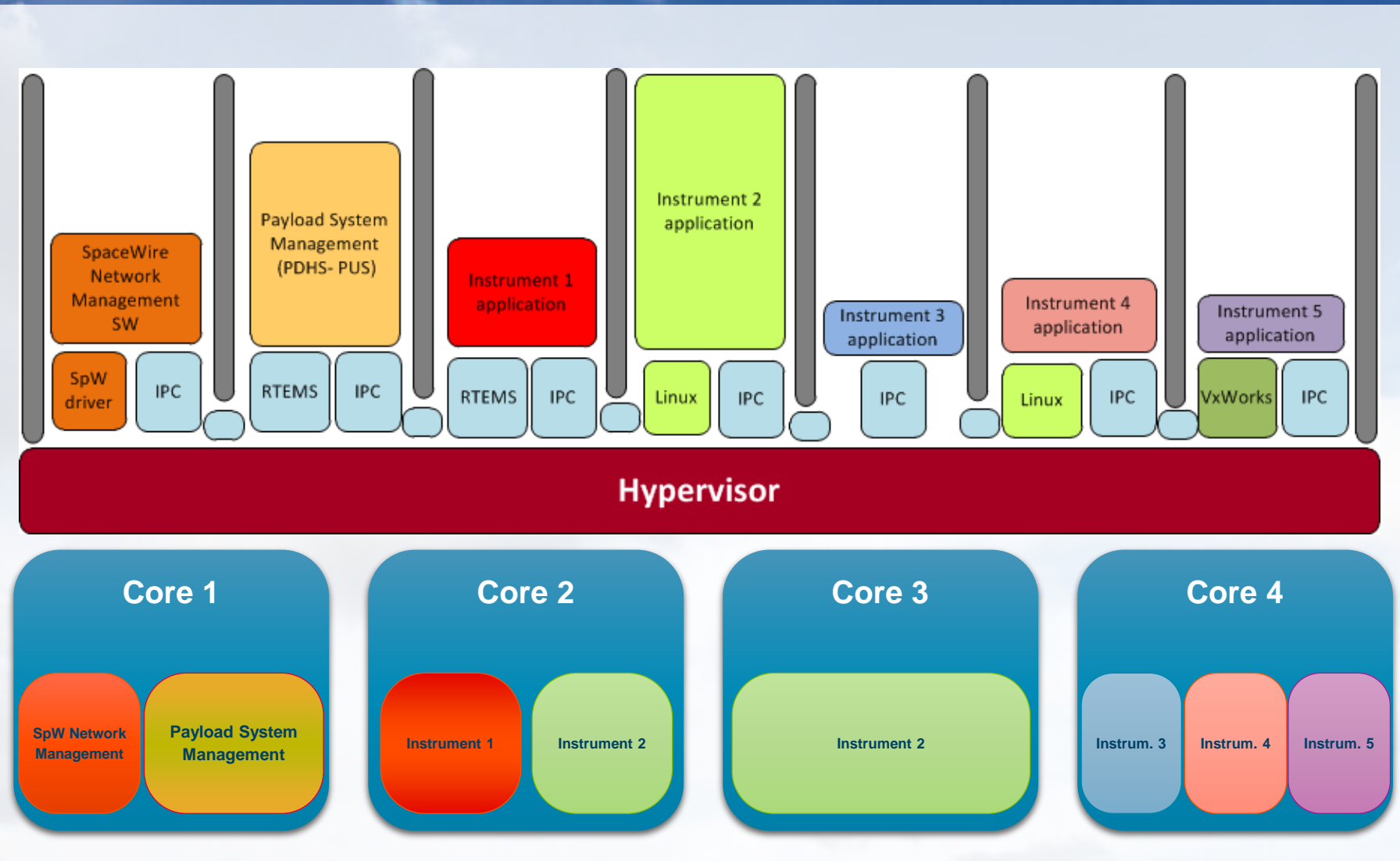
Asymmetrical Multi Processing

- Static partition mapping

- LEON 4 (GR740)
- ARM (DAHLIA)
- COTS (ARM, PowerPC)

Software: Integrated Instruments Control and Data Processing

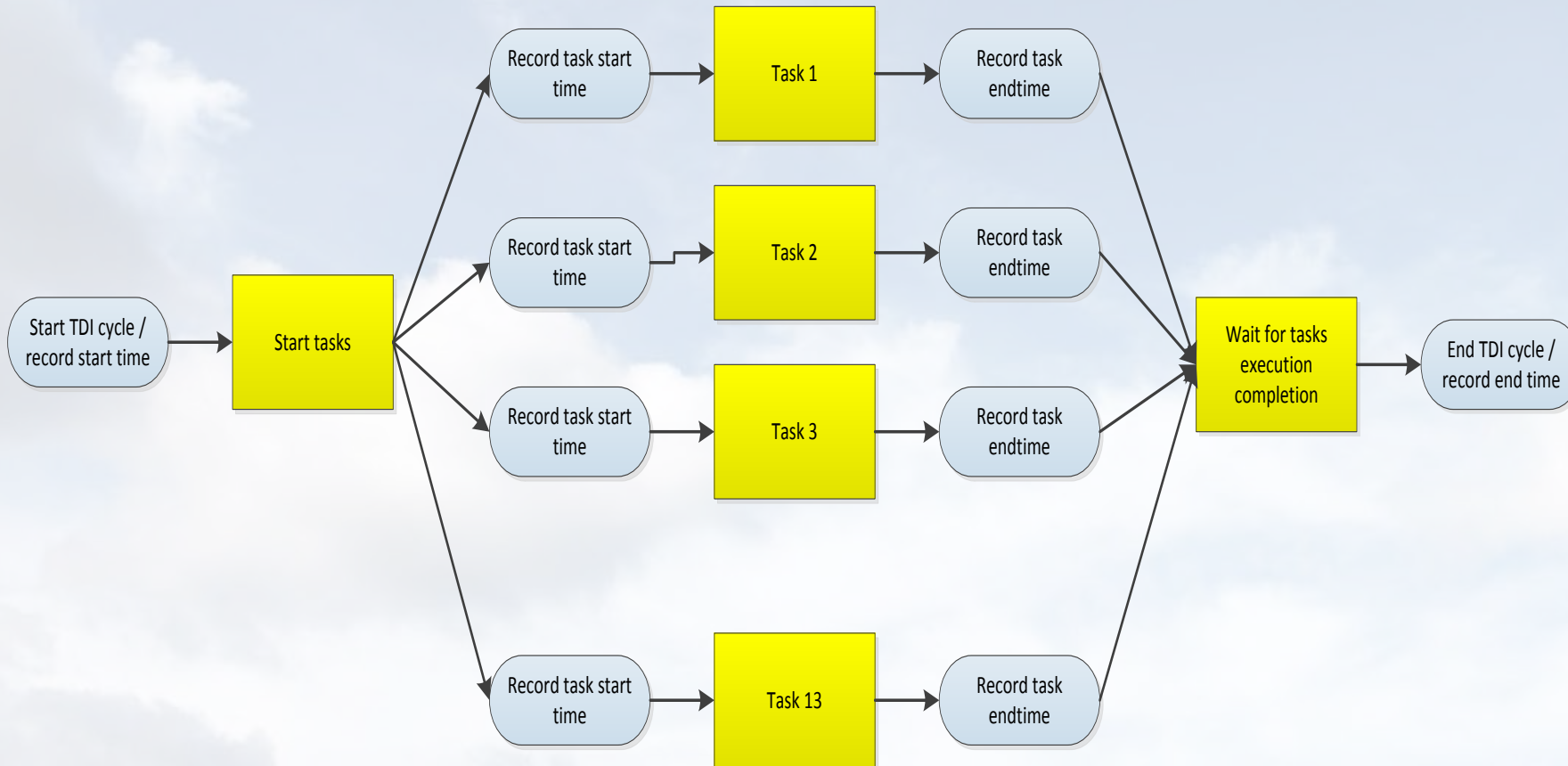
Payload Data Handling Software



- S/W partitioning
 - Independent software development validation & integration
 - Mixed criticality
- Operating System
 - Choice of the payload systems integrator and instrument developers
- LEON 4 (GR740)
- ARM (DAHLIA)
- COTS (ARM, PowerPC)

High Performance Payload Data Processing

Payload Data Processing



S/W Parallelisation

- RTEMS (SMP, MTAPI)
- OpenMP, OpenCL...

Multicore processor

- LEON 4 (GR740)
- ARM (DAHLIA)
- COTS (ARM, PowerPC)

Manycore

- MPPA (Kalray)
- GPUs
- RC64 (RamonChips)
- HPDP (Airbus)

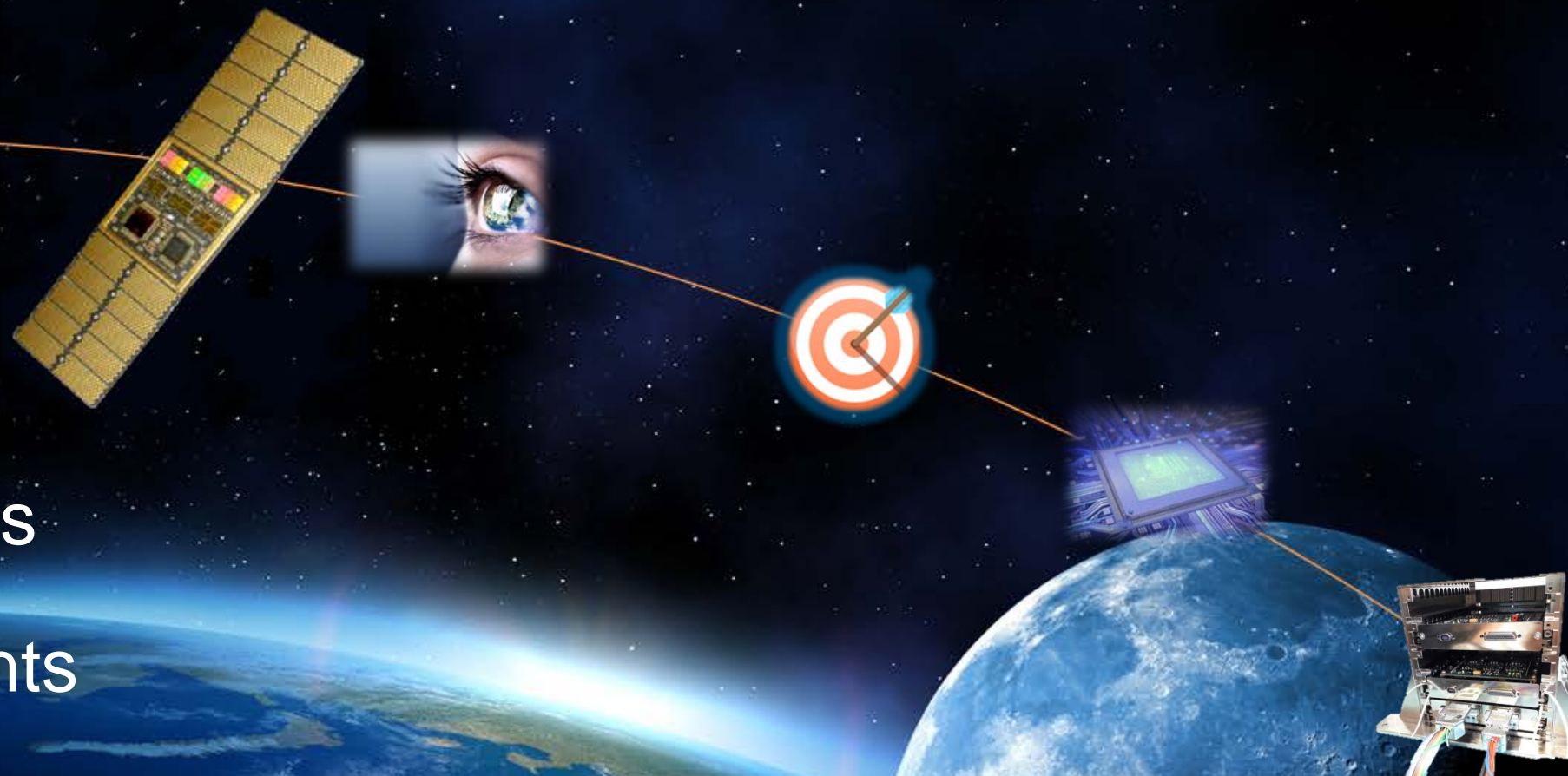
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SPINAS computer (OBC-SA project)



Monday @ 14:30

Wednesday @ 15:20

On-Board Computer System Architecture project (DLR)

• Objective

- Open Modular Architecture (Space cPCI Serial)
- Modular S/W with Time and Space Partitioning (PikeOS)
- High performance multicore processing for resource sharing
- Miniaturisation (3U boards, <5kg)

• Features

- High reliability SPARC V8 CPU (GR740)
 - 4 cores @ 250 MHz
 - 459 DMIPS per core
- 256 MB SDRAM (+EDAC)
- 2x Gigabit Ethernet
- 8x SpaceWire up to 300Mbit/s
- Redundant MIL-STD-1553B
- 2x CAN, 2x RS422
- Watchdog for system reliability



LEON4 Processor Board Bottom View



SPINAS EQM Computer Box

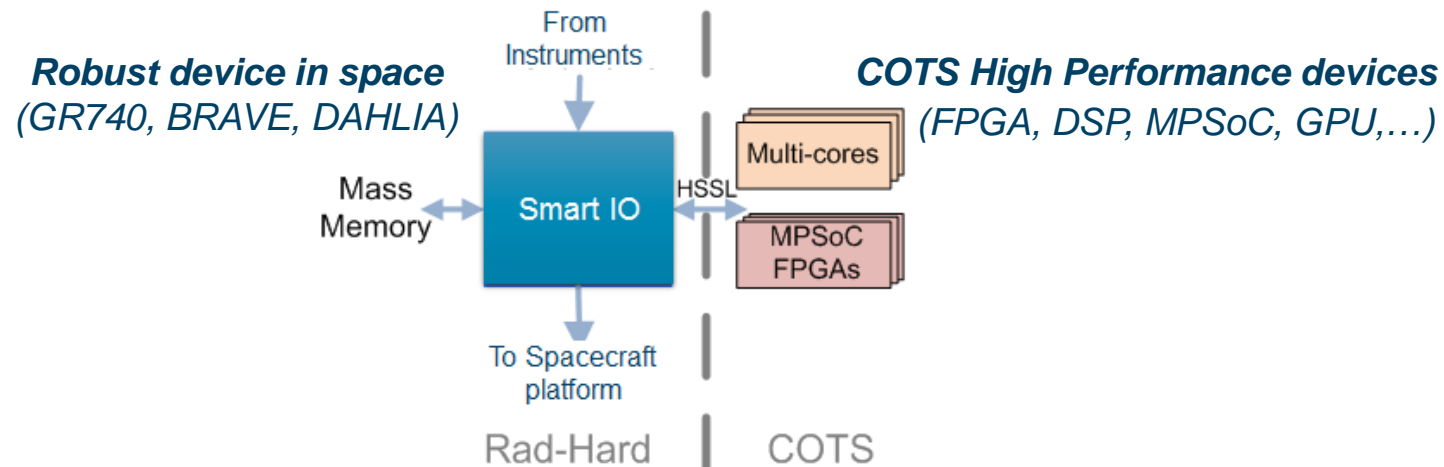
COTS based Reliable Architecture (COBRA)



Monday @ 14:50

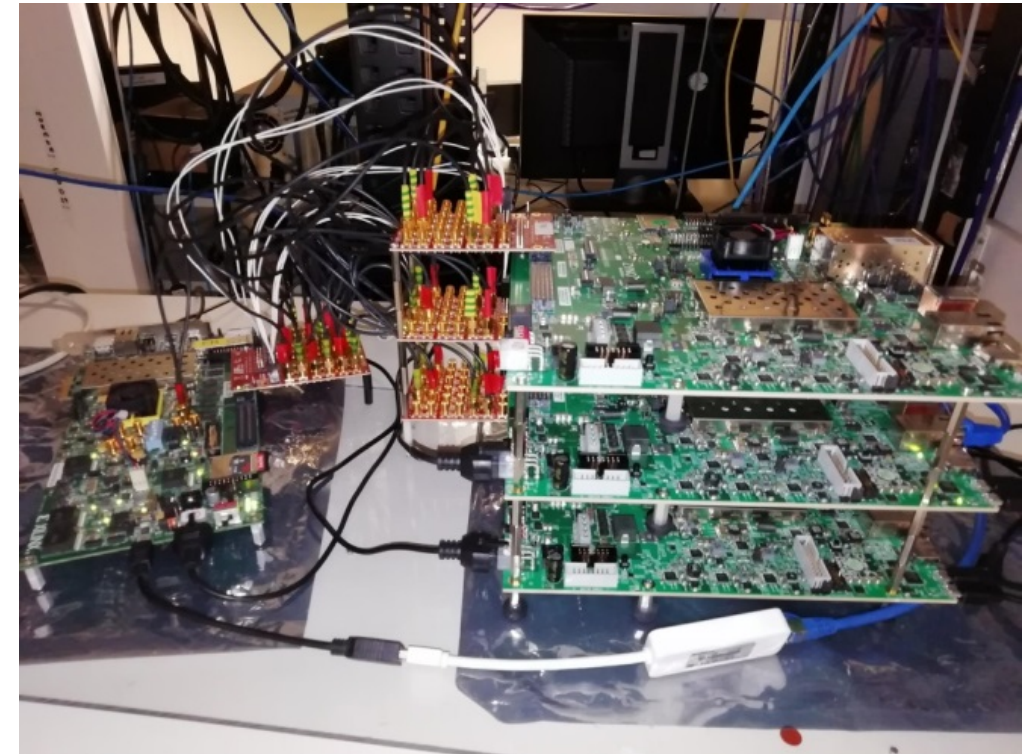
COBRA Concept

- ESA study « High Performance COTS based Computer »



- HW/SW codesign : Development methodology & tools
- Applications:
 - Low cost highly integrated processing platform
 - advanced image processing
 - Autonomy (navigation mission planning, AI...)
 - SDR radar/telecom...

COBRA demonstrator



COBRA demonstrator with 3 PM based on Zynq Ultrascale +

OPAZ

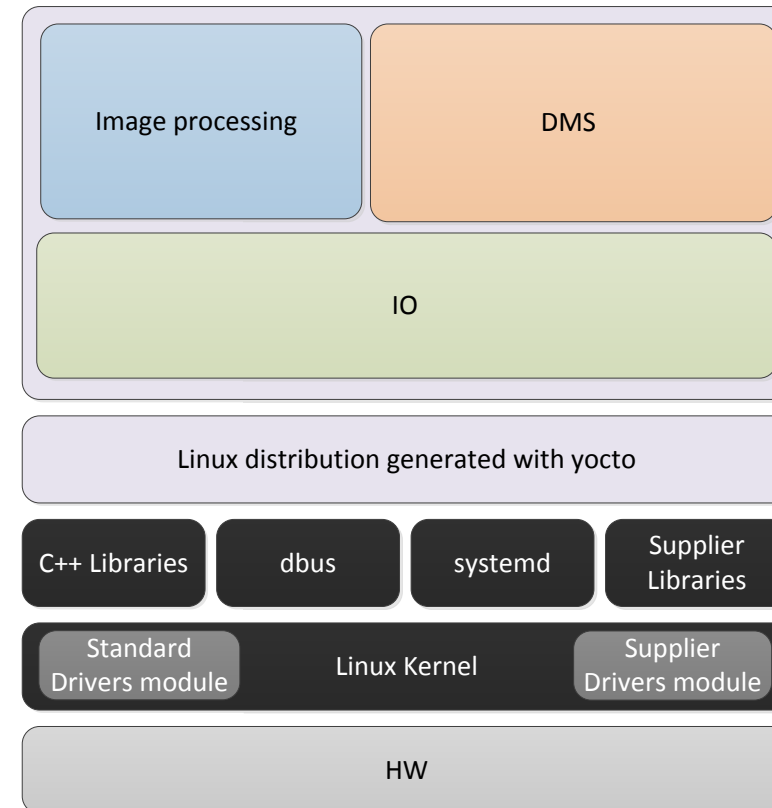


Tuesday @ 16:30
Poster session

- Optical Payload for Zephyr
 - Camera RGB 18cm over 1km²
 - Camera RGB 2m over 100km²
 - Live transmission
- Fully based on HW and SW COTS
- Embedded Linux:
 - Yocto distribution
 - SystemD : init and system manager
 - dBus : Inter process communication bus
- Keep it small and simple (KISS) design principle



OPEN

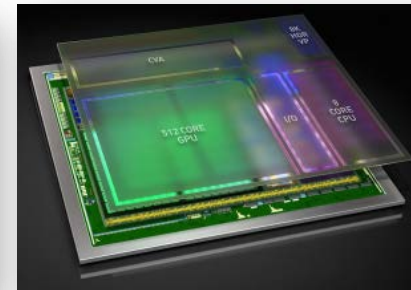
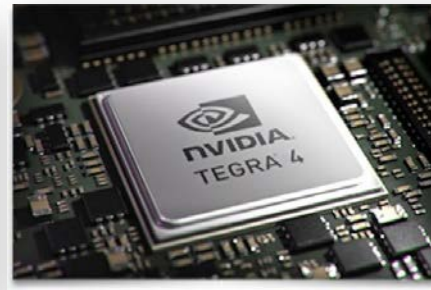
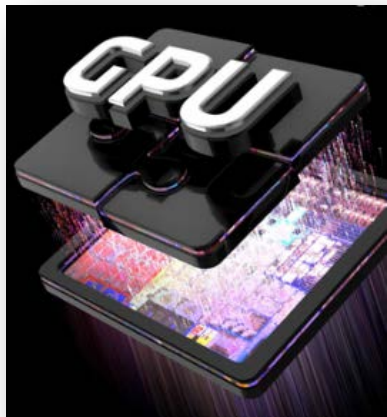


LPGPU4S - Low Power GPUs for Space

ESA Study with the Barcelona Supercomputing Center

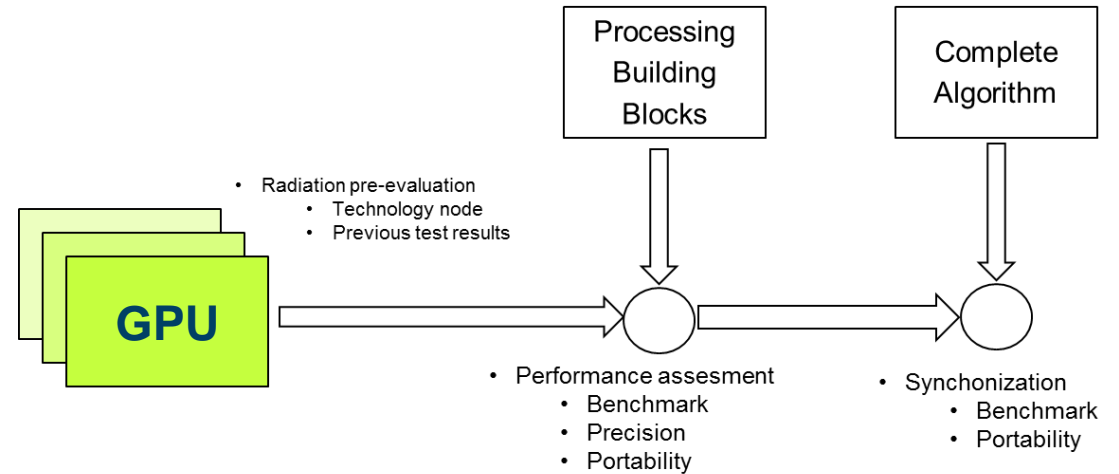


- Evaluation of Low Power GPUs for Space
 - Analysis of many GPU products
 - Main criteria's for evaluation
 - Technology robustness vs. radiation
 - Performance assessment (incl. power consumption)
 - Parallel Programming model
 - Licensing scheme
 - Application benchmarks



Wednesday @ 12:30

Evaluation methodology



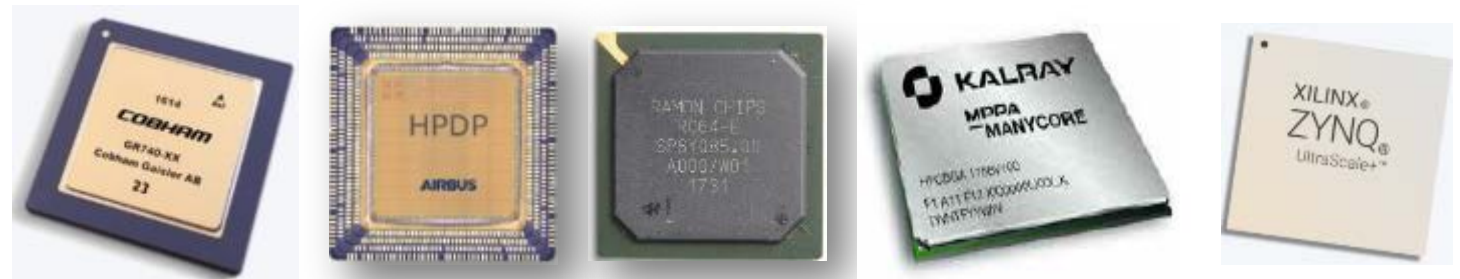
HP4S – High Performance Parallel Payload Processing for Space

ESA Study with the Barcelona Supercomputing Center



- S/W parallelisation with OpenMP
 - Selection of suitable MC targets
 - Adaptation/development of OpenMP
 - Application benchmarks
- Main criteria's for target selection
 - Technology robustness vs. radiation
 - HW compatibility with the OpenMP
 - Evaluation kit availability
 - S/W ecosystem and porting effort
 - Range of applications
- Evaluation benchmarks / use cases
 - ESA generic P/L processing benchmarks
 - GAIA VPU
 - Image processing
 - active mirrors
 - Robotics: disparity map, inverse kinematics

Target	Supplier	Type	Application	RH
GR740	Cobham-Gaisler	Quad Core Leon GPP	General purpose	Yes
MPPA	Kalray	80 cores clustered Processor Array (Coolidge)	General purpose with intensive Data flow	No
Zynq	Xilinx	Quad Core ARM53 on MPSoC	General purpose with internal FPGA accelerator	No
RC64	Ramonchip	64 DSP cores NoC	DSP	Yes
HPDP	Airbus-DS	40 cores Processor Array	Data flow intensive processing	Yes



Conclusion



Rad-hard space computers

• Processing elements

- LEON family up to GR740
- BRAVE family (DAHLIA , FPGA + MPSoCs)
- Manycores (HPDP, RC64)
- ASICs

GENERIC

SPECIFIC

• Applications

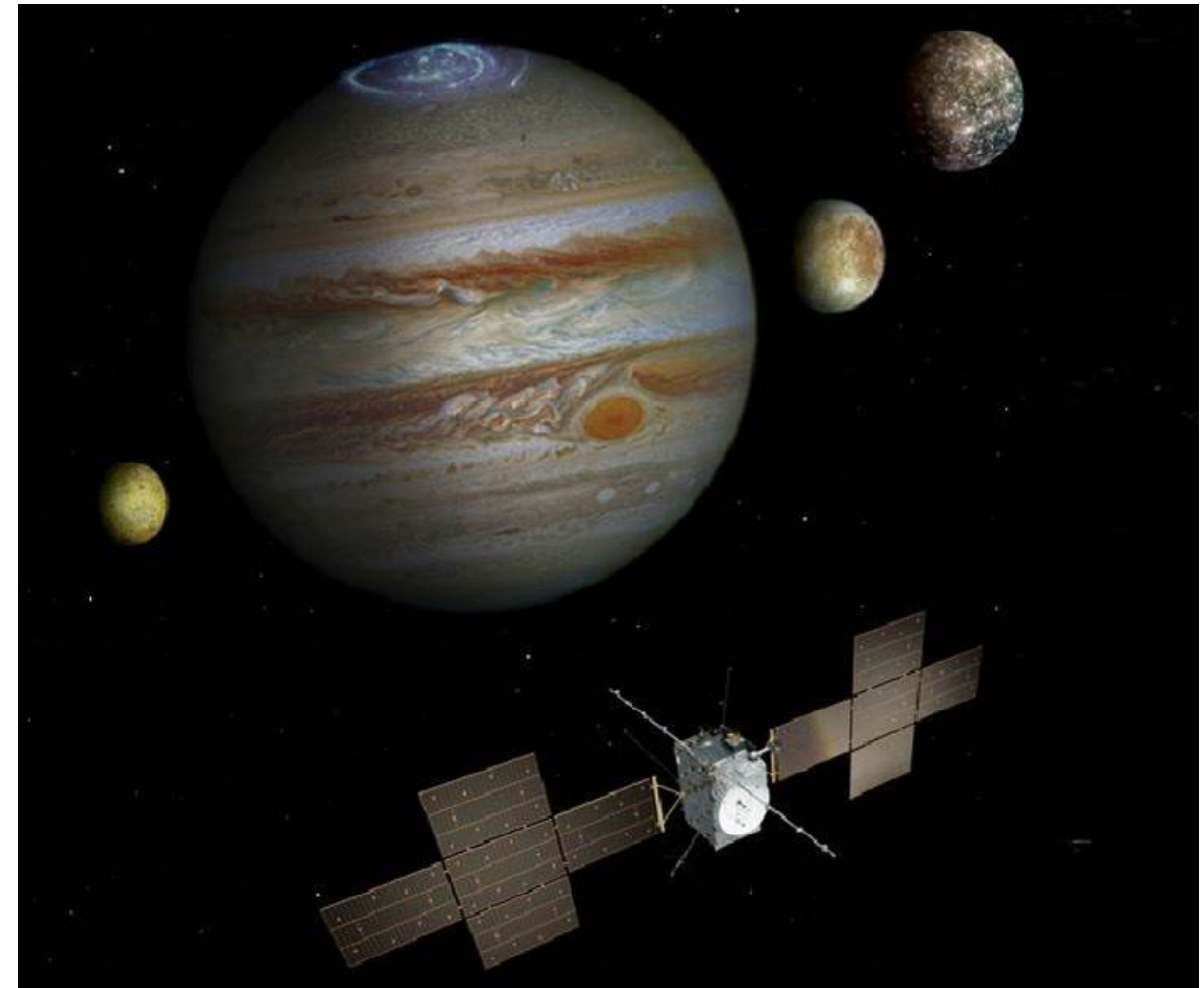
- Harsh environment, deep space science and exploration, critical functions...
- Long duration/critical missions in GEO/LEO
- Low number of spacecraft

• High RC / High NRC

- Specific Technologies & Tools
- Long developments cycles

Modular products with generic devices

Hardware Integration - Software Partitioning



COTS-Based fault tolerant computers



• Processing elements

- MP Processors (ARM, PPC, RiscV...)
- FPGAs (Kintex...) and MPSocs (Zynq...)
- Manycores (Low power GPUs, MPPA,...)

GENERIC

HIGH PERF

• Applications

- “*new space*” constellations, Low Earth Orbit, launchers, non-critical functions, Short missions
- Very high Performance non critical computers
- Fast expanding market

• High NRC / Medium to Low RC

- Mitigation of radiation effects
- Component characterisation and qualification
- Obsolescence management
- Low Recurring Cost with large number of units

Product lines with Large application range

Adoption of COTS standards and software

Thank you for your attention !

Questions ?

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