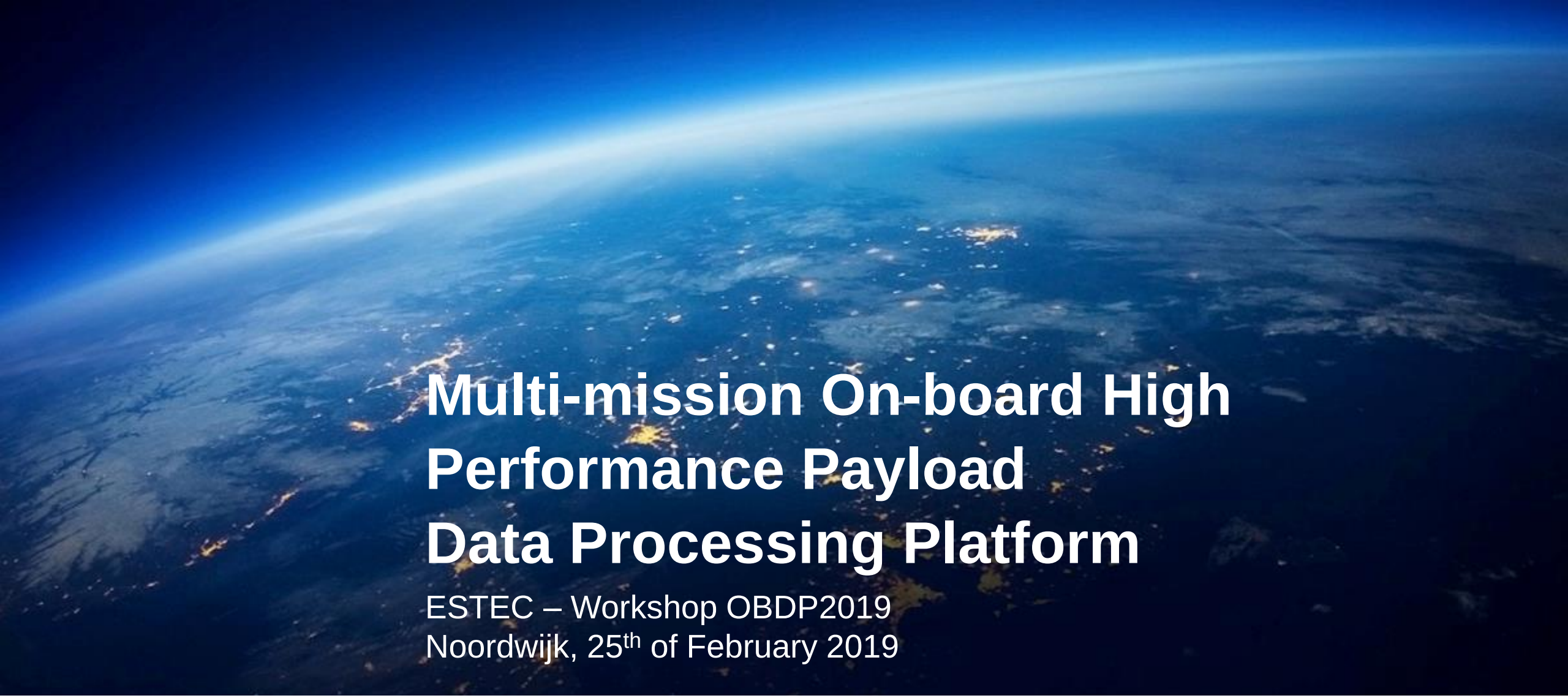

Multi-mission On-board High Performance Payload Data Processing Platform

ESTEC – Workshop OBDP2019
Noordwijk, 25th of February 2019

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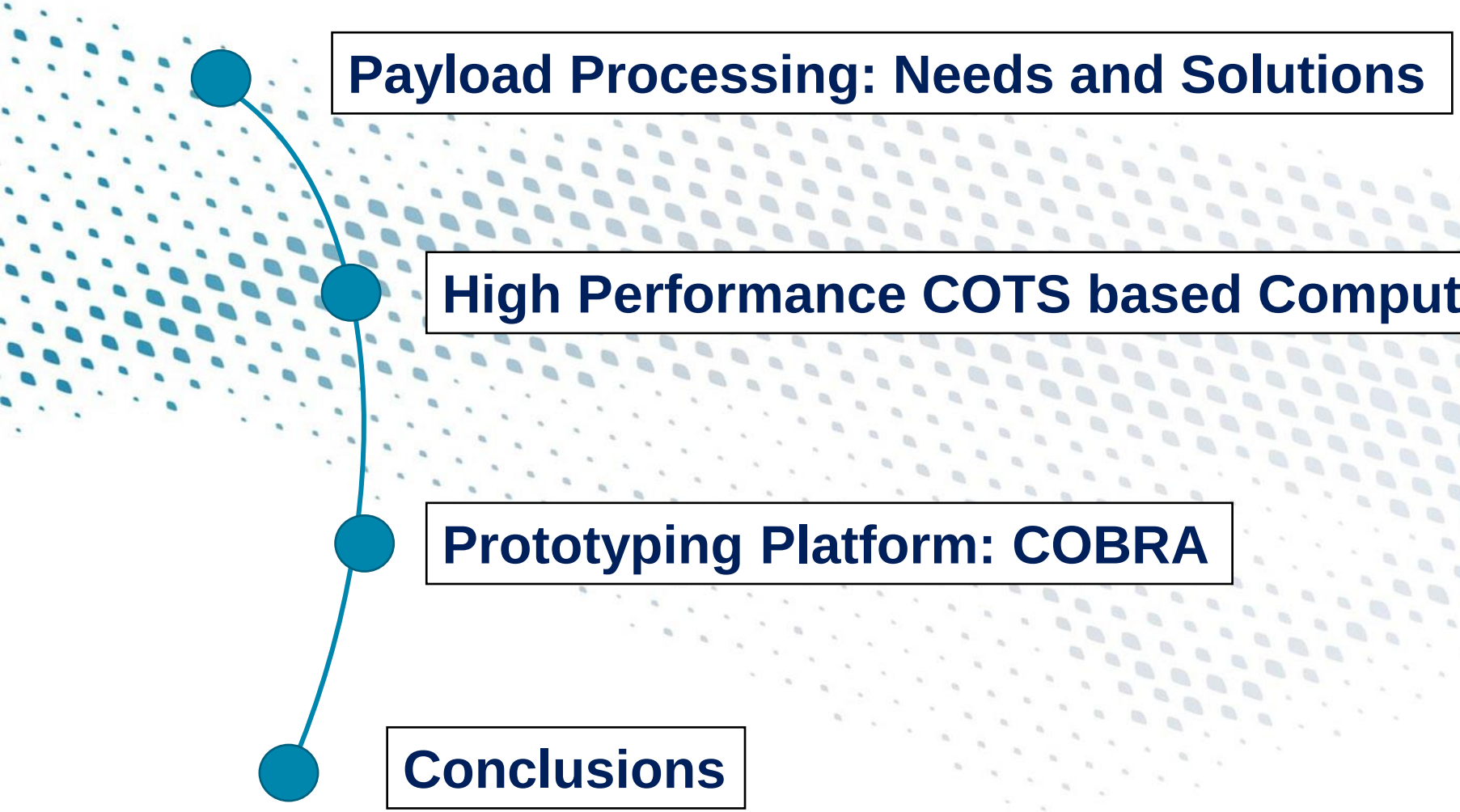
Marie RIMPAULT
Data Processing and On-Board Software – Airbus DS Toulouse

AIRBUS


Payload Processing: Needs and Solutions
High Performance COTS based Computer
Prototyping Platform: COBRA
Conclusions

Payload Processing: Needs and Solutions

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Payload Processing: Mission Needs

Need for higher on-board processing capabilities

New opportunities and innovations

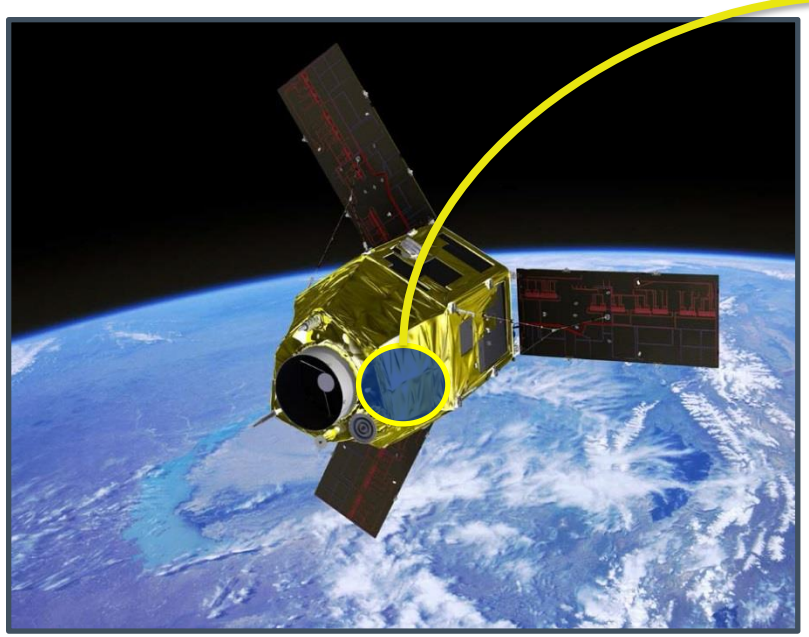
- Advanced image processing / vision based navigation applications
- Regenerative / demodulated telecom payloads

Increase on-board autonomy

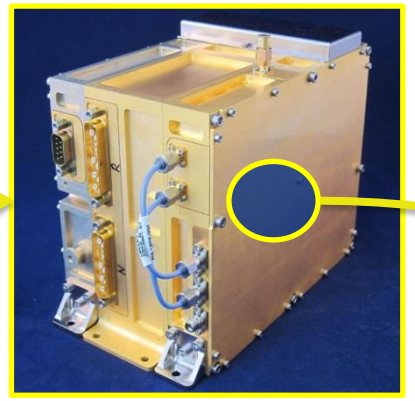
- Reducing the need for distant mission operation planning

Reduce the amount of information to be transferred to the ground segment

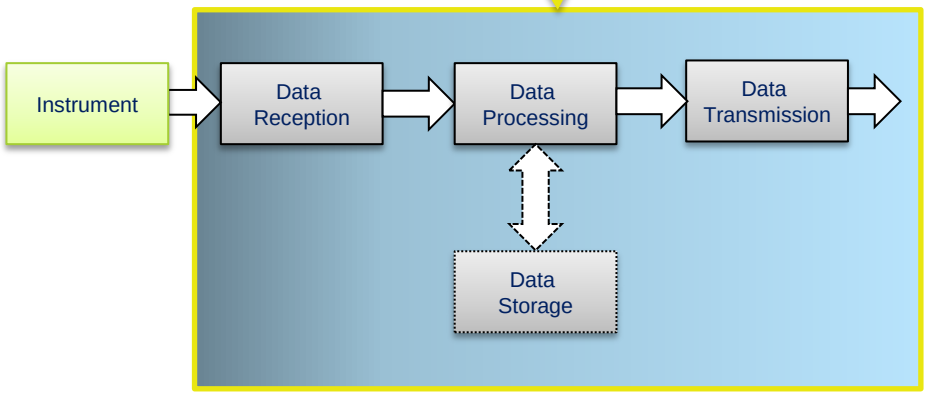
Payload Processing: Big Picture



Spacecraft

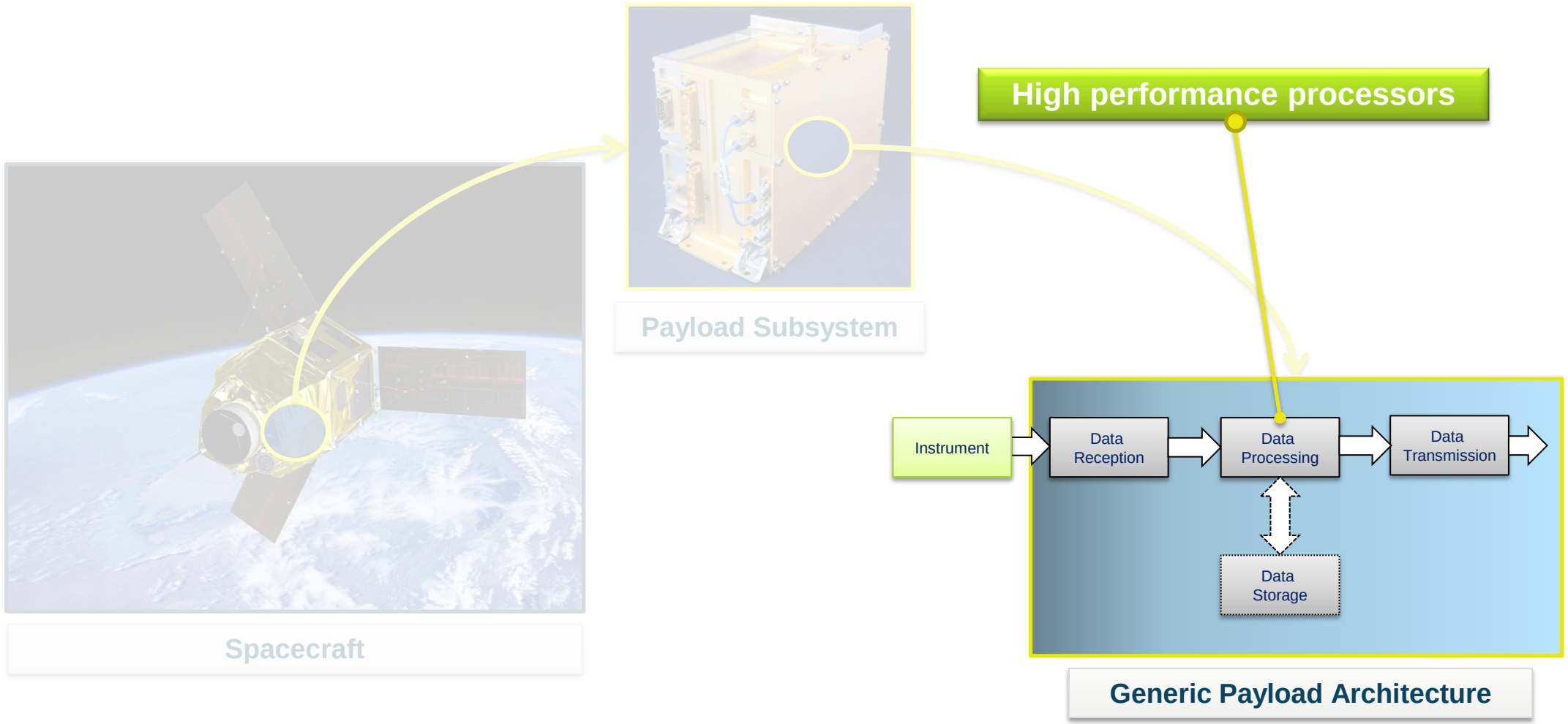


Payload Subsystem

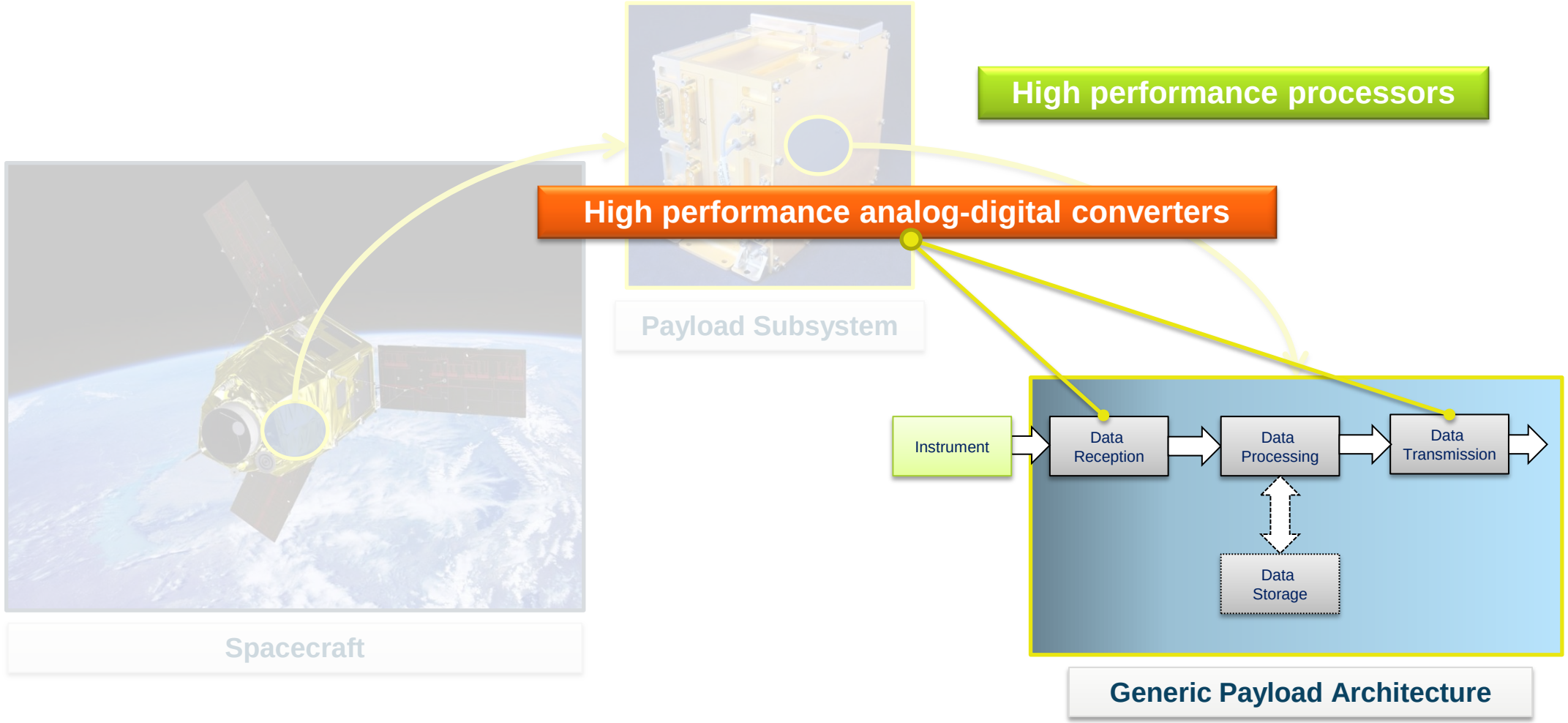


Generic Payload Architecture

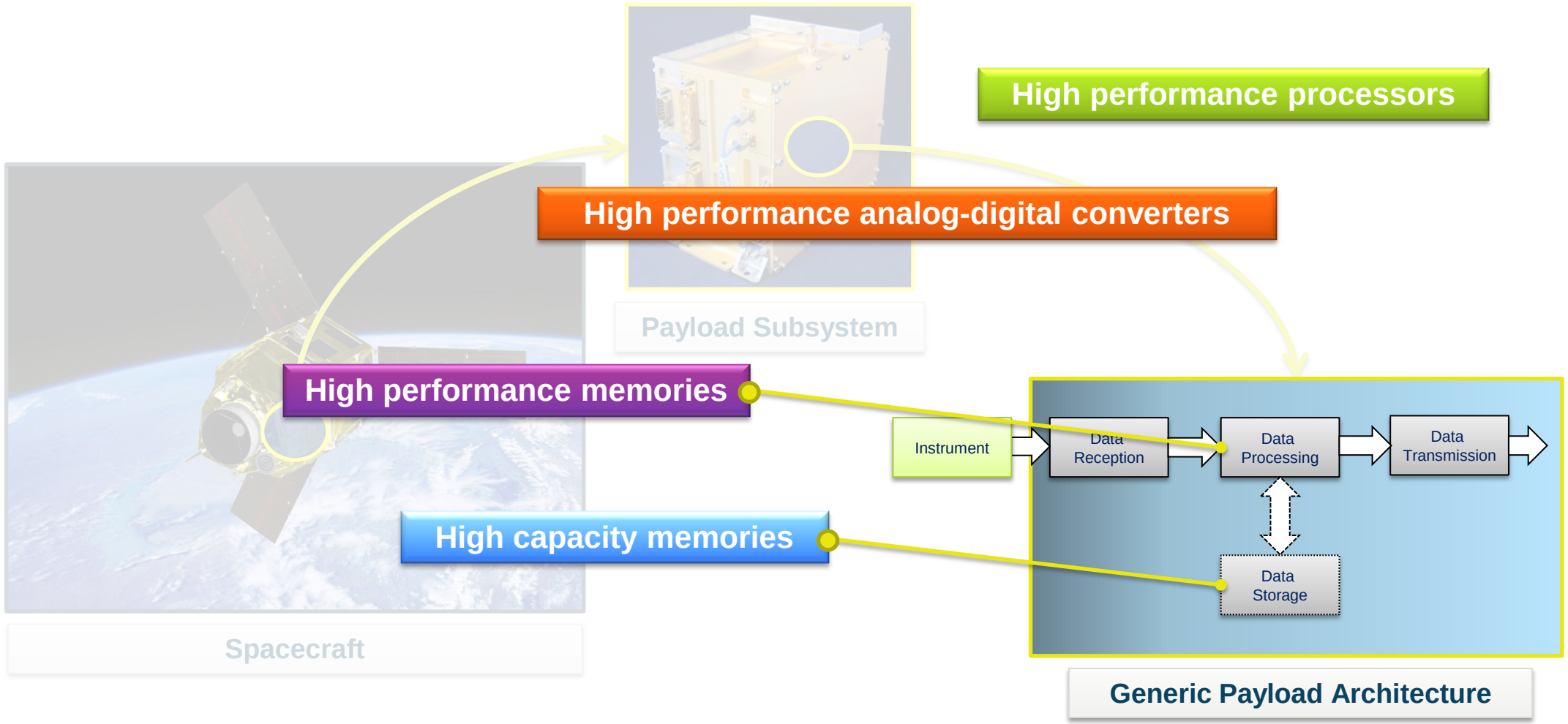
Payload Processing: Performance Needs



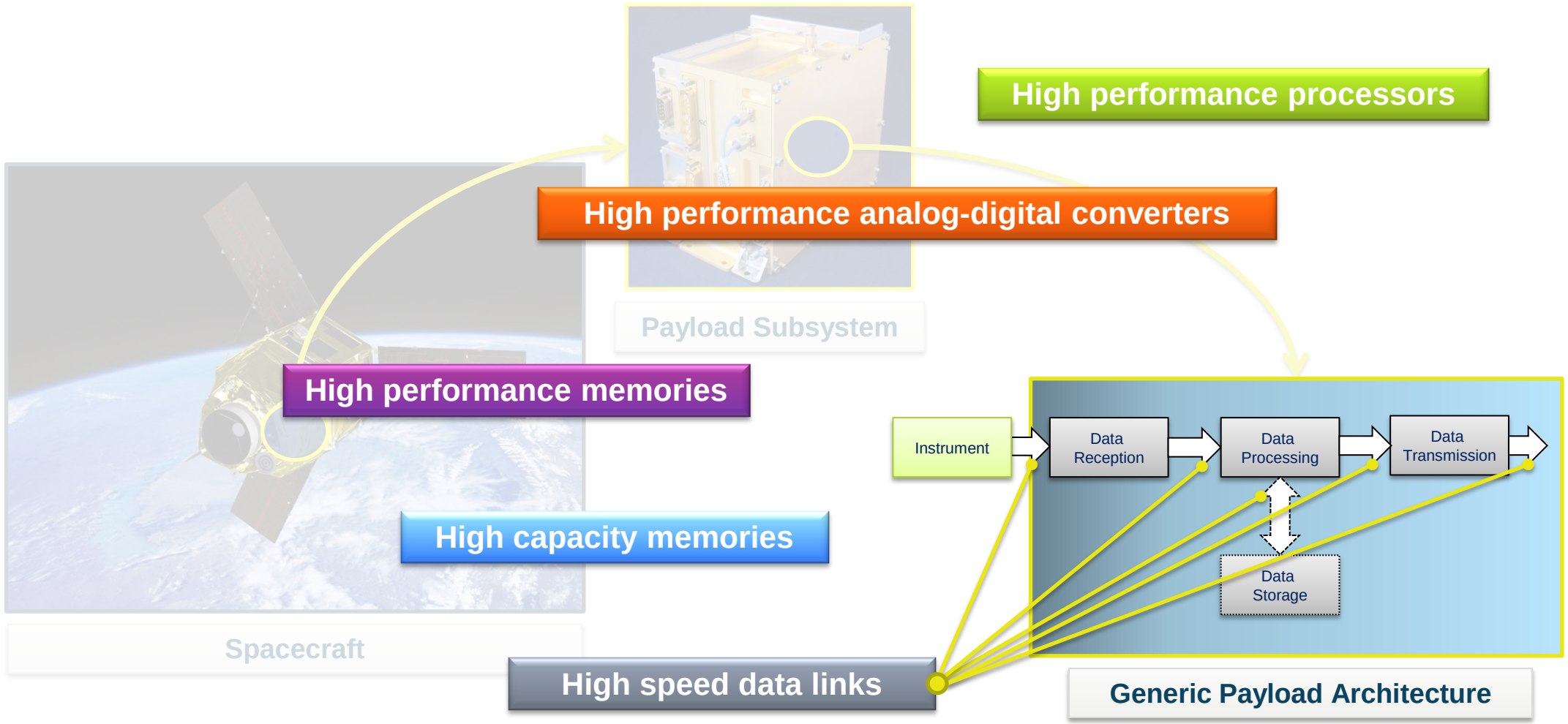
Payload Processing: Performance Needs



Payload Processing: Performance Needs



Payload Processing: Performance Needs



High Performance COTS based Computer

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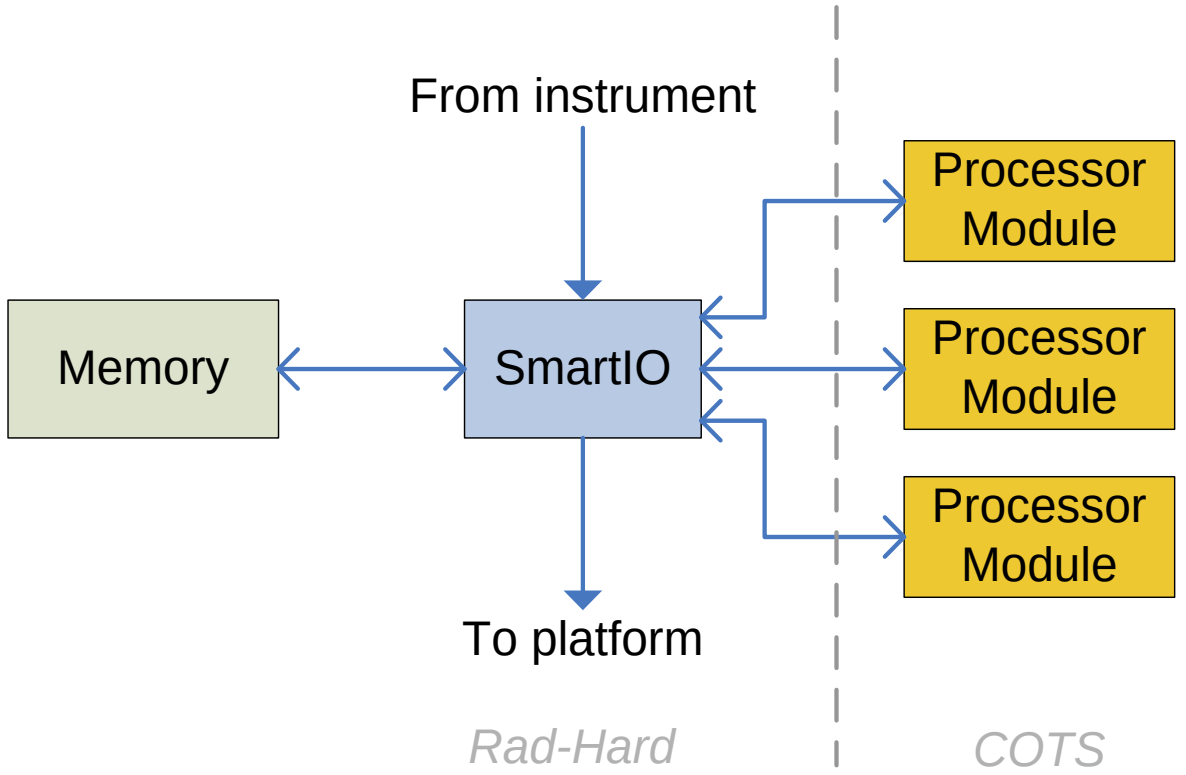
Mitigation Architecture: SmartIO Concept - Macro-mitigation

SmartIO

- Rad-hard component
  - In charge of the isolation between the COTS world and the rad-hard world
- Controls several COTS components
- Provides scalable fault mitigation and PM reconfiguration functions
- Buffers instrument data in a fast local memory, and replays it in case of error
- Acts as a master

Processor Modules

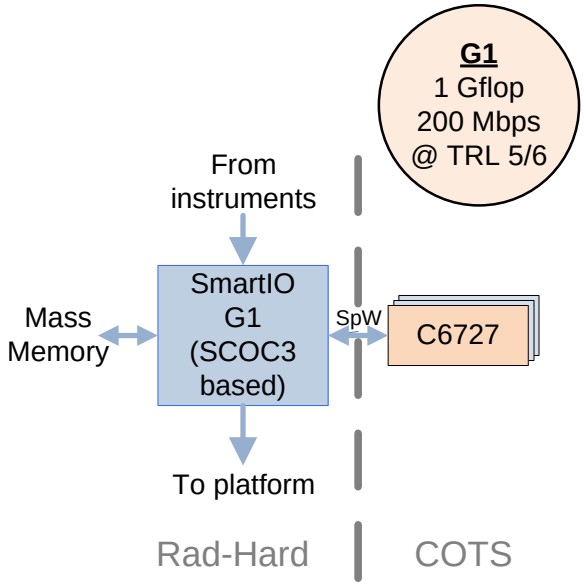
- Implemented with programmable devices (GPP, DSP, SoC, FPGA)
- Acts as slaves

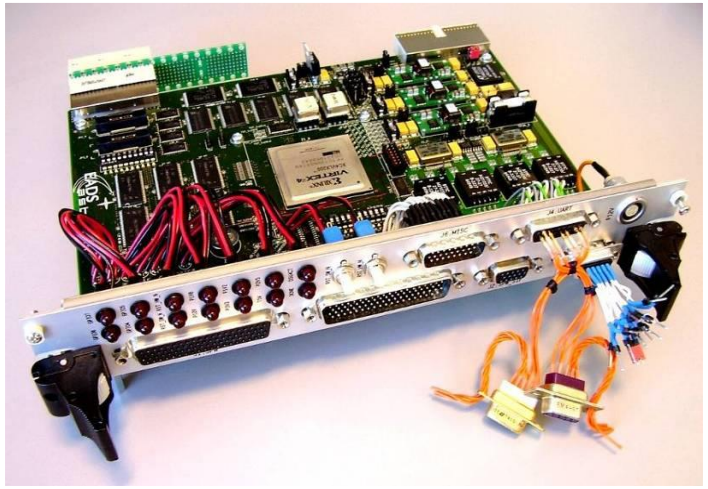


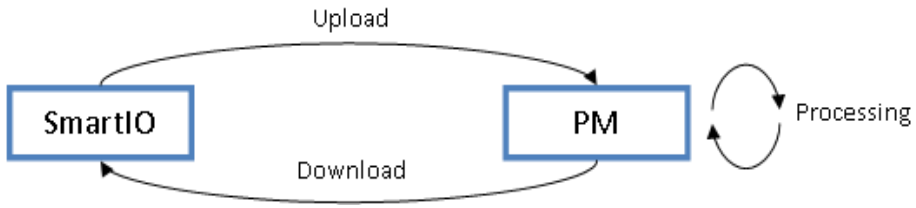
G1 Computer: HiP-CBC Demonstrator

HiP-CBC (ESA study)

- SmartIO fault tolerant architecture based on SCOC3
- Processor modules are C6727 DSPs
- TRL 5/6 demonstrator in 2014







Prototyping Platform: COBRA

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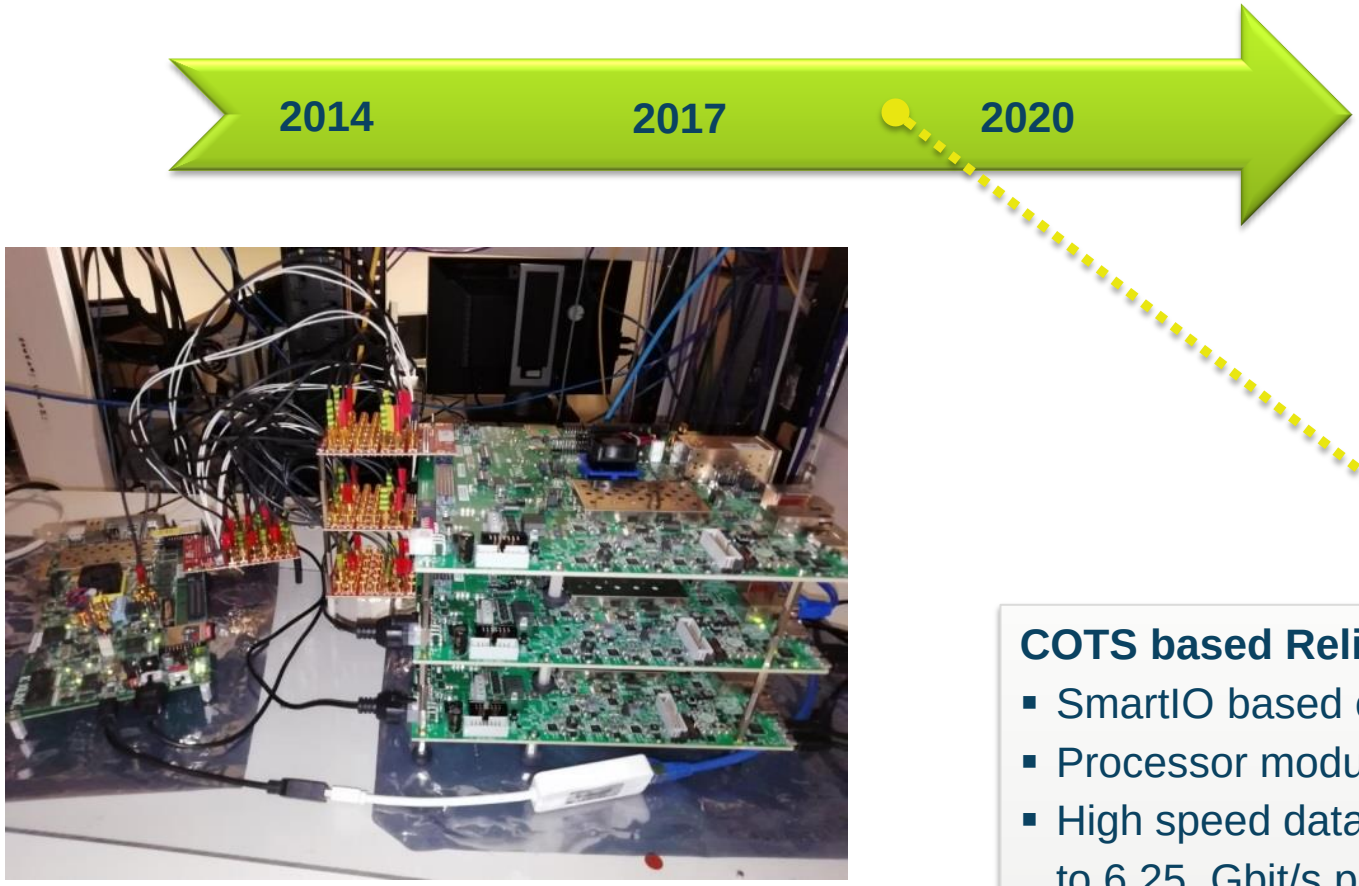
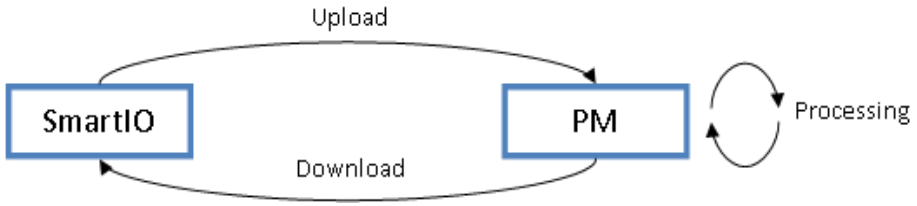
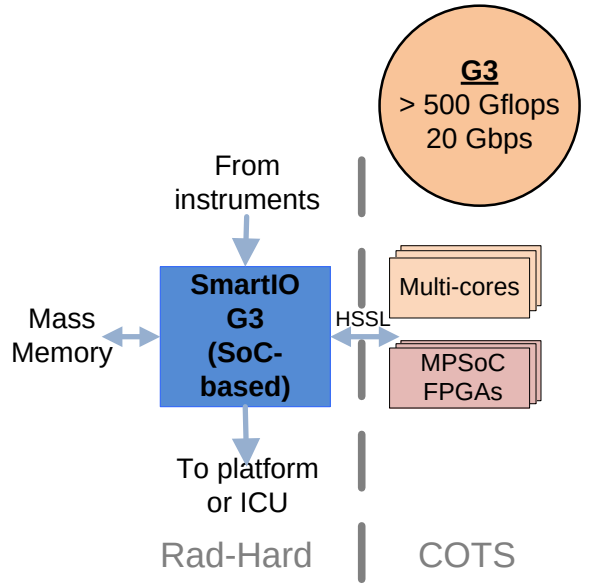
COBRA Demonstrator







COTS based Reliable Architecture (COBRA)

- SmartIO based on DAHLIA specifications
- Processor modules are MPSoC Zynq Ultrascale+
- High speed data links between SmartIO and PM (up to 6,25 Gbit/s per link)
- TRL 4 demonstrator

COBRA demonstrator : SmartIO

SmartIO demonstrator selection

- provide a prototype platform to develop BSP and HDL codes to de-risk the newer generation of the SmartIO
- As close as possible to the definition of the Dahlia (Nanoxplore NG-Ultra) to minimize the porting effort

ZYNQ architecture

- 2 ARM Cortex A9 cores @800Mhz
- processing performances 2.5 DMIPS/MHz
- a small or medium FPGA matrix
- HSSL 6.25Gb/s interface (Serial Rapid IO)

ZC706 board

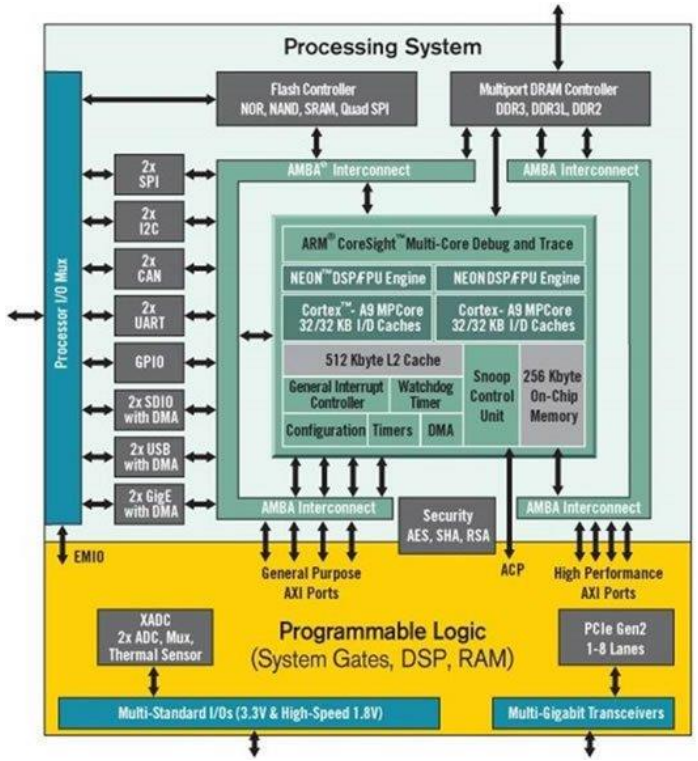
- Zynq-7000 XC7Z045 FFG900 – 2
- Video/ Display HDMI 8 color RGB 4.4.4 1080P-60 OUT
- DDR3 Component Memory 1GB (PS)
- DDR3 SODIMM Memory 1GB (PL)
- 2X16MB Quad SPI Flash (config)
- GigE RGMII Ethernet (PS)

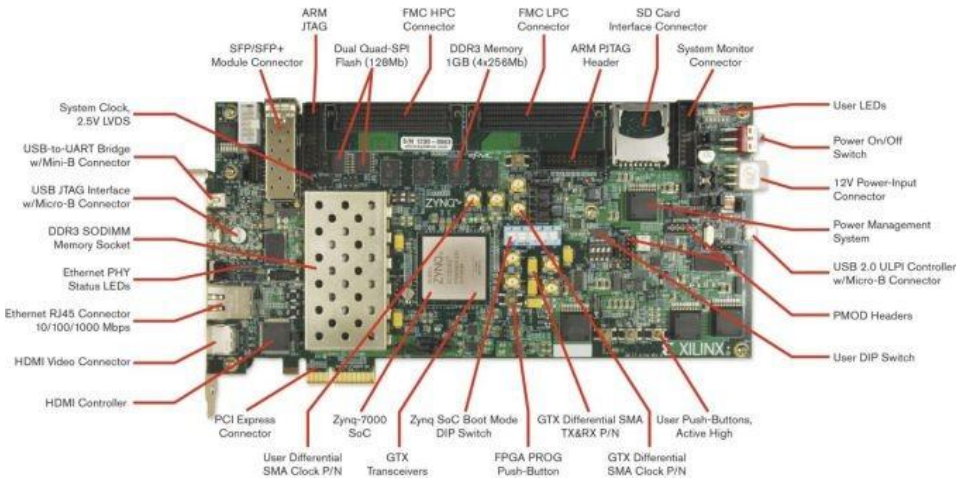
Tools :

Xilinx Vivado / Petalinux

OS

Linux





COBRA demonstrator : PM

PM selection

- latest SoC from Xilinx, providing a very fast and reconfigurable SRAM-based FPGA
- Up to 3 PM to allowing TMR configuration

ZYNQ Ultrascale+ architecture

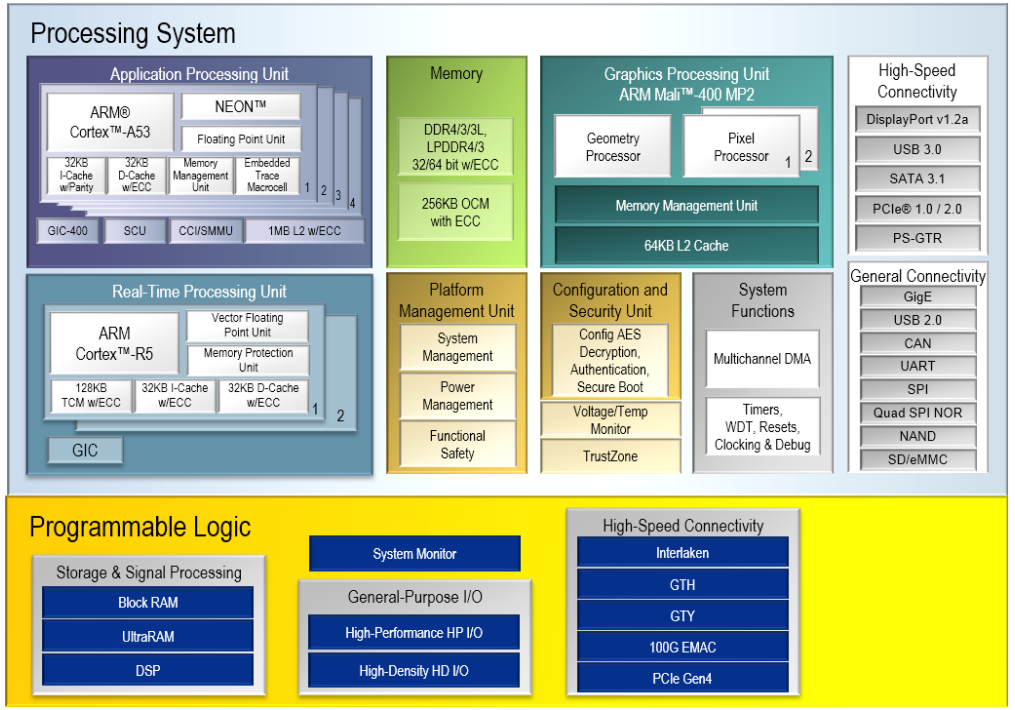
- ARM Cortex A53 @1,2 Ghz
- processing performances 10000 DMIPS
- Large FPGA (signal processing capability of at least 24 GMAC/s up to 705.6 GMAC/s)
- HSSL 6.25Gb/s interface (Serial Rapid IO)

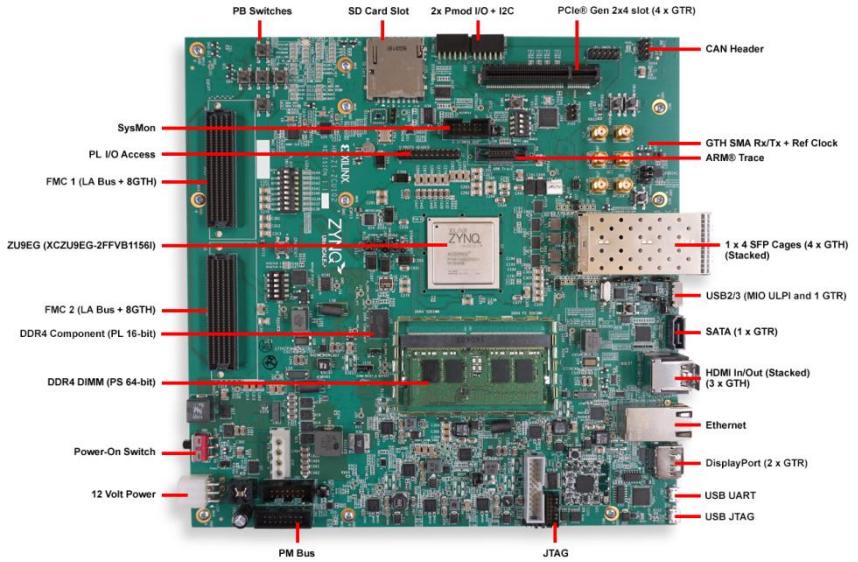
ZCU102 board

- Zynq UltraScale+ XCZU9EG-2FFVB1156-2
- DDR4 Component Memory 2GB (PS)

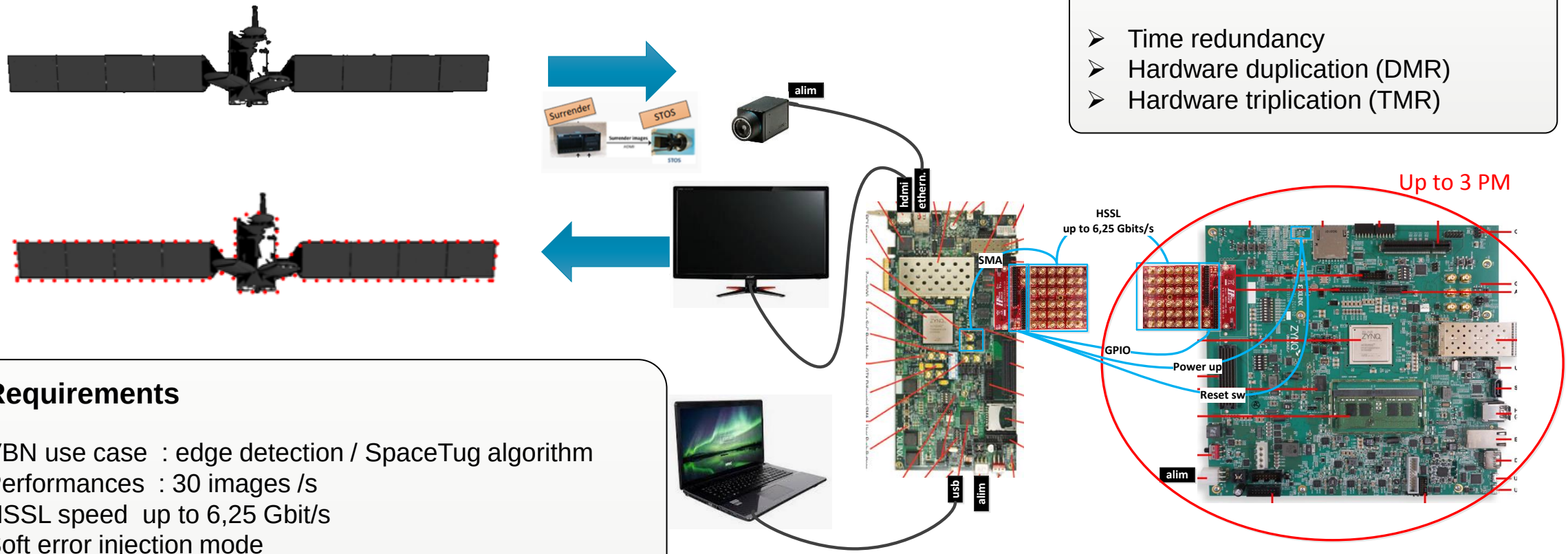
Tools

- Xilinx Vivado / Petalinux tool
- Xilinx SDSoc high level synthesis tool evaluation





COBRA demonstrator : VBN use case



Configurable Mitigation mode

- Time redundancy
- Hardware duplication (DMR)
- Hardware triplication (TMR)

Requirements

VBN use case : edge detection / SpaceTug algorithm
Performances : 30 images /s
HSSL speed up to 6,25 Gbit/s
Soft error injection mode

Power consumption :
- SmartIO < 5 W
- PM < 15 W

Low Recovery time
High to very high Availability depending on mitigation strategy

Conclusions

Conclusions

Prototyping Platform

- Early assessment to de-risk performance issues
- Flight SW and logic for application layers can be developed in parallel with HW equipment with appropriate methodologies (HW / SW Codesign)

Cobra demonstrator

- Final demonstrator available soon (results will presented at DASIA 2019)
- Very generic architecture adapted to Multi-mission application
- Architecture adapted for wide spectrum of applications
  - Software-defined radio (SDR) application
  - Software-defined image (SDI) application
  - Artificial intelligence (AI) application

Thank you

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