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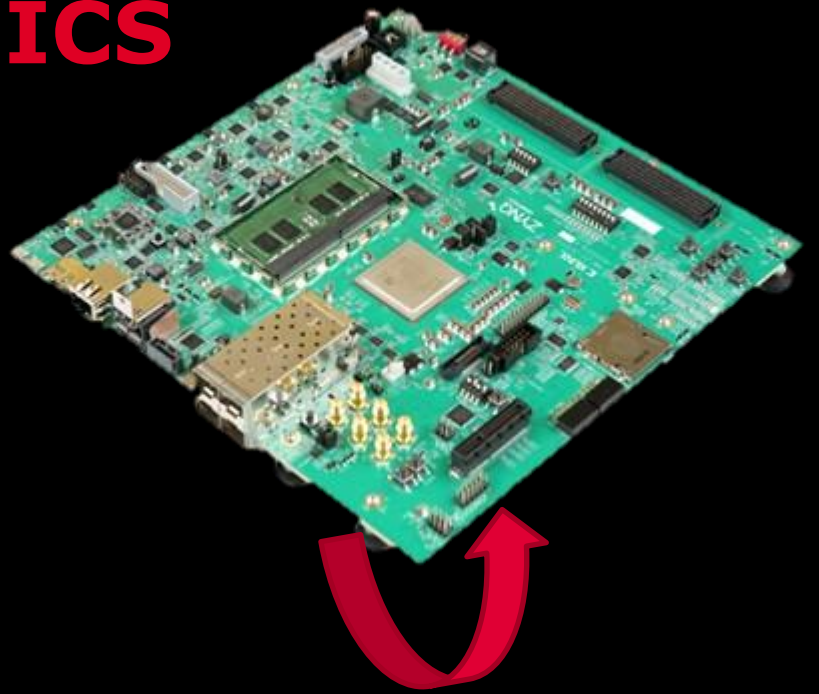
HW RECONFIGURABLE PROCESSING AVIONICS FOR SPACE VISION-BASED NAVIGATION



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CONTENTS

ENABLE-S3 PROJECT

- The project covers the supply value chain of the validation process for embedded processing in critical autonomous applications in industry:
  - Automotive
  - Aerospace
  - Rail
  - Maritime
  - Health care
  - Farming

- Aerospace UseCase8: Reconfigurable Video Processor for Space
  - Vision-Based Navigation in Space Exploration with mission planned FPGA Reconfiguration to interchange the Image Processing HW-accelerator depending on the distance to the target Asteroid and the criticism of the mission phase.
  - Environment Representative conditions emulated by fault-injection with self-healing FPGA reconfiguration in case of electronics degradation or Single Events problems detected

USE CASE INFORMATION

The system under test:

- is an industrial system that deals with cosmic radiation
- multicore architecture capable of in-flight configuration
- Payload data processing equipment, for video processing, and navigation cameras based on camera systems
- In charge of conditioning, processing images acquired by :
  - Earth observation satellites before transmission to the ground
  - any kind of spacecraft for navigation purposes

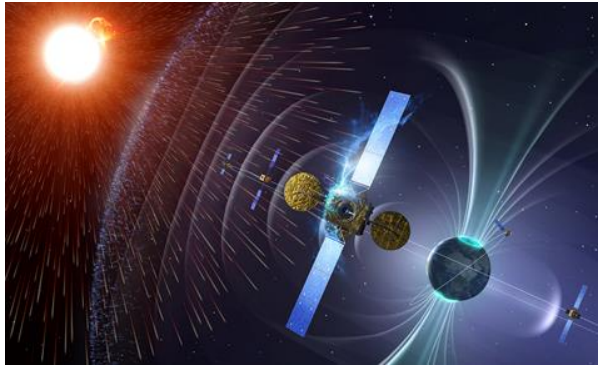
Participation from 5 partners :

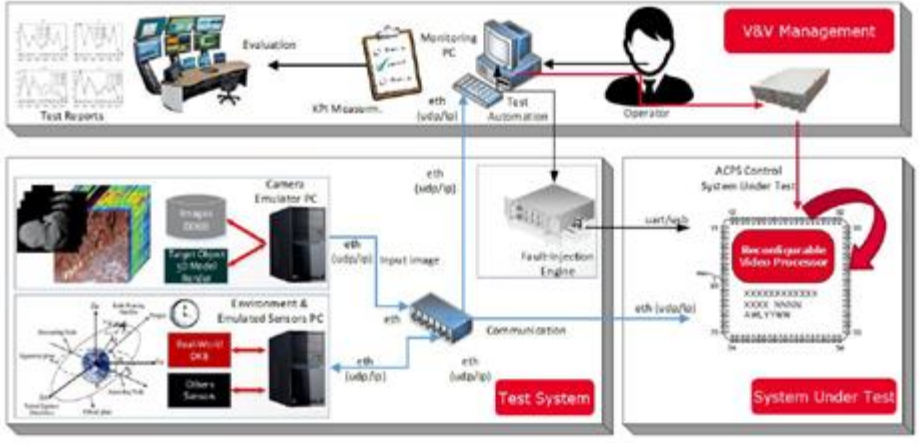
- GMV : GMV AEROSPACE AND DEFENCE SA UNIPERSONAL
- ITI : INSTITUTO TECNOLOGICO DE INFORMATICA
- ULPGC : UNIVERSIDAD DE LAS PALMAS DE GRAN CANARIA
- UPM : UNIVERSIDAD POLITECNICA DE MADRID
- TASE : THALES ALENIA SPACE ESPANA, SA

USE CASE OBJECTIVES

Demonstrating feasibility of the following elements:

- ❑ Autonomous Failure detection and reconfiguration features
- ❑ Autonomous video adaptability for space variable environment
- ❑ In-flight reconfigurable autonomous Vision-Based Navigation
- ❑ Compliance to Real-Time and dependability space constraints
- ❑ Radiation Tolerance with self-healing reconfiguration techniques





Space Challenge: Cost reduction and performance improvement

- Electronic Devices
  - Cosmic Radiation, Power consumption, miniaturized
- Test
  - Validation, Qualification, Functional & Performance Test

ENABLE-S3 V&V Architecture

- Simulators, Model, HW-in-the-loop
- Fault-injection vs Radiation Beam Facilities

USE CASE 8 – GMV VALIDATION

Previous V & V methodology

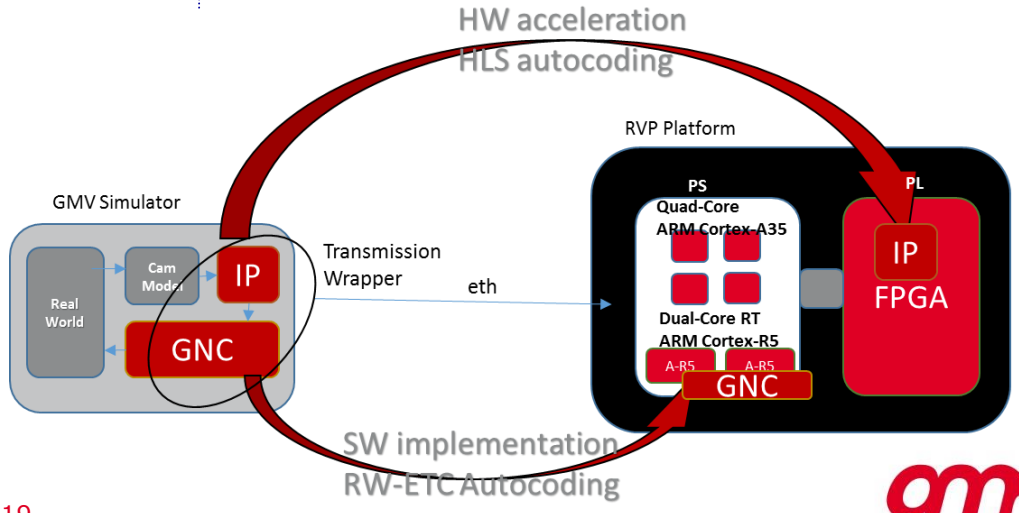
- Algorithms implemented in SW and HW
- V & V performed on HW-SW development
- V & V needs HW implementation in order to take place

Enable-S3 V & V steps. *Close loop V&V steps*

- MIL : Every module is simulated as a model
  - Model V&V
- SIL : GNC is auto-coded to C
  - SW V&V
- PIL : GNC is executed in target processor
  - *SW implementation / RW-ETC Autocoding*
  - Target Processor V & V
- FIL : Image Processing is auto-coded and executed in FPGA
  - HW acceleration / HLS autocoding
  - Final V & V

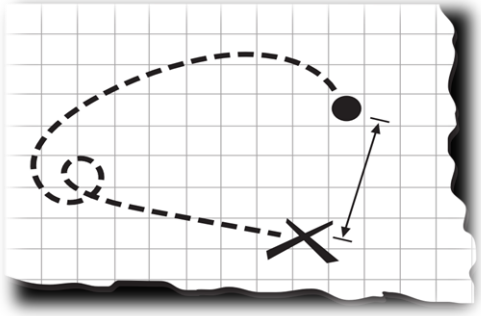
Benefits of the new approach:

- V & V starts in early steps
- V & V is performed in several steps
- Problems can be detected early
- Costs & Time saving



GMV IN ENABLE-S3

- General Enable-S3 architecture mapped to GMV specific work in the project
- GMV prepared 2 use cases. Mapping is provided to the use case#1.
  - Use-Case#1: Vision-Based Navigation in Interplanetary Mission with mission planned FPGA Reconfiguration to interchange the Image Processing Algorithm depending on the distance to the target Asteroid and therefore the criticism of the mission phase.
  - Use-Case#2: Stereo-Vision Tracking of a satellite with self-healing FPGA reconfiguration in case of electronics degradation or Single Events problems detected.
- Vision-Based Architecture is defined: FPGA+Processor including high-level interfaces.
- Validation and Verification Preliminary Methodology is defined
- GNC filter SW in Simulink (with DKE simulation)
- Simulator for asteroid render for images generation
- Vision-Based Navigation techniques survey and SW implementations
  - HW-acceleration of image processing and matching
    - FPGA porting of those algorithms into VHDL developments
    - VHDL developments integrated into reconfigurable architecture
    - FPGA-CPU intercommunication
- HW-in-the-loop test campaigns including FPGA, CPU, Simulators/Emulators
  - High TRL only possible with representative environment or flight proven



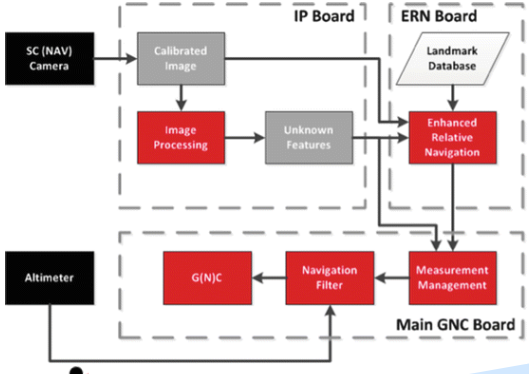
HW-RECONFIGURATION APPROACH IN INTERPLANETARY VISION-BASED NAVIGATION

		Tasks With only SW in PS				Tasks With HW acceleration parts in PL				
	TASKS	TEST SYSTEM MONITORING	SYSTEM MANAGEMENT AND DATA HANDLING	GNC	FAULT DETECTION AND RECONFIGURATION	RELNAV IP	ABSNAV IP	LIMBFIT-NAV IP	HYPERSPECTRAL COMPRESSION	LOC & MAP IP
	MODES	ACTIVATION								
1	COASTING	x	x							
2	SCIENTIFIC USE	x	x		x				x	
3	NAVIGATION INIT	x	x	x	x			x		
4	ABSOLUTE NAVIGATION	x	x	x	x		x			
5A	BRAKING PHASE NAV-A	x	x	x	x	x				
5B	BRAKING PHASE NAV-B	x	x	x	x		x			
6	RELATIVE NAVIGATION	x	x	x	x	x				
7	TERMINAL DESCENT	x	x	x	x					
8	LANDING OPERATIONS	x	x							x
9	MODE CHANGE	x	x	x	x					
10	ERROR RECOVERY		x		x					

x: Activated

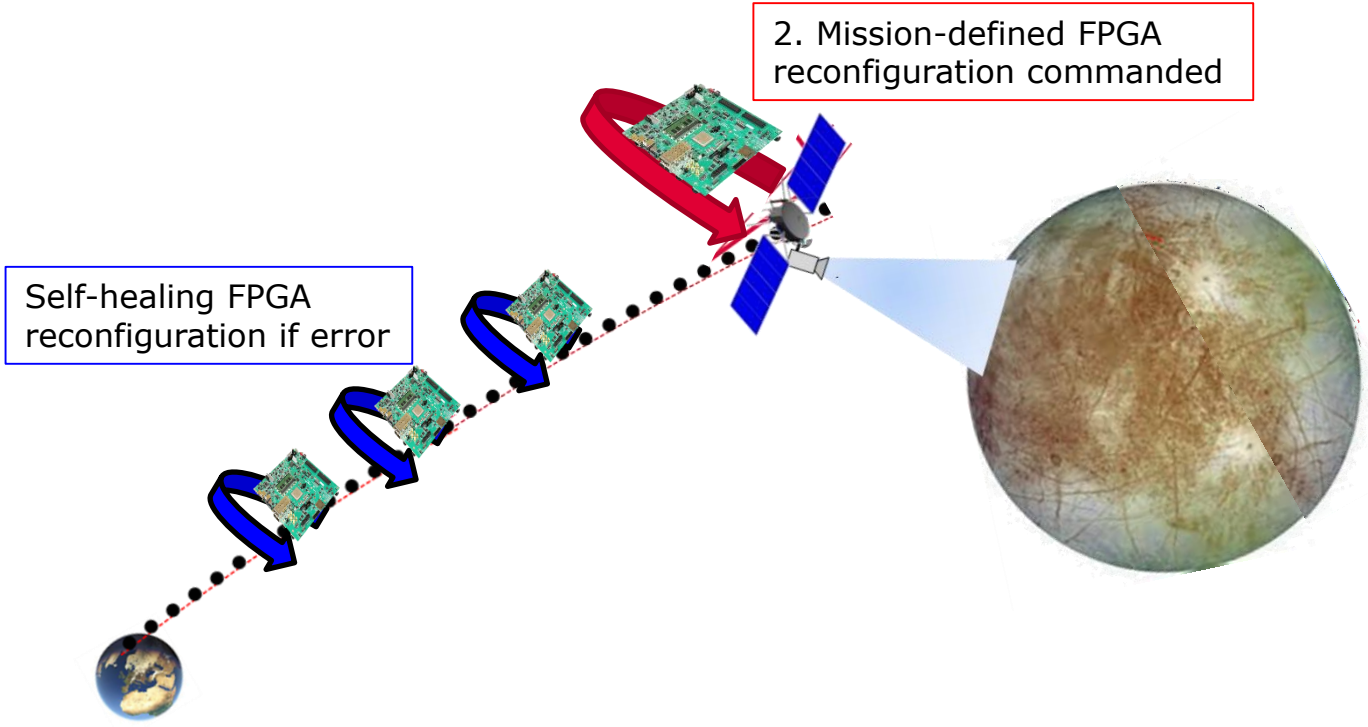
HW-RECONFIGURATION APPROACH: IMAGE PROCESSING ACCELERATED IN FPGA

1. FPGA-based image processing in far-range feeds Guidance, Navigation and Control system with centroiding-like LOS

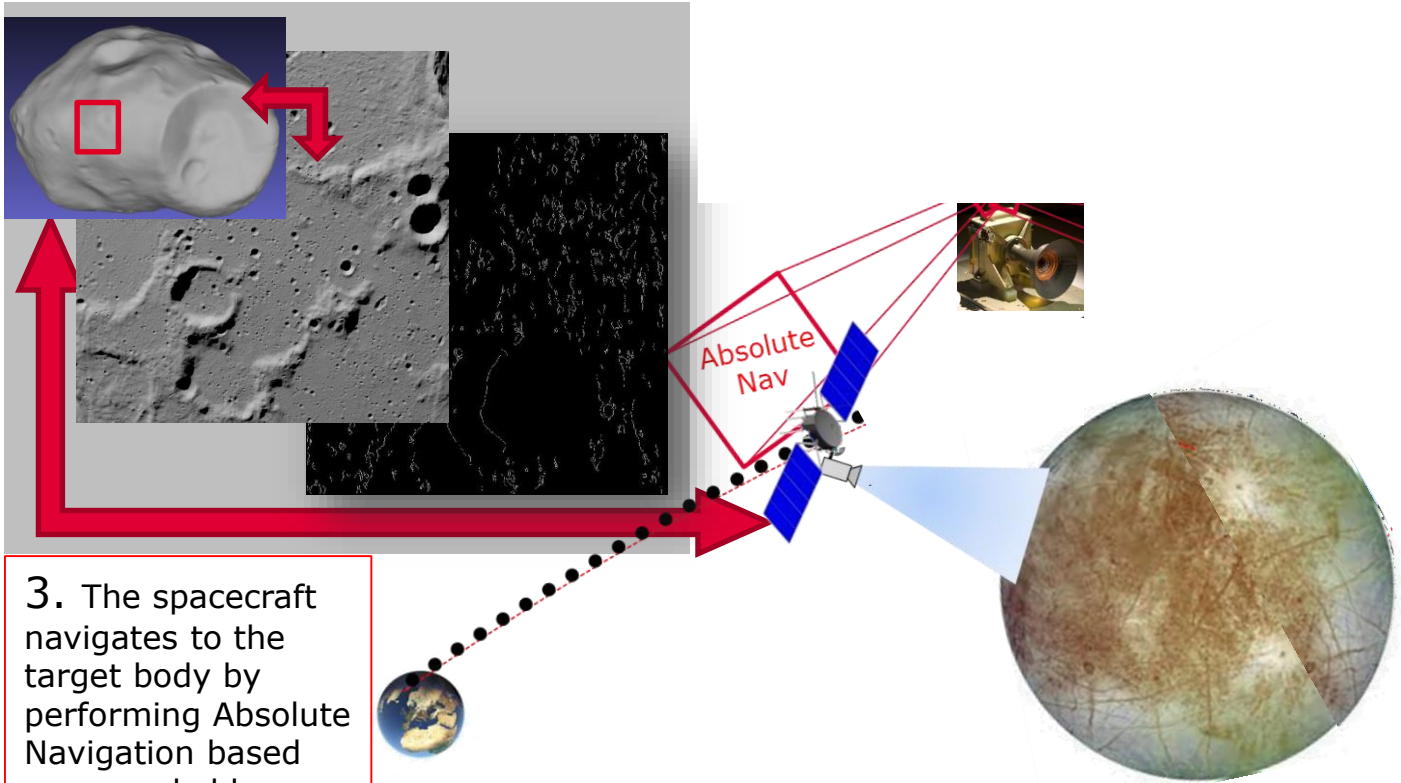


Limb Fitting

HW-RECONFIGURATION APPROACH: SELF-HEALING VS PLANNED

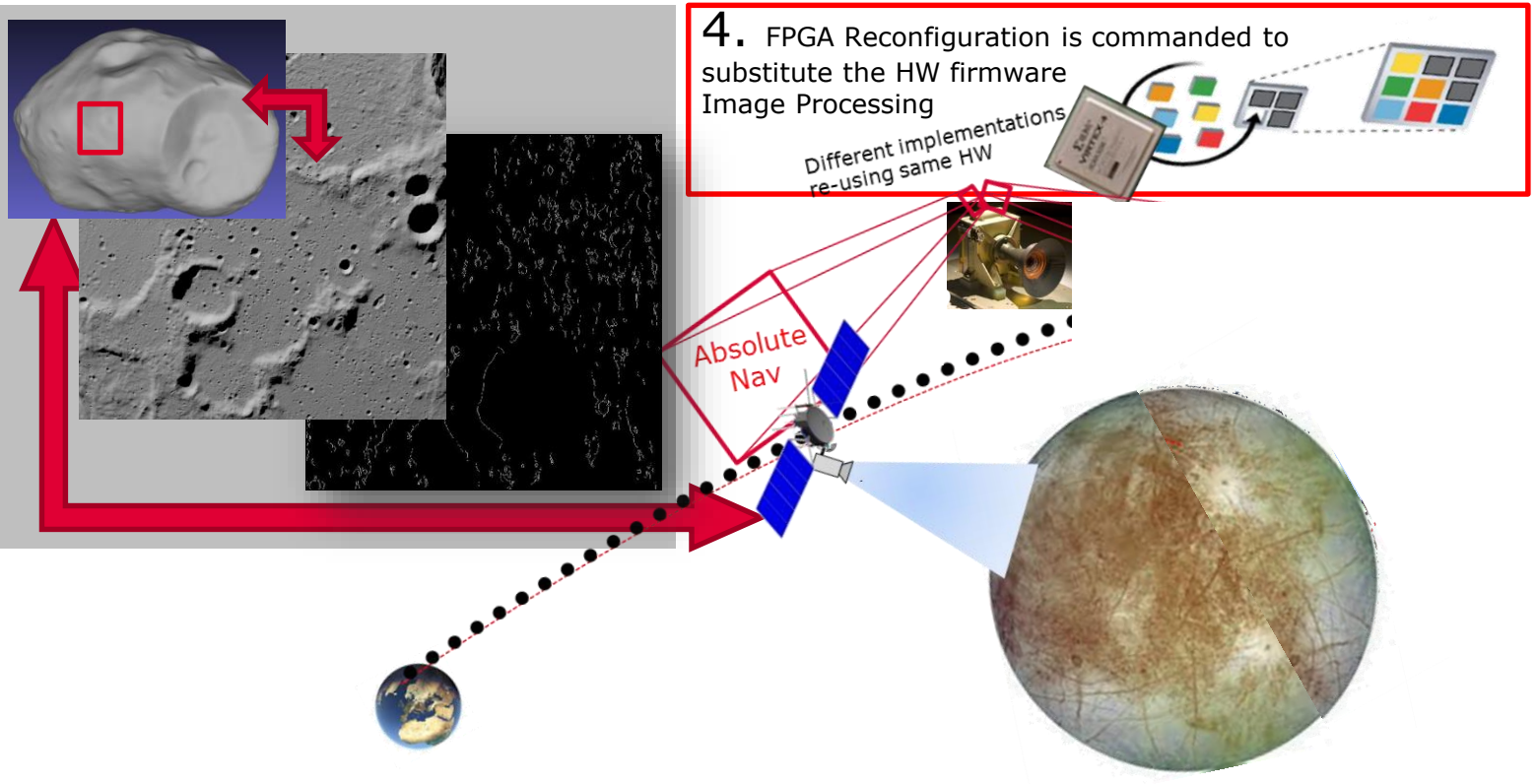


HW-RECONFIGURATION: PROXIMITY PHASE



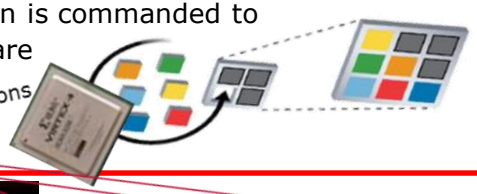
3. The spacecraft navigates to the target body by performing Absolute Navigation based on remarkable landmarks to match with a data-base

HW-RECONFIGURATION: PROXIMITY PHASE

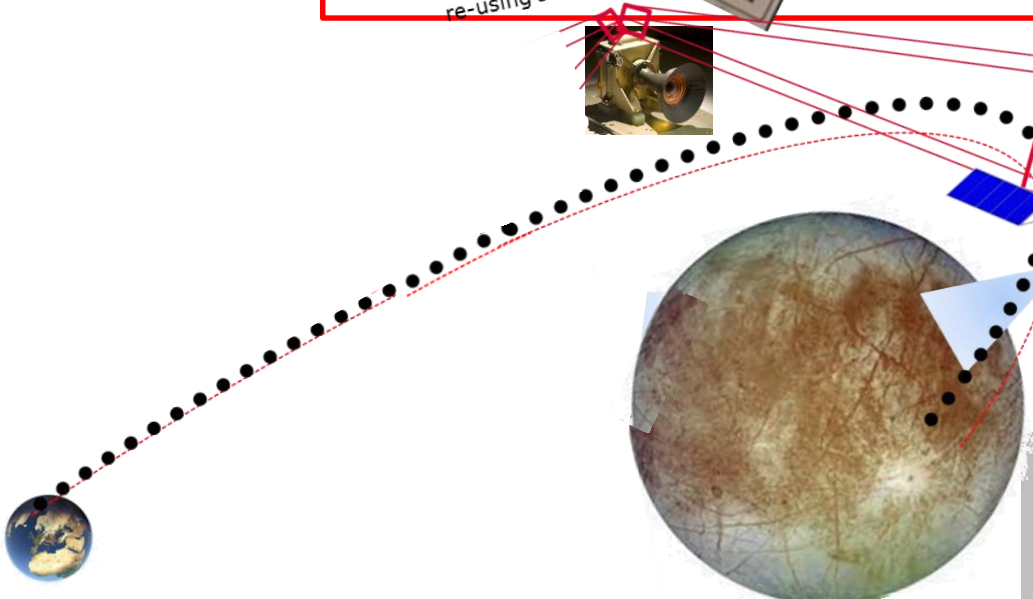


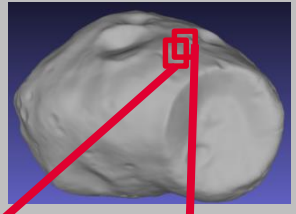
HW-RECONFIGURATION: DESCENT

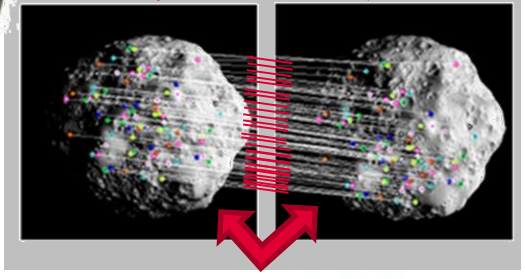
4. FPGA Reconfiguration is commanded to substitute the HW firmware Image Processing



5. Final part Descent & Landing using Relative Navigation VBN tracking unknown features between consecutive images.







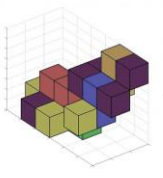
RECONFIGURABLE VIDEO PROCESSOR

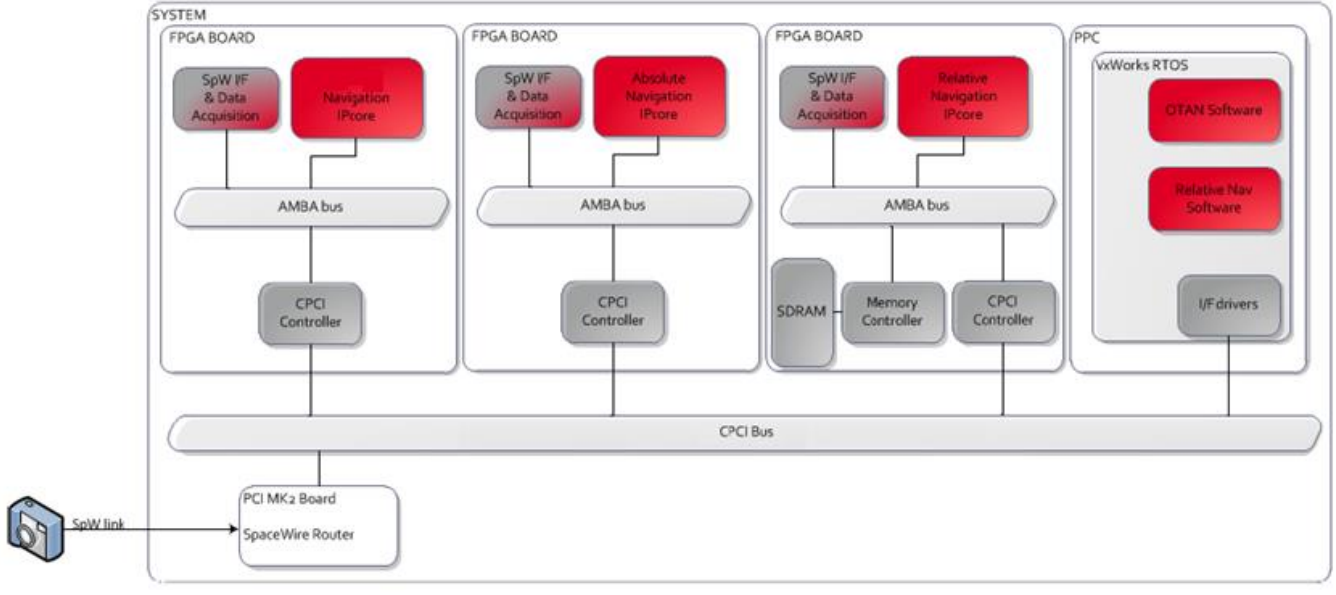
HW-SW Co-Design

- ❑ 3 FPGAs
- ❑ On-Board Computer

Image processing algorithms:

- ❑ Limb Fitting
- ❑ AbsNav
- ❑ RelNav





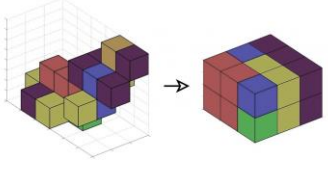
RECONFIGURABLE VIDEO PROCESSOR

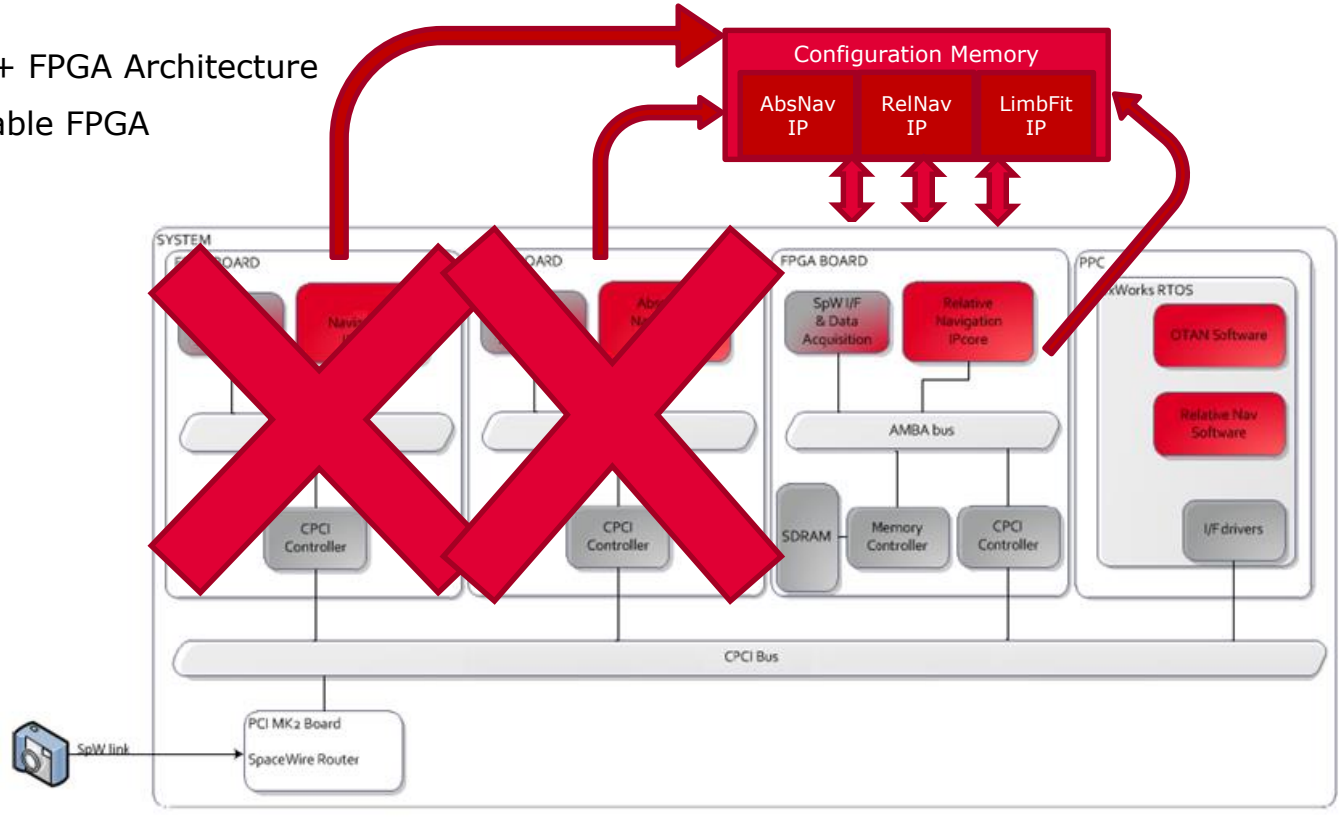
System-on-Chip : Processor + FPGA Architecture

- ❑ 2/3 FPGAs → 1 Reconfigurable FPGA
- ❑ Save Payload Mass/Volume

Image processing algorithms

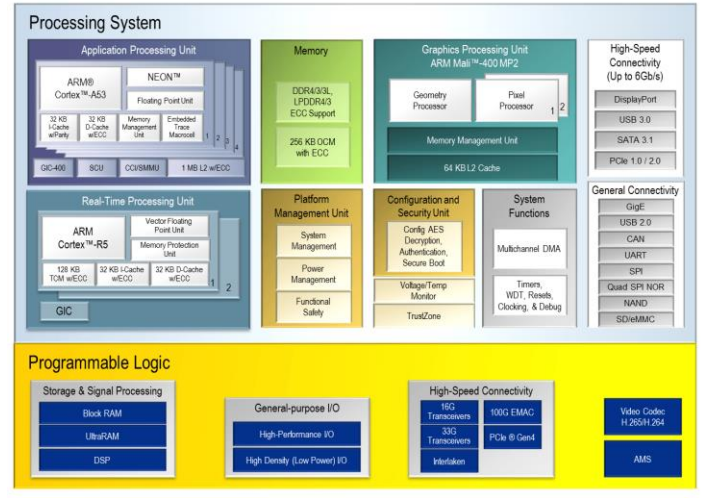
- ❑ Limb Fitting
- ❑ AbsNav
- ❑ RelNav





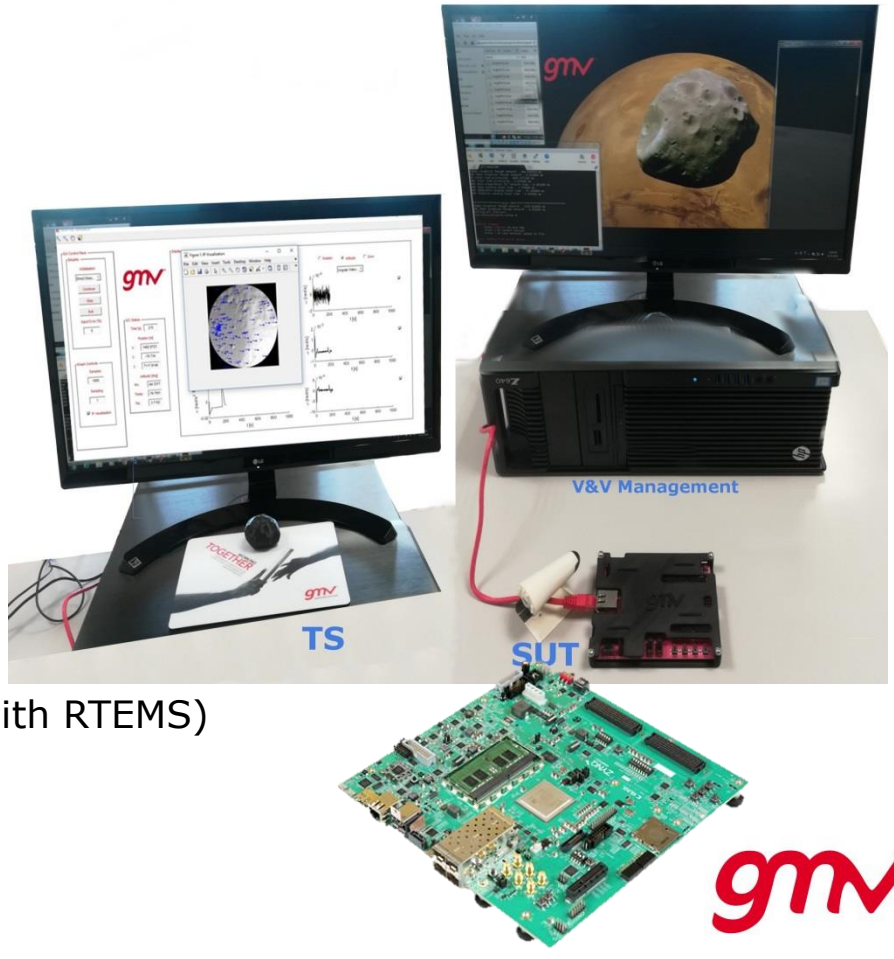
RECONFIGURABLE PLATFORM

- MPSoC including FPGA logic and real-time SW processor
  - From Zynq 7020 to Zynq Ultrascale+ ZU19
  - ZU+ includes dual-core R5 in lock-step
  - BRAVE FPGA includes R5 embedded in the chip
  - ARM4Space and DAHLIA in the roadmap for Space
- We defined and implemented a demonstrator including RTEMS planned modes and tasks for the defined use-case scenario.
- We implement HW accelerators modules constraint to architecture reconfigurable blocks of the FPGA and implements the critical SW managing navigation in the different phases
- Universidad Politécnica de Madrid provides the architecture that allows FPGA reconfiguration.
- SRAM-based FPGAs allow high-performance complex and resource-hungry applications be accelerated, but this technology is more susceptible to SEU/SEE radiation-induced faults.



GMV DEMONSTRATOR

- MIL ⇢ SIL ⇢ PIL ⇢ HIL
- Images Data Sets : Inputs for the VBN
- GMV-DL-Simulator used for
  - Input data control
  - Validation of results
  - Pixel error injection
  - Close-loop
- 2 HW PLATFORMS Evaluated (SUT)
  - Zynq 7015
  - Zynq Ultrascale+
    - (FPGA logic + ARM R5 lock-step with RTEMS)
- Test System (TS)
  - Spacecraft data generation



CONCLUSIONS

- FPGA dynamic partial reconfiguration architecture with fault tolerance capabilities is tested for vision-based navigation in space allowing multiple complex HW-accelerators to co-exist in only 1 FPGA in the cases where 3 FPGAs would be needed without reconfiguration
- FPGA monitoring for self-healing by partial reconfiguration adds robustness to the system.
- Validation and Verification Framework of ENABLE-S3 allows more efficient testing campaigns of critical autonomous embedded systems
- The GNC meets precision landing requirements and stable behaviour even in harsh environment allowing robustness to different illumination conditions
- Real-Time performance can only be achieved by designing proper HW architecture for the Vision-Based Navigation System and the corresponding reconfiguration platform
- HW demonstrator of the system prototype will be implemented using flight-representative HW including equivalent space-grade version of the architecture boards
- This implementation and validation methodology will cause a cost reduction due to an early error detection process

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THANK YOU

D. Gonzalez-Arjona, A. Jimenez-Peralo, M.A. Verdugo, A. Pastor, R. Domingo; E. de la Torre, A. Otero, A. Perez, A. Rodríguez

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