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ON-BOARD COMPLEX IMAGE PROCESSING BASED ON FPGA ACCELERATION FOR AUTONOMOUS NAVIGATION IN SPACE

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CAMPHORVNAV

- Project within MREP Program
  - Part of Phobos Sample Return Mission (PhSR)
  - Vision-Based Navigation Camera (VBNC) providing three modules:
    - COU BB (Camera Optical Unit)
    - IPB EM (Image Processing Board)
    - Image Processing algorithms Firmware
  - VBNC used in the Descent & Landing Phase to Phobos
  - TRL6
- Extended with lessons learned from QUEENS-FPGA
  - Quality assessment Evaluation of European NanoXplore SW for brave FPGA

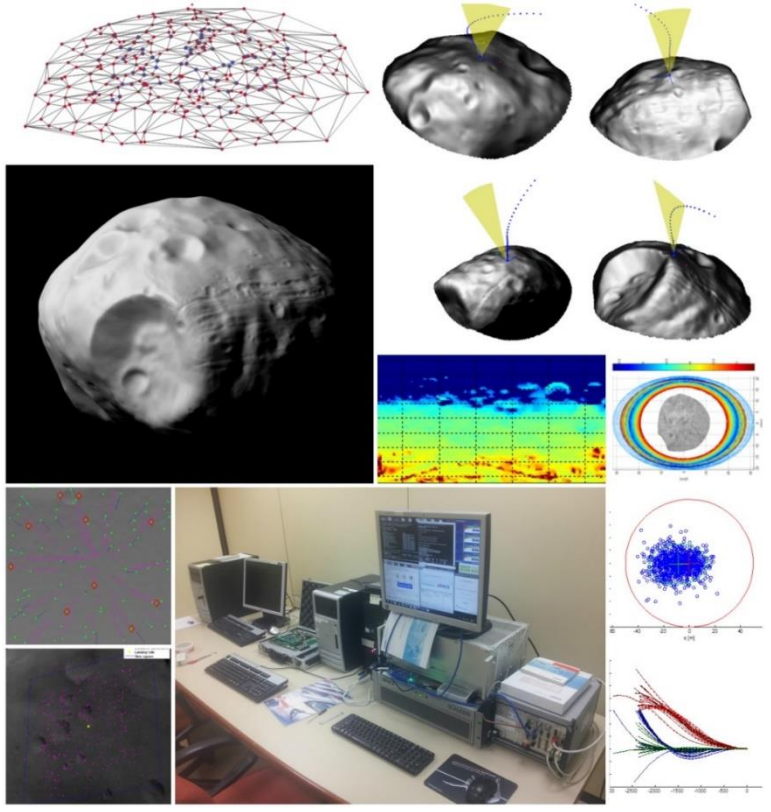
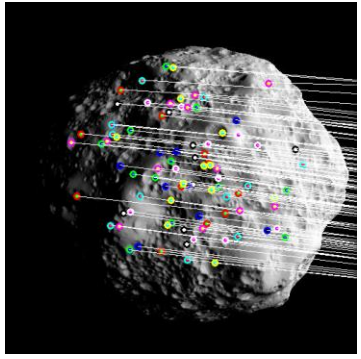
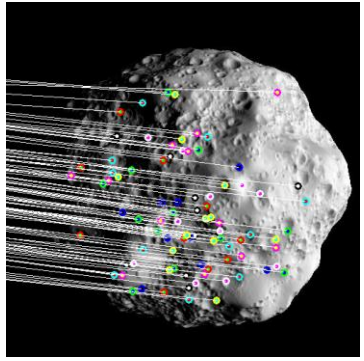
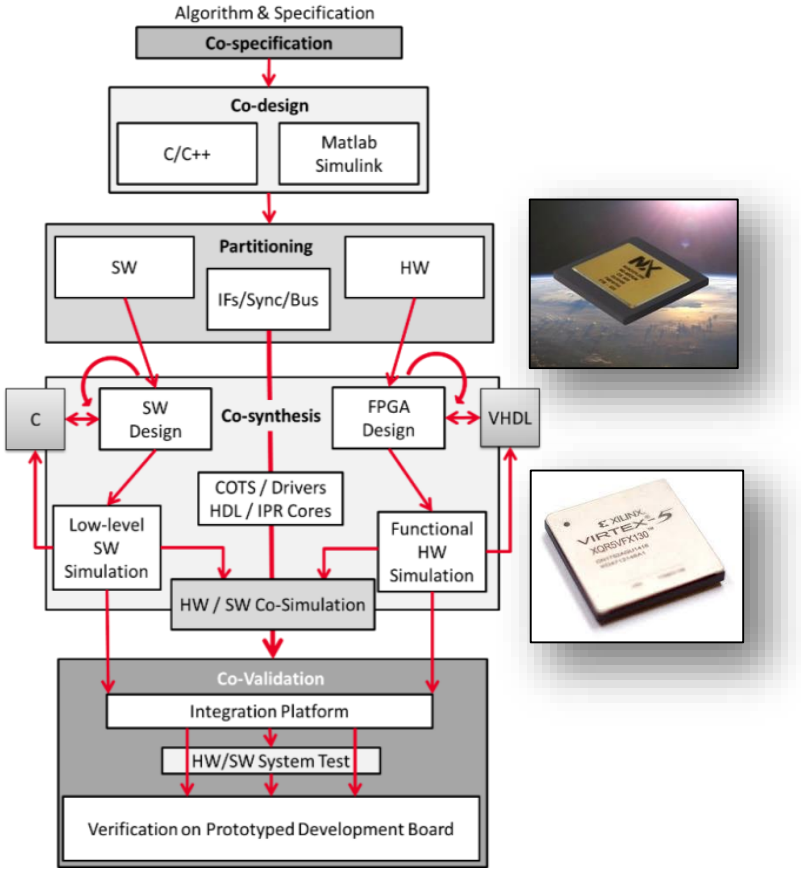


IMAGE PROCESSING HW ACCELERATION

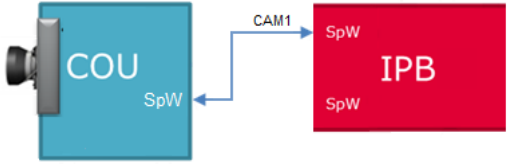
- Used in the D&L Phase
- HW/SW Co-design approach
- GNC implemented in LEON4
- Image Processing Board
  - 2 FPGAs: Virtex5 and NG-MEDIUM Rad-Hard FPGAs
  - Based on Feature Tracking HW-acceleration
  - Algorithm control & commands in LEON4
  - Camera and OBC Interfaces Management in FPGA



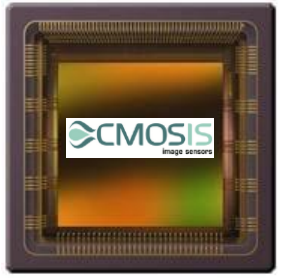




COU BASELINE

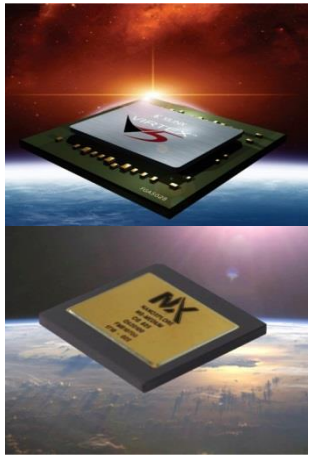


- SpaceWire I/F with the IPB → CCSDS/PUS Tailoring to allow re-use compatibility
- Design Based on CMV4000 → 2048x2048 pixels of 8-12bits
  - CNES radiation tests campaigns available
  - Same detector as in PILOTB+ Lunar Lander scenario (Requirement established by ESA in the ITT)
- COU is used for two scenarios, scientific and navigation, with trade-off decisions to better fulfill their different requirements:
  - For QSO Operations cropping Center 1024x1024 pixels provide a 10 degrees FoV
  - For Descent & Landing Binning the 2048x2048 to 1024x1024 provides 20 degrees FoV



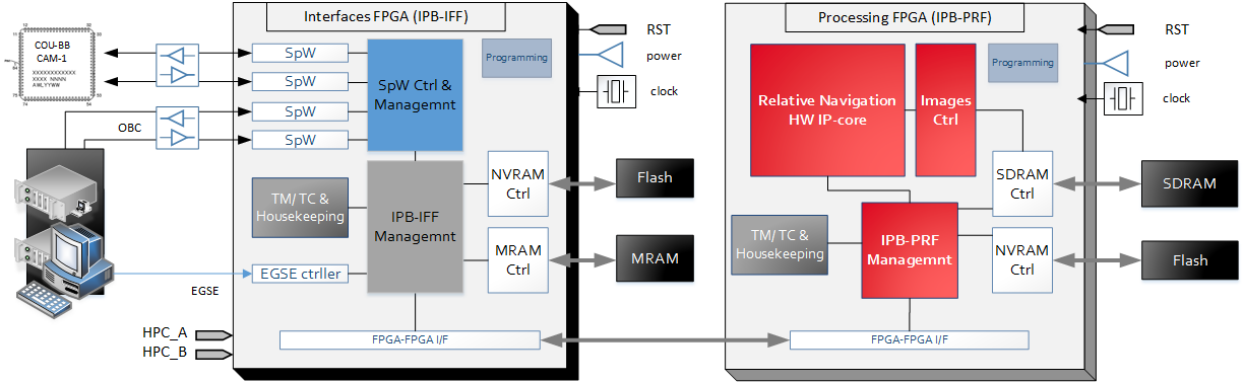
- ProAsic3 FPGA implements read-out, transmission and low-level image pre-processing
  - Bias/Gain Frame correction
  - Bad Pixel Correction
  - Binning/Cropping
  - GMV Demonstration on NG-MEDIUM inside IPB
- COTS Optics used of 35 mm
- TRL5 for the Cameral Optical Unit Breadboard implemented by MCSE partner

IMAGE PROCESSING BOARD



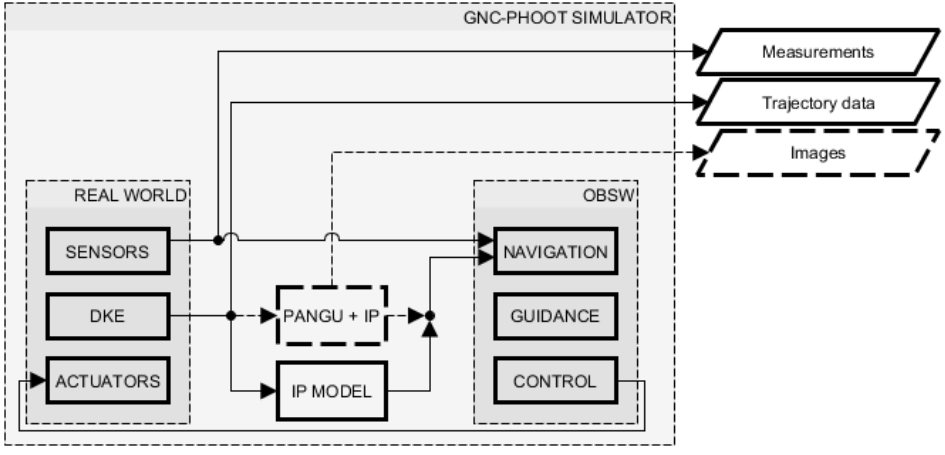
- Processing FPGA: Image Processing HW IP-core (high-performance & high-density SRAM-based FPGA)
  - Virtex-5 VFX130T
  - Memory controllers
  - Hosts RelNav IP
  - Data Acquisition and Synchronization
  - FPGA-FPGA parallel communication

- Interfaces FPGA:
  - NG-Medium
  - Image Pre-Processing Capabilities (Camera corrections)
  - Deals with the interfaces of the IPB to the external world (smaller Flash-based FPGA)

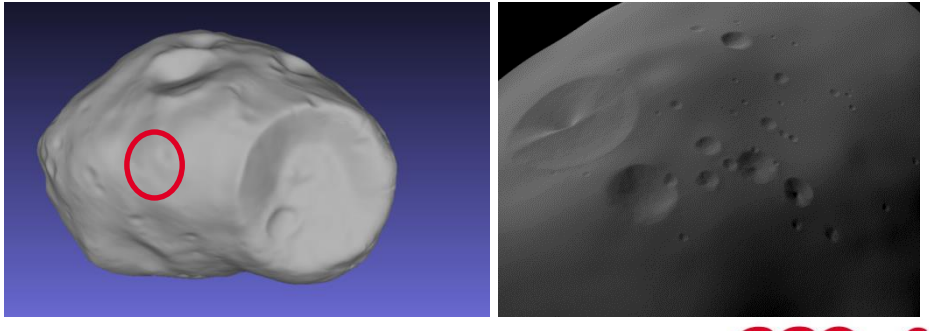


MIL & IMAGES GENERATION

- **Simulink model** Developed within the scope of *GNC for Phootprint Descent and Landing* project.
- New version of PANGU 4 that includes updated model of Phobos. Note that image rendering is very demanding (powerful PC is needed)
- Medium-Fidelity (performance model) vs High fidelity (PANGU + IP implementation in SW)
- Autocodeble models for GNC algorithms (Used in Leon2, updated and verified for Leon4)
- **Simulator is used to obtain the relevant trajectory data, measurements and PANGU images** to verify and validate the implemented IP algorithms.
- Optical facility (ViSOS) will use a database for the trajectory data obtained using the Simulator in the medium/high fidelity, including the set of PANGU generated images of the trajectory.
- In case of ViSOS or platform-ART tests only trajectory and measurements data are used, therefore, no PANGU is required



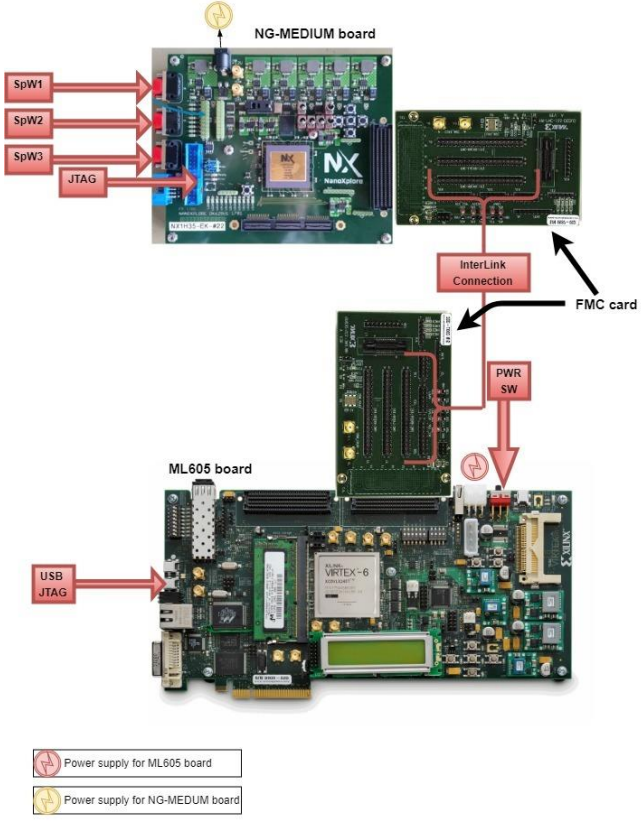
Input model of Phobos with selected landing site area (left); Enhanced DEM with craters rendered by PANGU (right).



IPB BB: INTERMEDIATE STEP

IPB BB includes:

- ❑ NG-Medium DevKit2
- ❑ Xilinx ML605 Board
- ❑ 2 x FMC-XM105
- ❑ Wiring and SpW interfaces
- ❑ GMVScope FPGA debugger



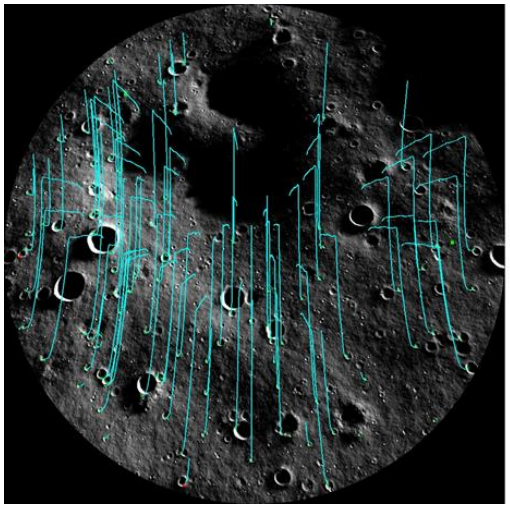
Virtex-6 suitable breadboard demonstrator for Virtex-5:

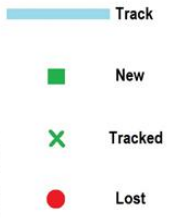
- ❑ Over-constraining the IPB-PRF clock at x1.15
- ❑ USE DPORT set to False for DSP48E1
- ❑ FMC Boards for I/O standard matching
- ❑ Over-constraining external memory (Burst Chop 4 mode)
- ❑ System Monitor (SYSMON)

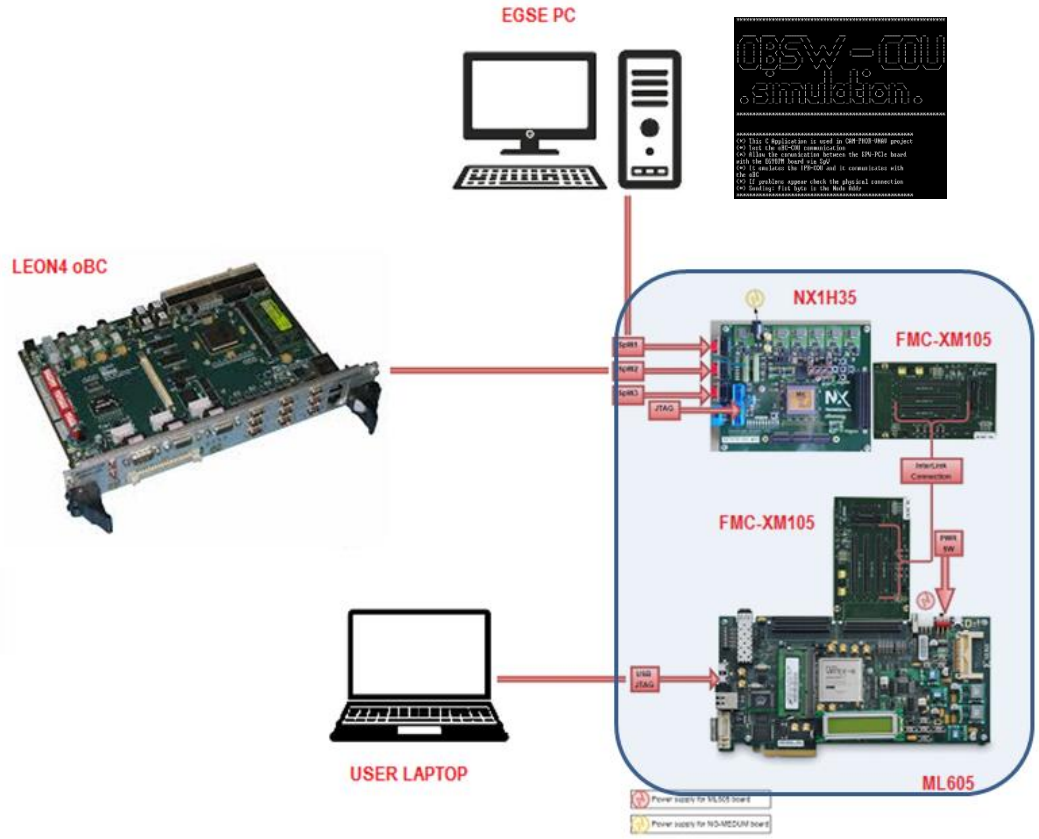
IPB BB VALIDATION

Tests performed:

- ❑ Housekeeping Services Verification
- ❑ Debug (Memory W/R)
- ❑ Full Navigation Verification

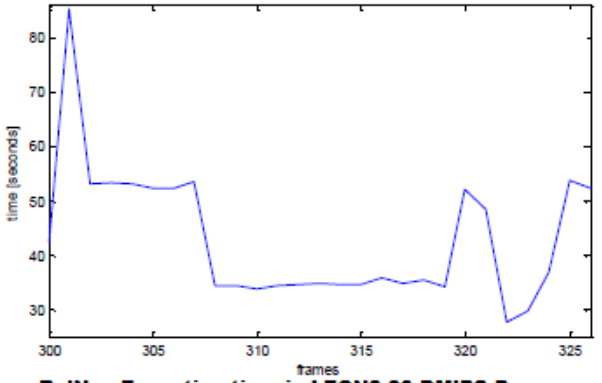




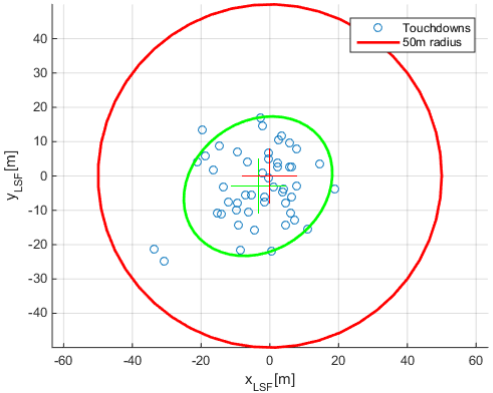


FEATURES & PERFORMANCES

- Landing Accuracy : better than 50 meters
- Pre-Processing functionalities implemented in the Interfaces FPGA
- Feature Tracking Algorithm implemented in the Processing FPGA
- GNC algorithm running in SW in the LEON4 On-Board Computer
- RelNav Processing Time in FPGA : 120 - 150 ms



RelNav Execution time in LEON2 86 DMIPS Processor



GNC	Horizontal Position Error [m]	Horizontal Velocity [cm/s]	Vertical Velocity [m/s]	Final thrust altitude [m]	Attitude error [deg]
Minimum	0.748	0.534	-0.860	46.721	0.141
Maximum	39.891	3.813	-0.785	54.712	0.264
Mean	4.536	1.611	-0.823	51.408	0.214
Std. Dev.	14.830	1.095	0.017	1.627	0.025

COU CHARACTERIZATION

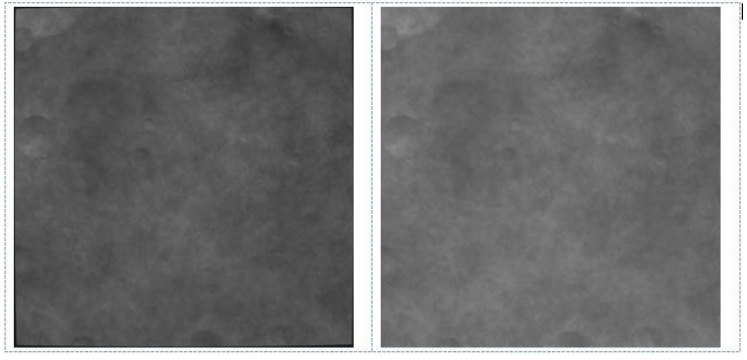


Image Correction & Calibration

- ❑ Bright/Dark Field (Bias/Gain Tables Needed)
- ❑ Bad Pixels (Bad Pixels Map Needed)
- ❑ Lens Distortion (Intrinsic Matrix Needed)

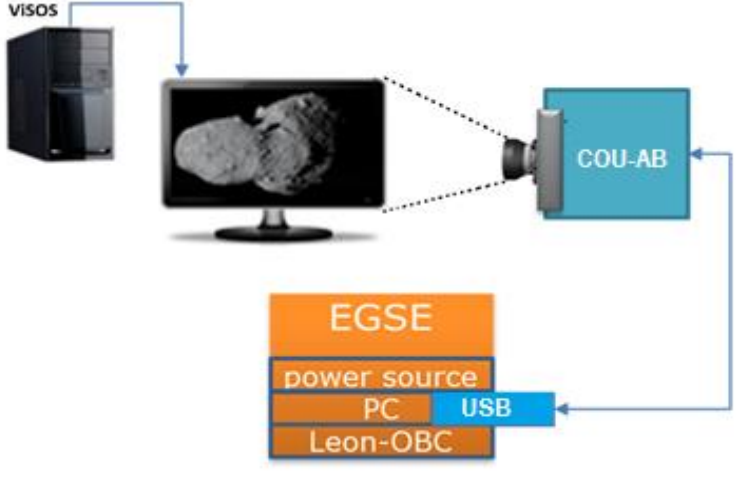


Image Comparison

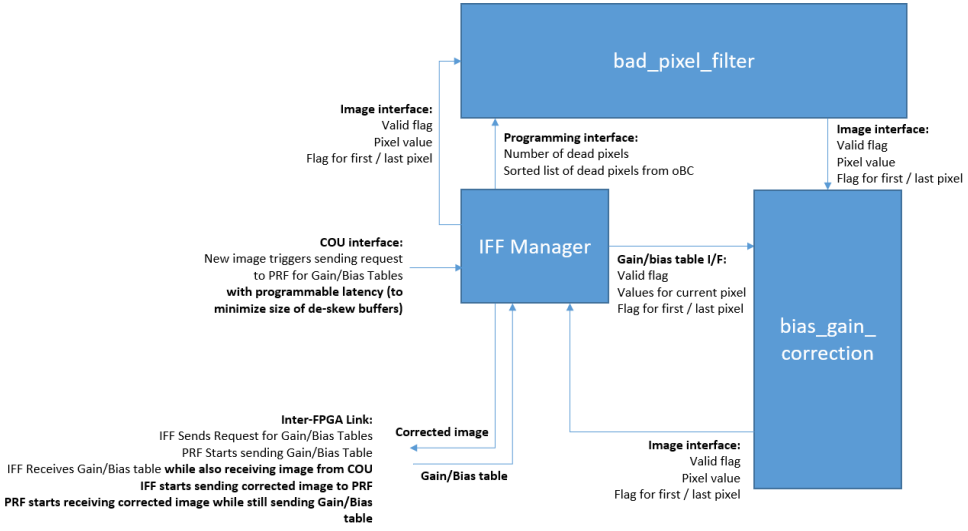
- ❑ Structural Similarity Index Matrix (SSIM)
- ❑ Peak Signal to Noise Ratio (PSNR)
- ❑ Mean Square Error (MSE)

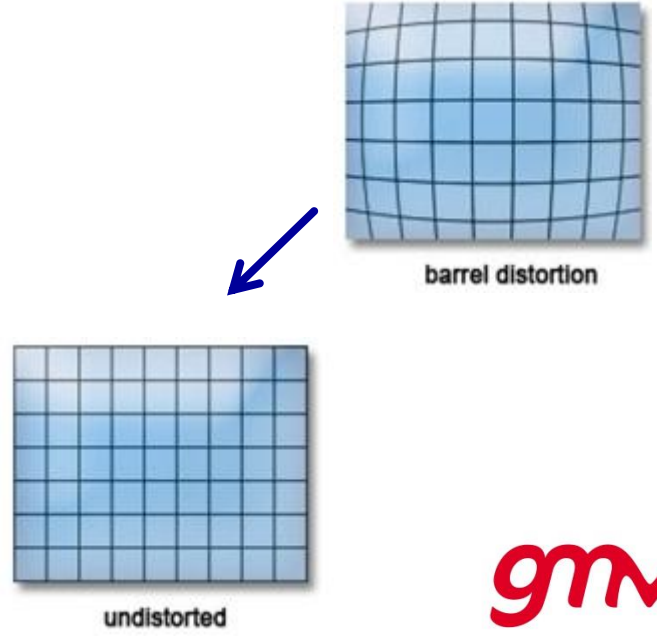
	SSIM [%]	PSNR [dB]	MSE [Pix Value]	Exposure Time [ms]
Limit Values	95.11	34.60	22.52	15

LOW-LEVEL IMAGE PRE-PROCESSING

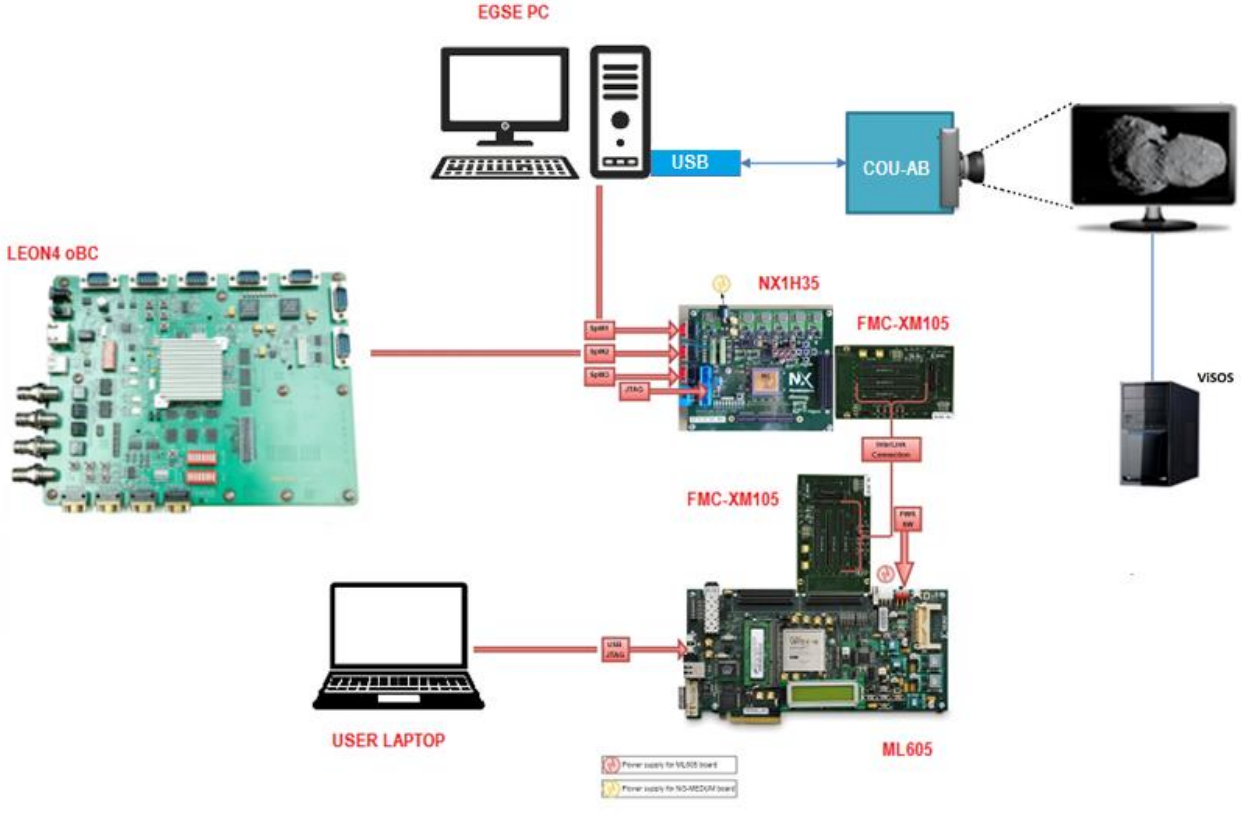
Image Correction & Calibration

- ❑ Bias/Gain Correction – Implemented in NG-Medium before RelNav Processing
- ❑ Bad Pixel Correction – Implemented in NG Medium before RelNav Processing
- ❑ Camera Distortion Correction – Software Implemented in EGSE PC

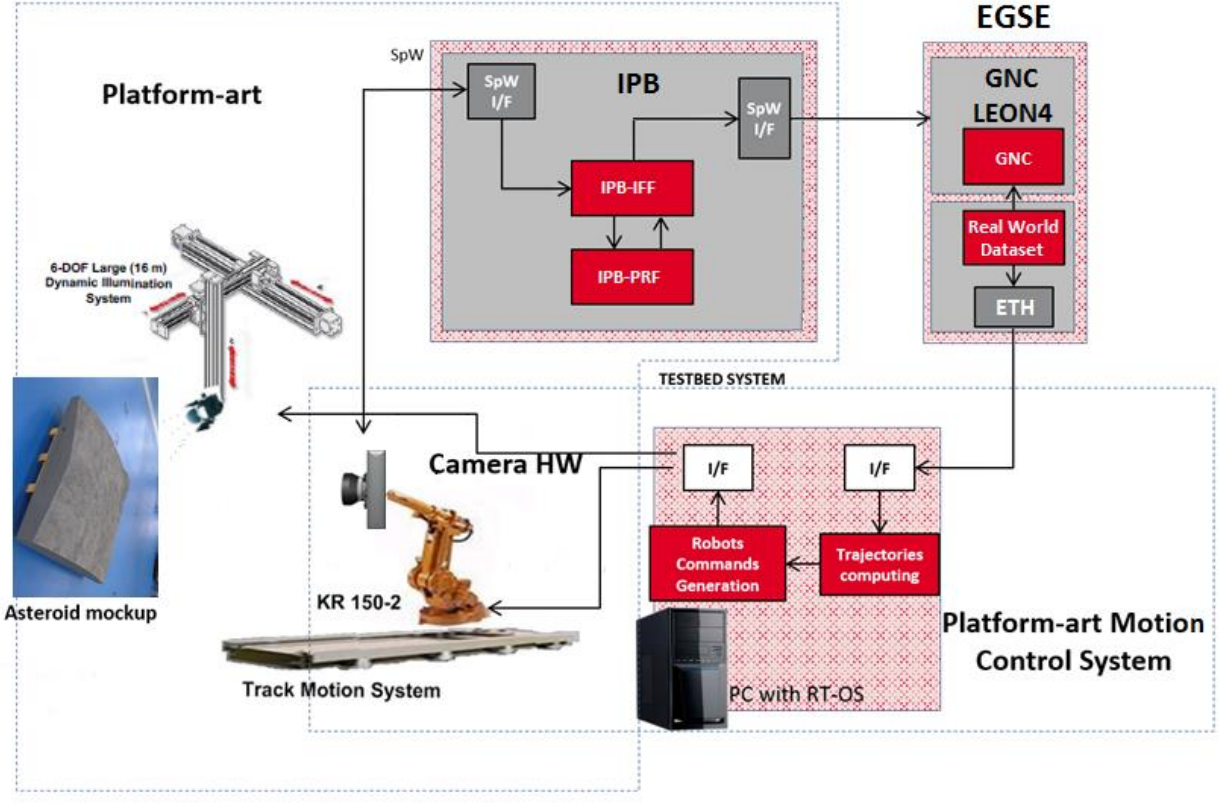




OPTICAL FACILITY VALIDATION



platform-art© VALIDATION



- GMV Dynamic Testbed
  - 2 x KUKA Robotic arms
  - Dynamic Illumination System
  - Phobian surface
  - EGSE
  - IPB+COU
- Real air-to-air metrology stimulation
- Raising TRL to 5/6
- FARO Laser Tracker Calibration

CONCLUSIONS

- 2 space-graded FPGAs architecture for Image Processing Board, validated by means of breadboard integration with 2 commercial FPGA development kits.
- Image Pre-Processing functionality tested and validated using BRAVE FPGA.
- Capability of NG-Medium to deal with multiple high data-rate interfaces was demonstrated (spacewire routing of up to 4 links with redundandcy scheme).
- Reliable and accurate navigation solution achieved through complex image processing and through distributed on-board highly computationally capable chain (NG-Medium, Virtex-5(6), LEON4).
- Real-Time performance achieved by means of HW acceleration of the Feature Tracking algorithm (Feature tracking algorithm accelerated from average 43 seconds in LEON2 to average 130 milliseconds in FPGA).

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THANK YOU

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