OBDP 2019

Next Generation Data Handling System – OBC-SA / SPINAS (On-Board Computer – System Architecture / SPace INfrasructure And Software)

DEFENCE AND SPACE

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AIRBUS

Objectives

S

Next Generation Data Handling System

- Flexible HW architecture
- Flexible SW architecture
- Deterministic high speed and secure bus system for exchanging data

→ obvious: this is not only related to solely HW or SW. Its both – and more →architecture necessary to focus on the end-to-end chain during the development

→ How do we want to achieve this?

Objectives II

Three ingredients

1. Flexible HW architecture

→ Integrated Modular Architecture (IMA) →HW (and SW)
→ IMA used in several and Airbus and Boeing Aircraft Families – widely adopted, makes it more robust, reduces complexity and harness
→ Not single board but “platform” is needed

2. Flexible SW architecture

→ No monolithic SW package
→ Time-Space Partitioning
→ Reusable SW Framework – core Flight System (cFS)

3. Deterministic high speed and secure bus system for exchanging data

→ Deterministic Bus System (TT-Ethernet)

IMA – HW SPINAS OBC/SA

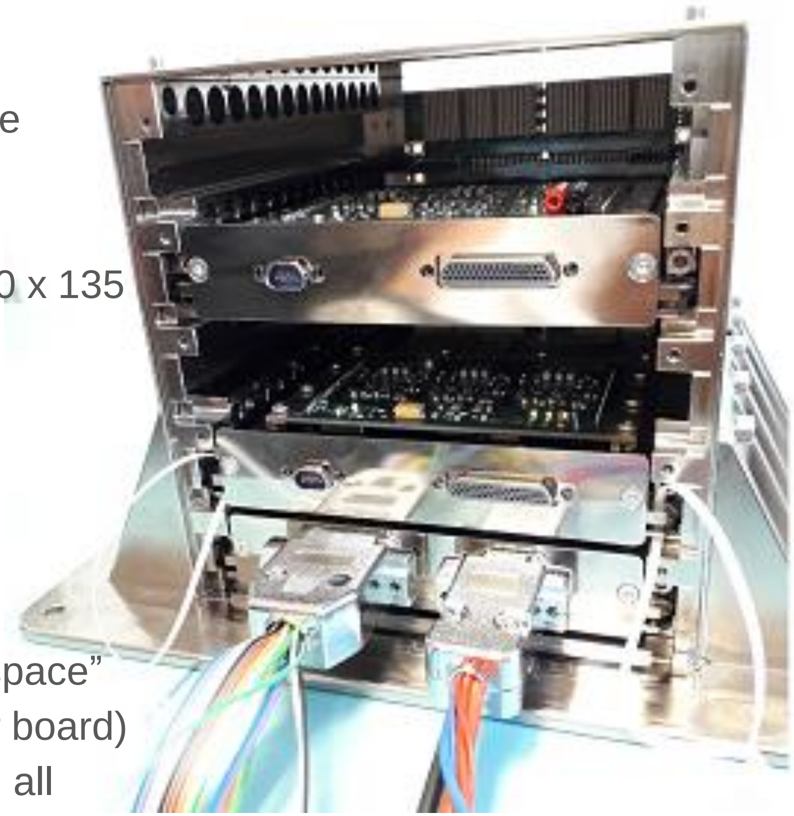
SPINAS – Space Infrastructure and Software
OBC/SA - On-Board Computer – System Architecture

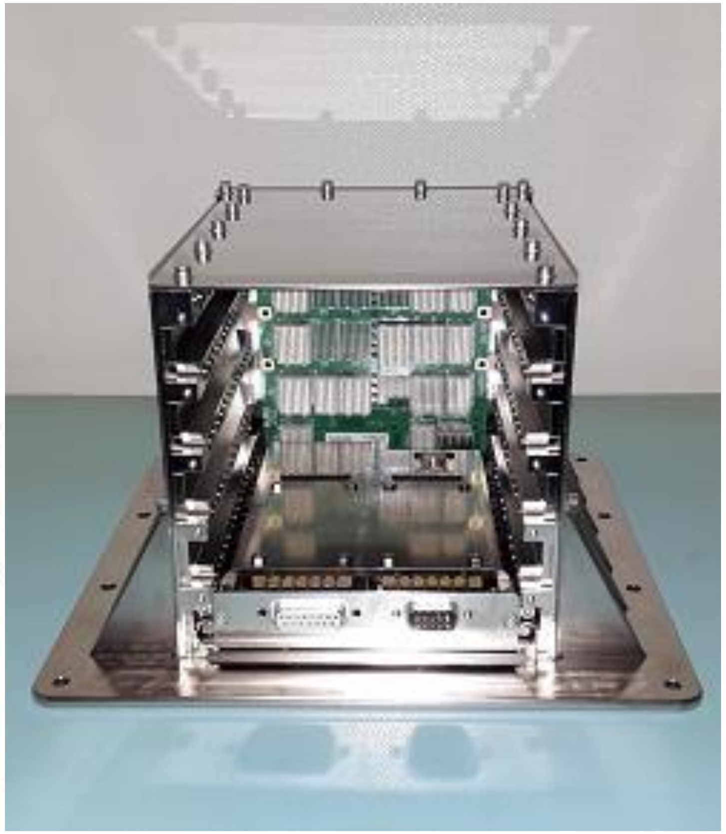
3U Compact size / small footprint
Mass < 5kg, Dimensions (L x B x H) [mm]: 230 x 230 x 135

Consists of:
- Computer Board – LEON4 – GR740
- IO Board - TTEthernet
- Power

Connected by standardized backplane “cPCI serial space”
→boards are exchangeable, e.g. if DAHLIA (or other board) comes to market, CPU board can be exchanged and all other components remain

Status: TRL6 is expected for March 2019
Most of EQM Tests executed in Q4 2018





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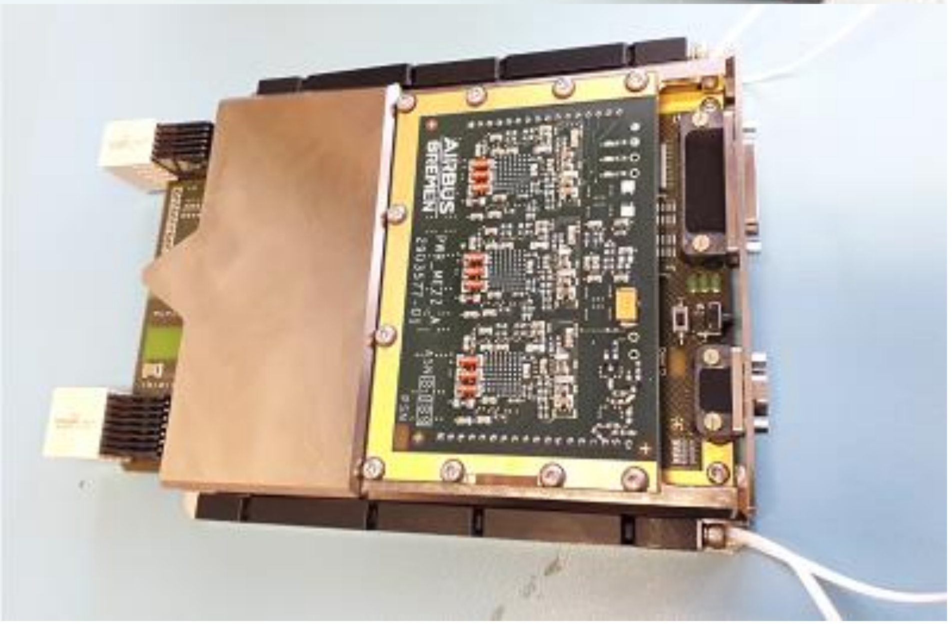
IMA – HW SPINAS OBC/SA II



CPU Board

- High reliability SPARC V8 CPU – LEON4
- 4 cores @ 250 MHz
- 459 DMIPS per core
- 256 MiB SDRAM (+EDAC)
- 4 Partition with 64MiB NOR-Flash
- 2x Gigabit Ethernet
- 8x Spacewire up to 300Mbit/s
- Redundant MIL-STD-1553B
- 2x CAN, 2x RS422

IO Board

- Xilinx Virtex 5 FPGA
- 3x Gbit TTEthernet / Ethernet
- 1x Ethernet
- 2x SpaceWire
- 1x RS422
- 1x SPI

IMA – SW

Goals which needs to be achieved

No monolithic SW package

Integration needs to be made easy

Easier to maintain

Easier configuration management

Many different vendors / “App Store Concept”

Ease testing – simulated and original equipment at the same time / exchange whenever necessary

(Part of the) Solution

Multicore, Time Space Partitioning

Open Architecture

Building Blocks

At the end

→ Many applications on one computer

→ Many different criticalities on computer

IMA – SW – Operating System

Necessity

- Each application must not interfere another application
- OS is either certified or certifiable.

→Operating System is needed which, together with the features of the processor, ensures this goal.

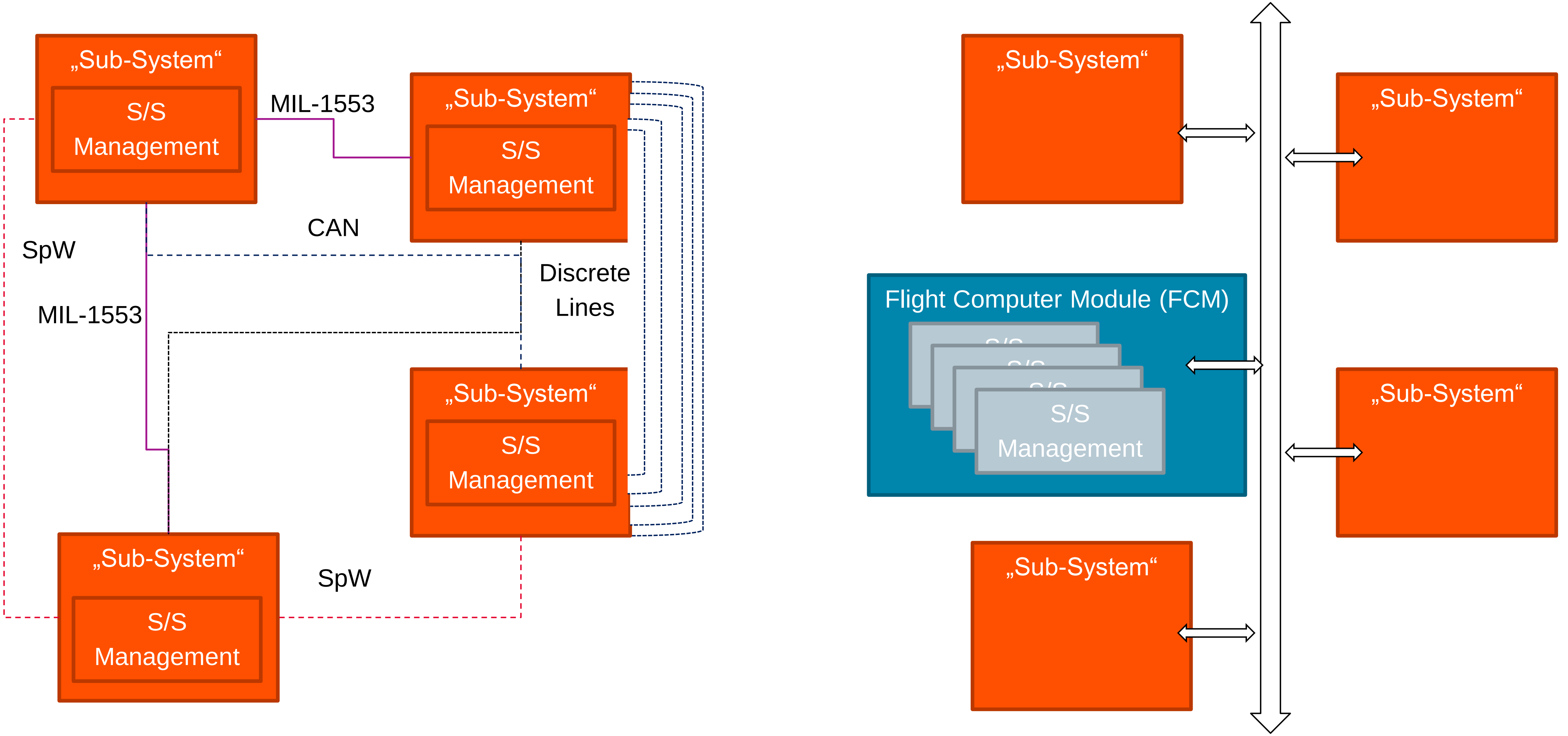
OS

- PikeOS 4.x
- VxWorks 7
- (RTEMS 5.x)

Candidates / next steps

- VxWorks 653
- XtratuM

“Boxes” ./. “IMA”



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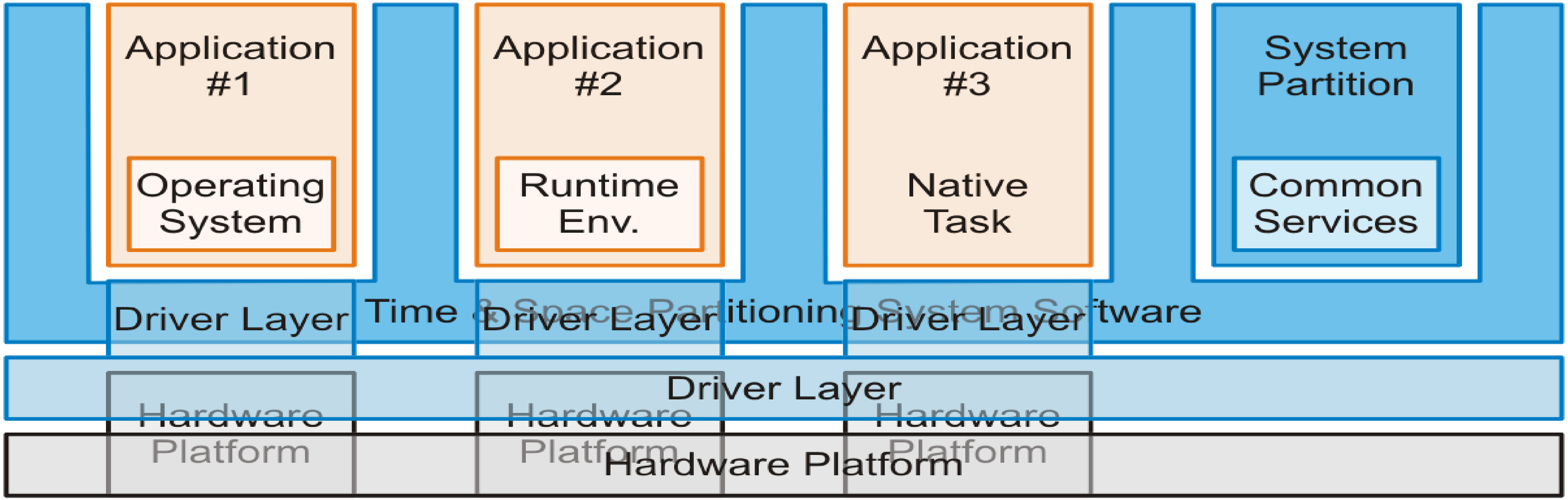
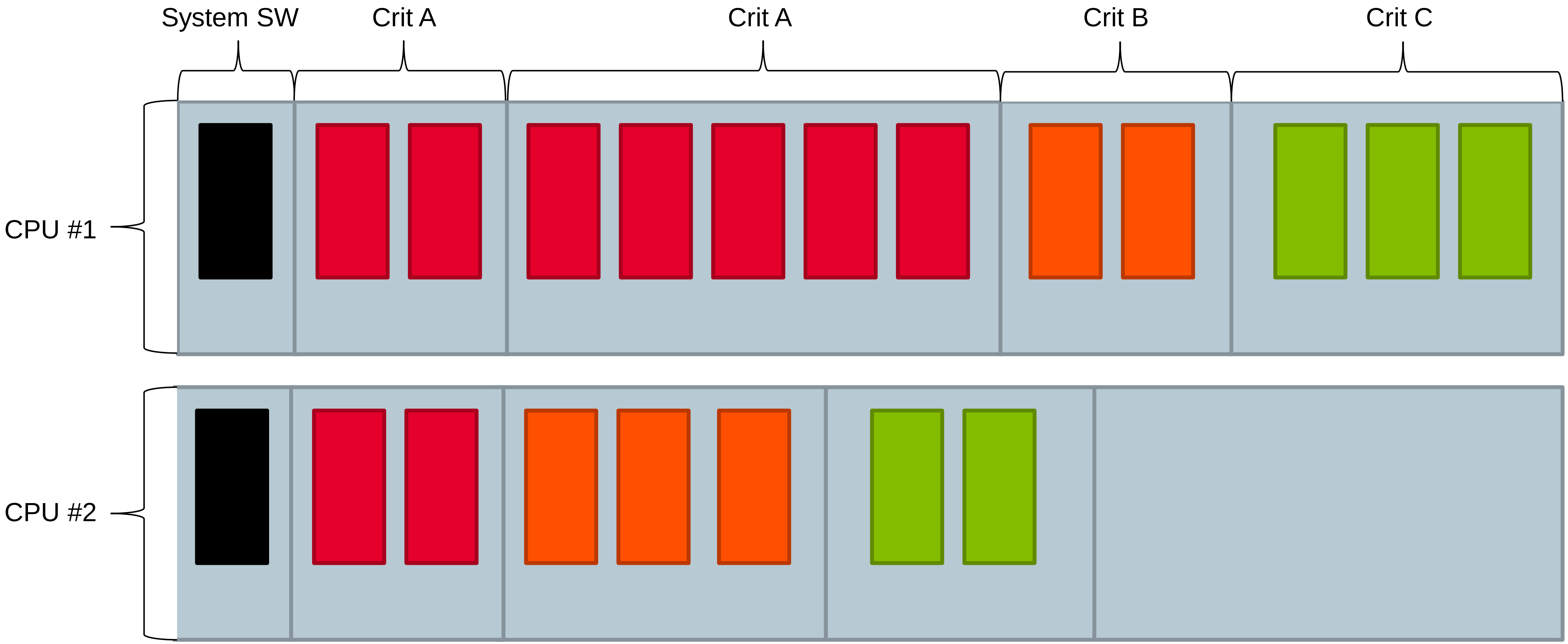
IMA – SW – Time Space Partitioning



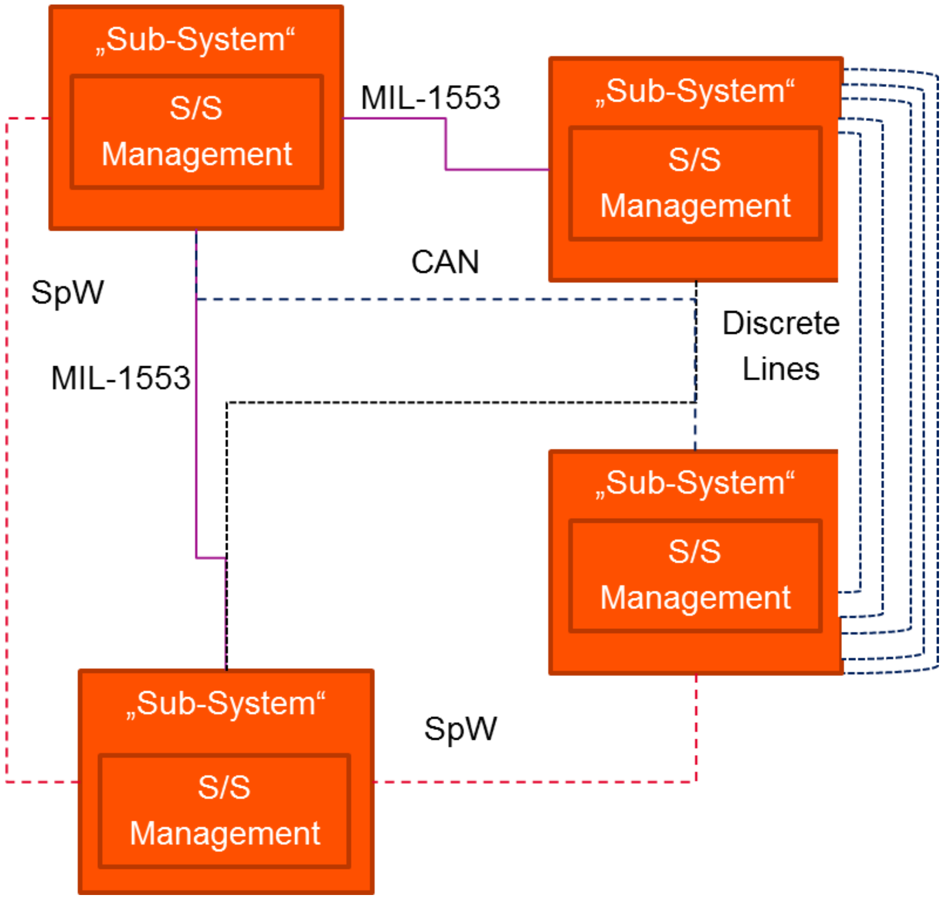
IMA – SW – Time Space Partitioning II



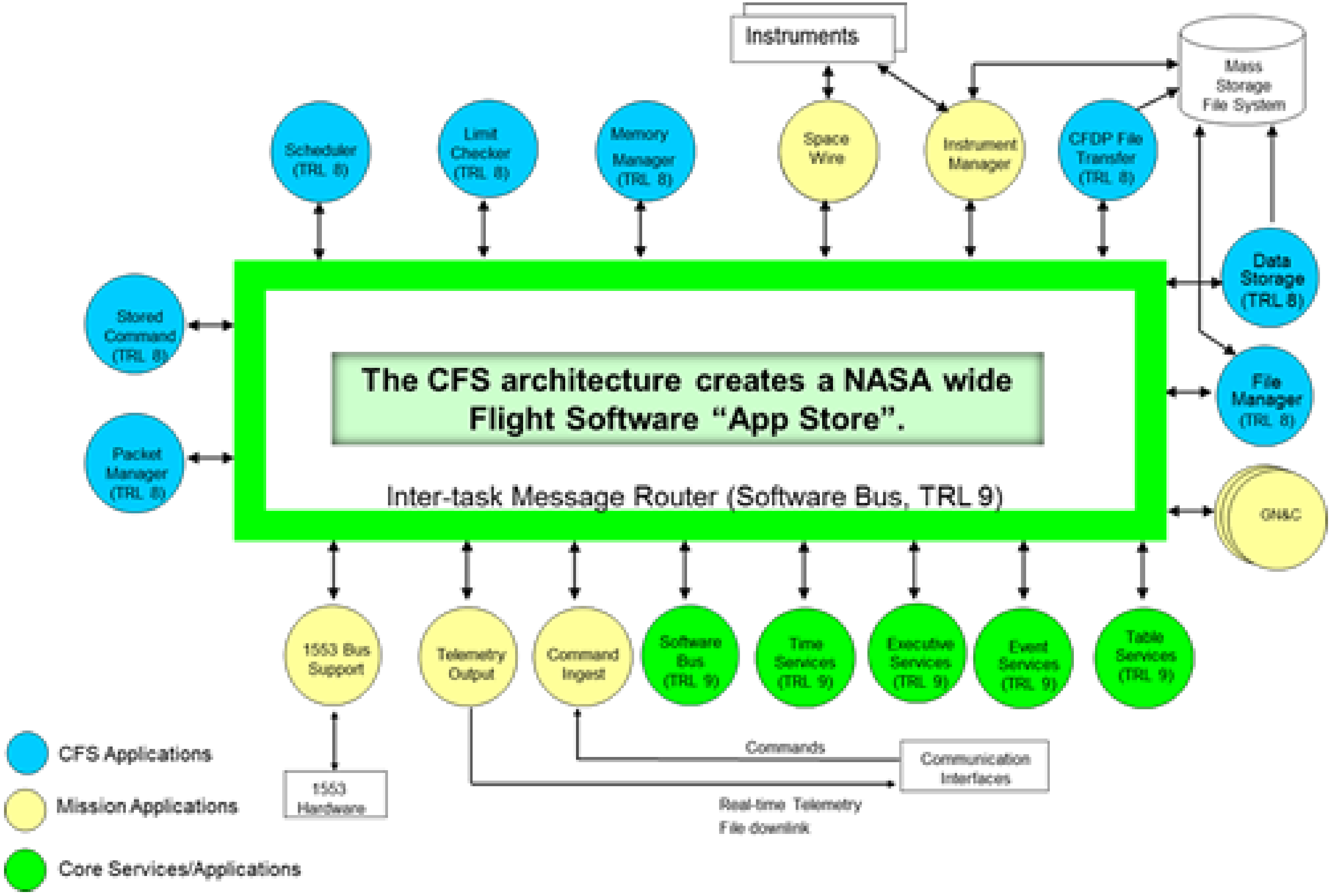
IMA

What is not IMA?

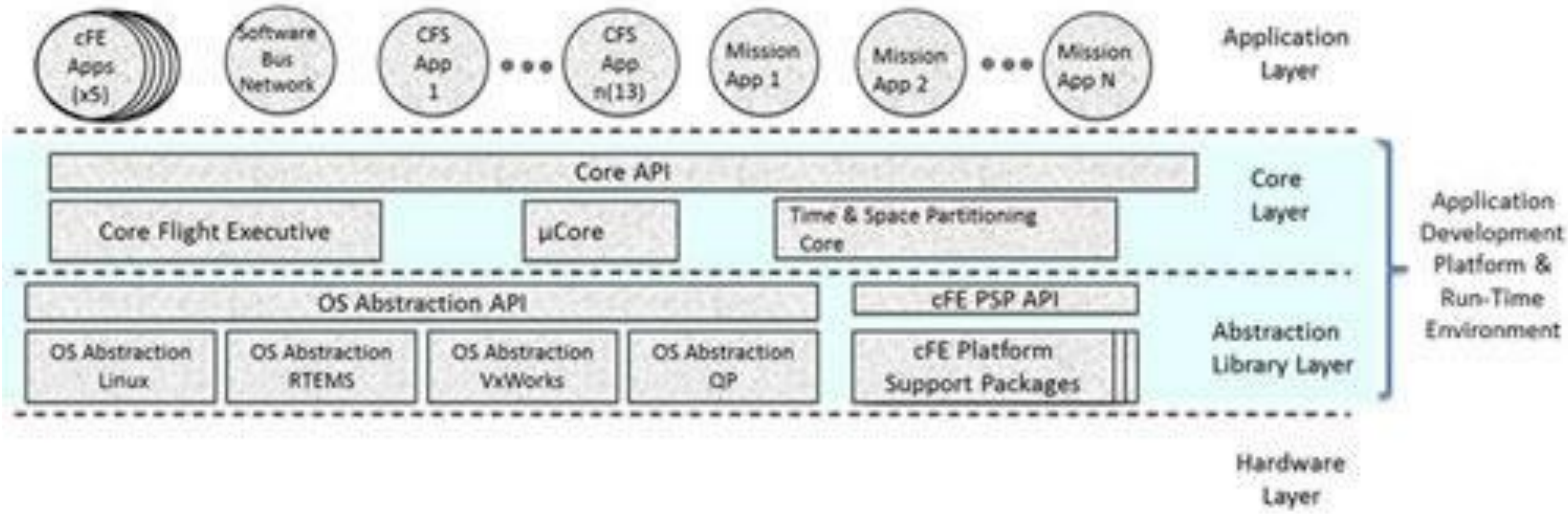
- Take some existing boards and place them into one housing
- Create some kind of connectivity between these boards
- Run existing SW on boards which do not have a common architecture
- Bridge existing SW components via proprietary connections – which cannot be reused later on



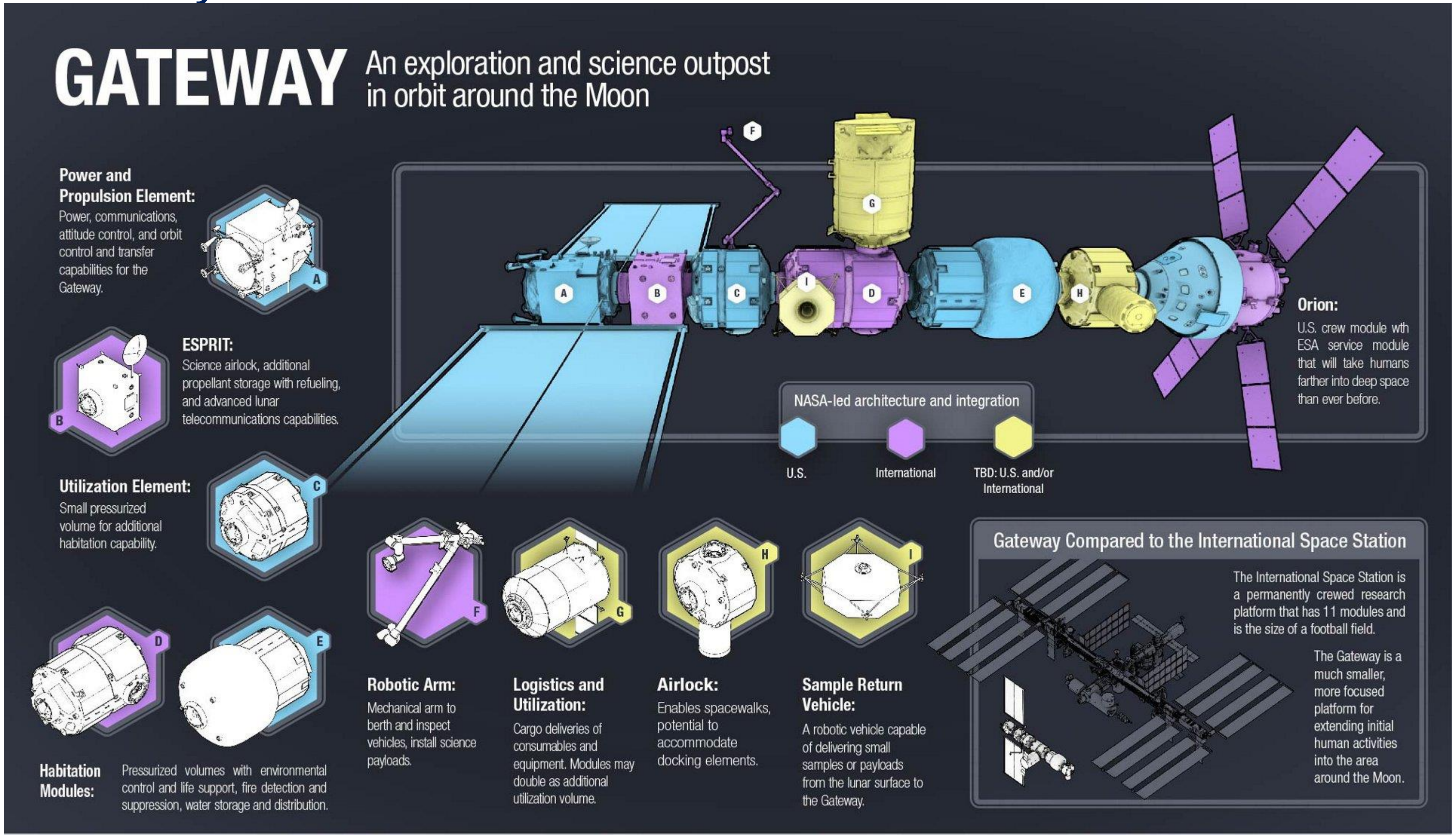
Reusable SW Framework – core Flight System



Reusable SW Framework – core Flight System II



Study – Gateway



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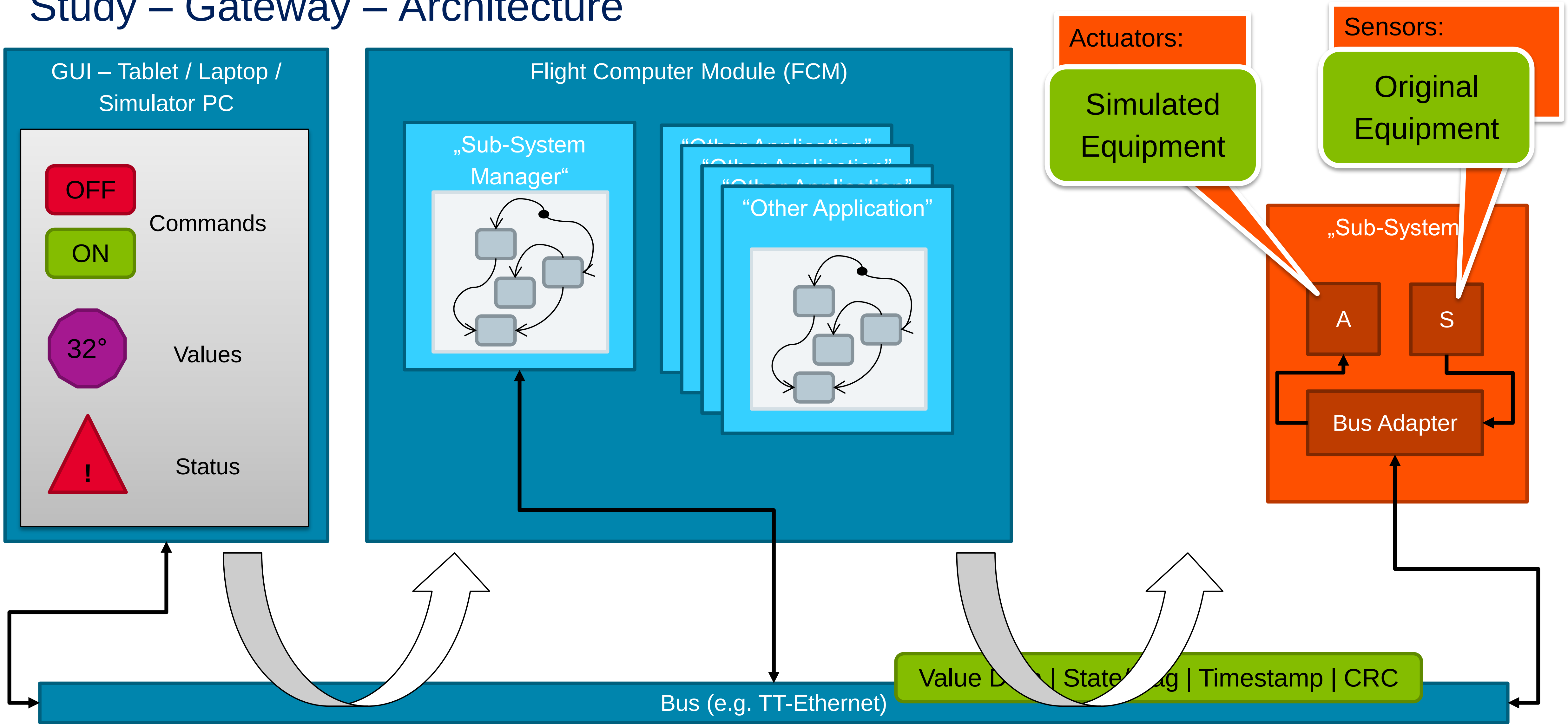
Study – Gateway – Objectives Breadboard Development

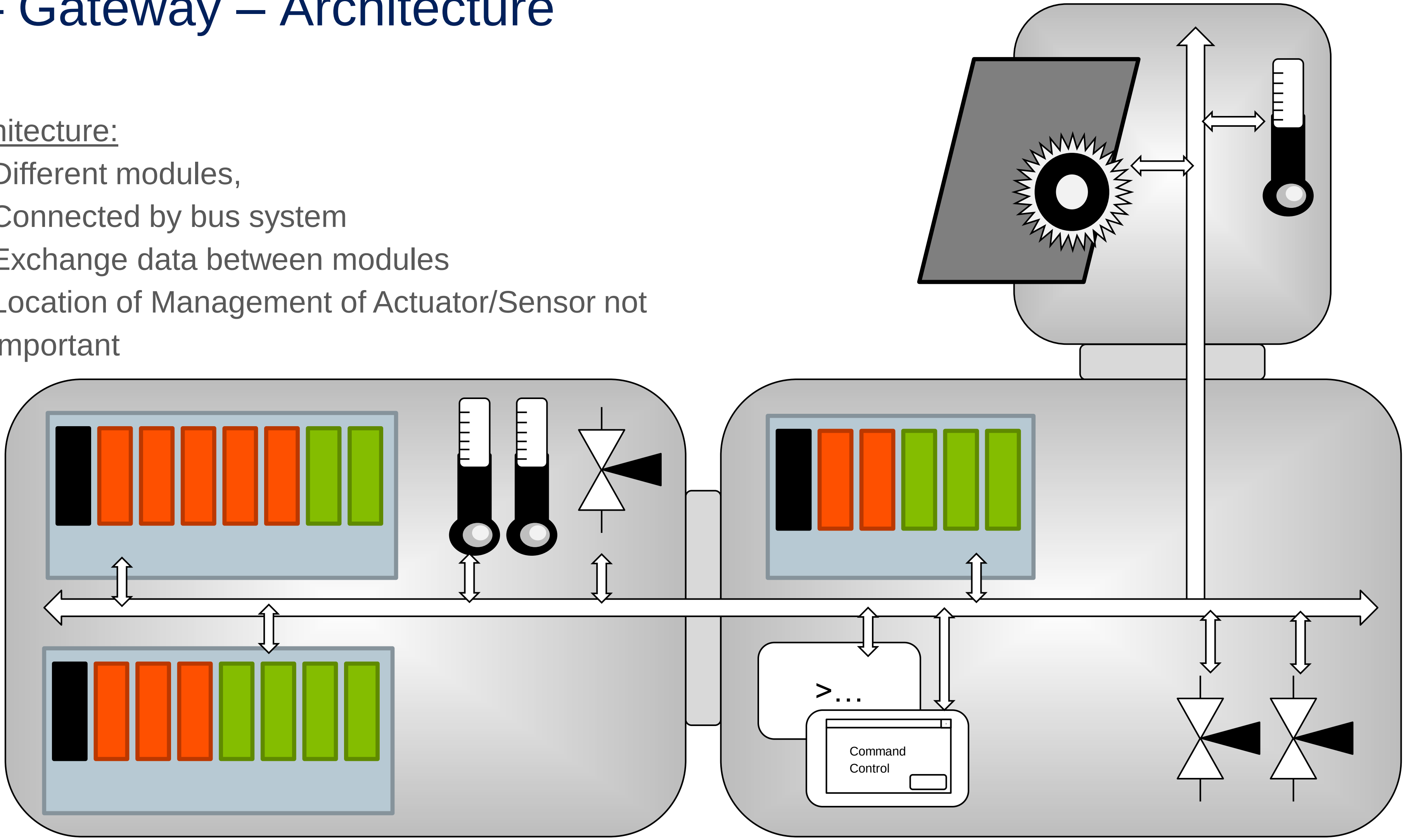
Based on IMA, Spinas, cFS and TT-Ethernet

Scenario 1: Apps running on different partitions
Scenario 2: Apps running on different nodes
Scenario 3: Load, Start, Stop, Unload cFS Apps in run-time in an FDIR scenario
Scenario 4: Shift functionality from one node to another
Scenario 5: Resume failed App on node via other App or from Ground

Study – Gateway – Architecture



Study – Gateway – Architecture



Architecture:

- Different modules,
- Connected by bus system
- Exchange data between modules
- Location of Management of Actuator/Sensor not important

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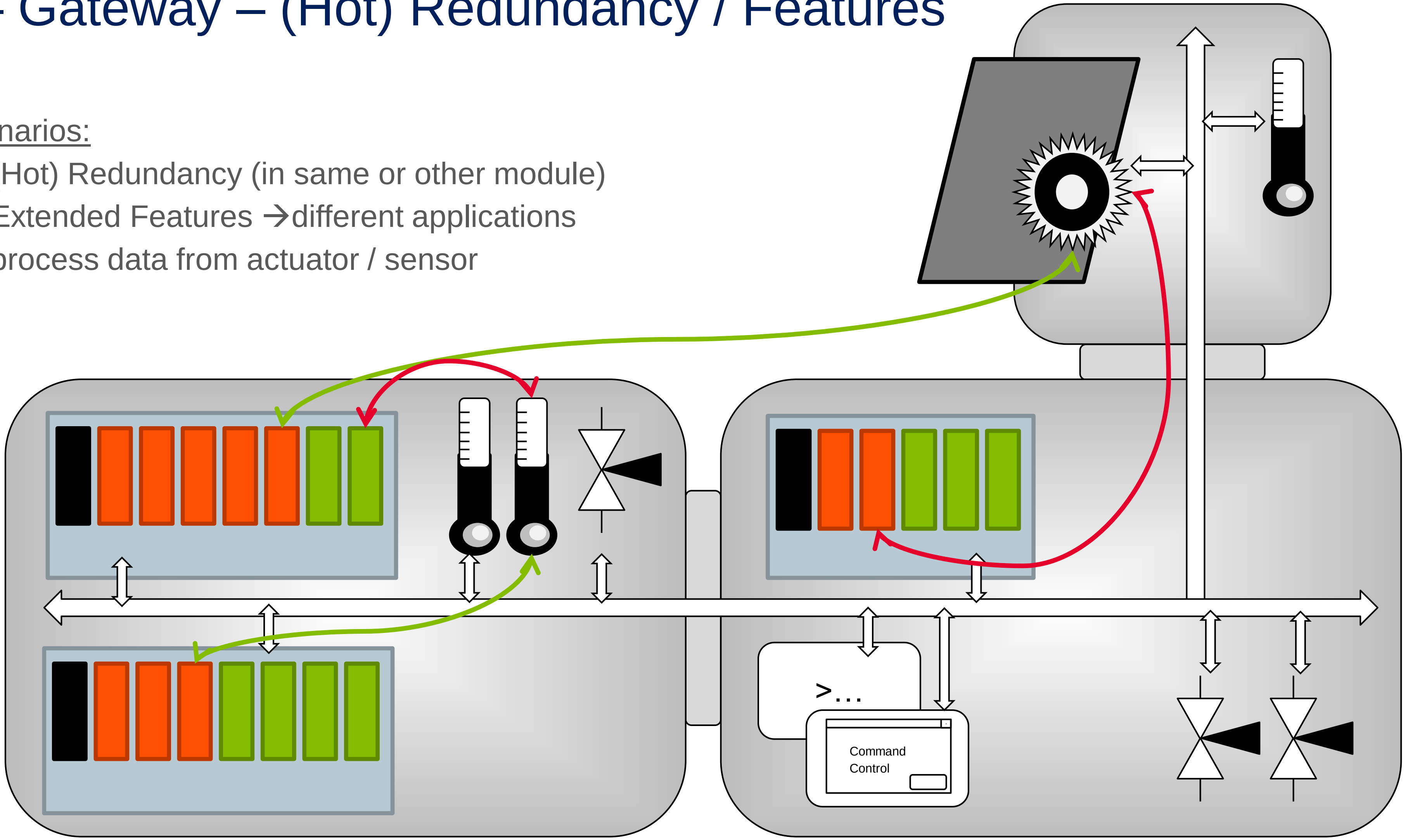
Study – Gateway – (Hot) Redundancy / Features

Scenarios:

- (Hot) Redundancy (in same or other module)
- Extended Features →different applications process data from actuator / sensor



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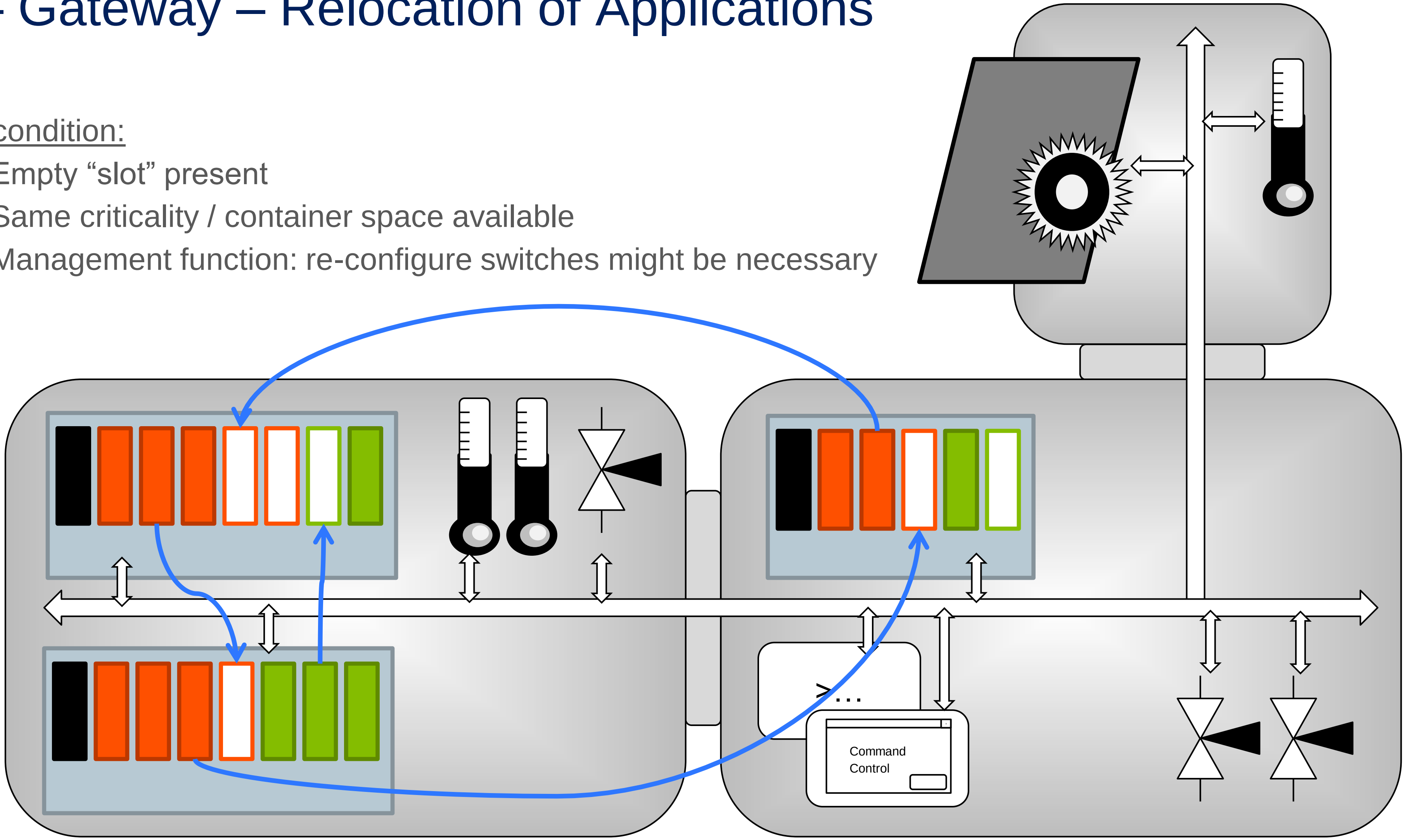
Study – Gateway – Relocation of Applications

Precondition:

- Empty "slot" present
- Same criticality / container space available
- Management function: re-configure switches might be necessary



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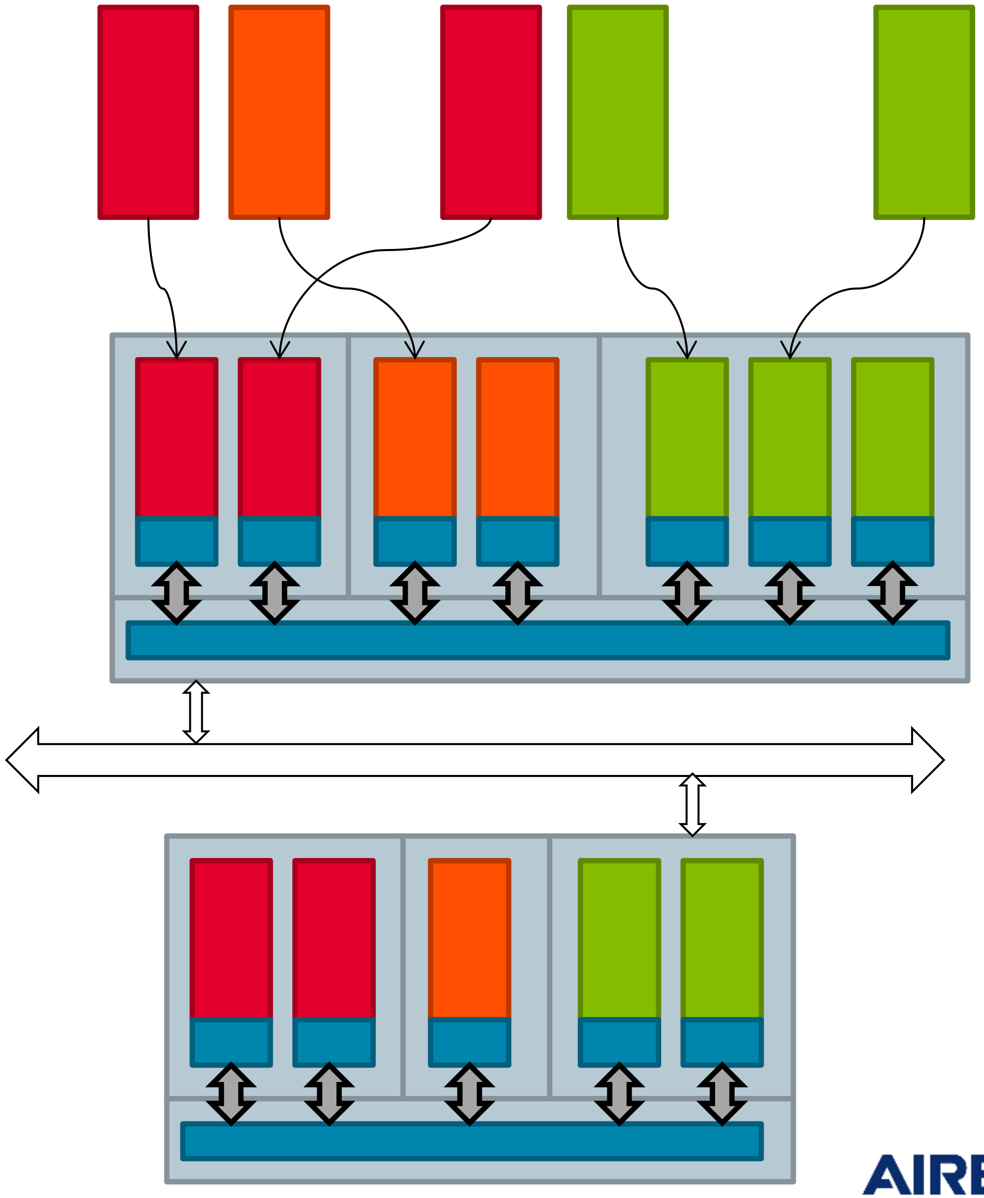
Conclusion

Be able to create applications in a distributed environment
(e.g. supplier, not everything in-house, SW development across sites, …)

Secure each part of the SW
Run SW with same criticality in one or more than one container
Run SW with different criticality in different containers

Run SW on different platforms
Be able to exchange processor board with next generation processor board

Use deterministic bus system
Ensure deterministic communication by using a high reliable, high performance and also secure network



Thank you!