NX RHBD FPGA solutions for OBDP applications

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Agenda

1- Company Overview

2- NX RHBD FPGA devices

3- Embedded Processing

4- Digital Signal Processing

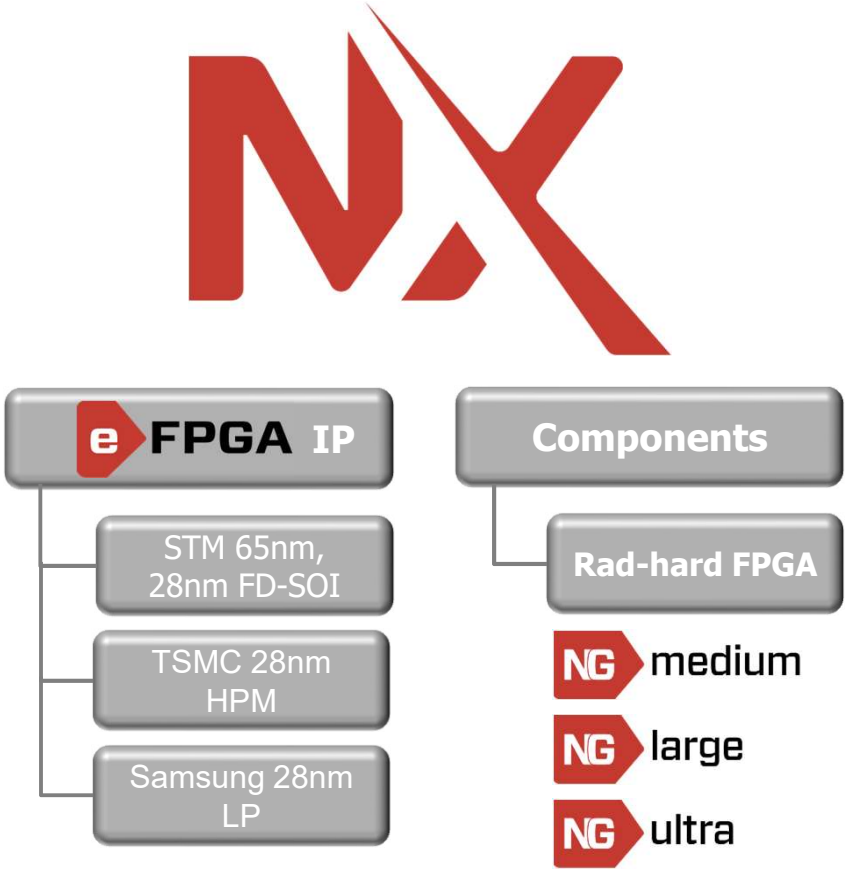
5- High Speed Serial Links

6- CONCLUSION

Questions & Answers

NanoXplore

NanoXplore Overview



- **Created in 2010** by three veterans of semiconductor industry with long experience in the design, test and debugging of FPGA cores.
- **Fabless** semiconductor company headquarter in France
- R&D engineers in two offices in France:
  - Sèvres: Hardware developments
  - Montpellier: Software developments
- **NanoXplore is a leader in the design of large scale programmable logic arrays for state of the art FPGA cores**
- The company is focusing on 2 main activities:
  - Offer hard block embedded FPGA core IP (NX-eFPGA)
  - Developing rad-hard FPGA qualified for space applications (from BRAVE contract)

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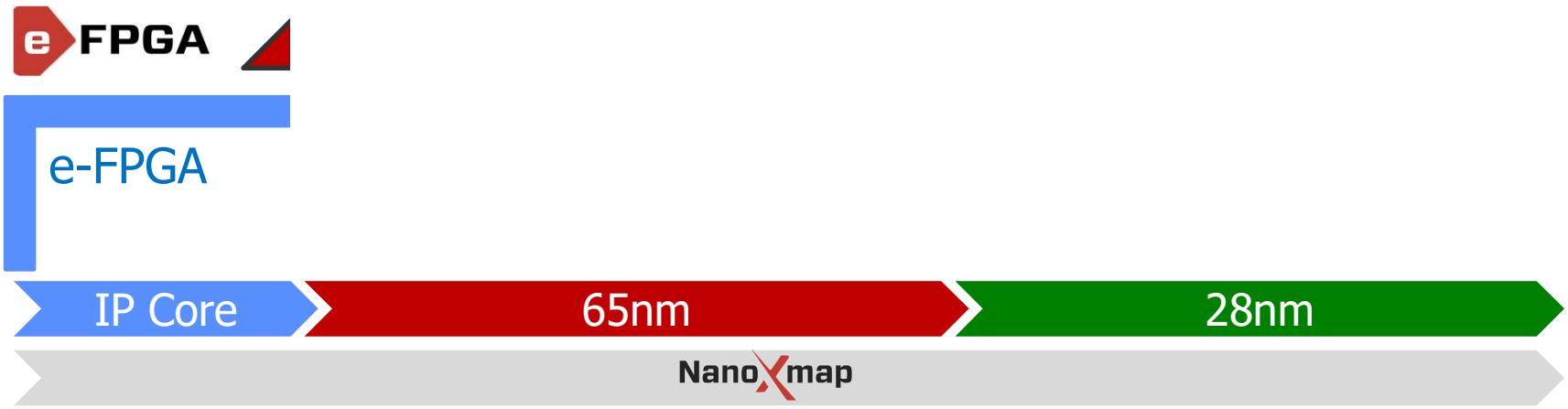
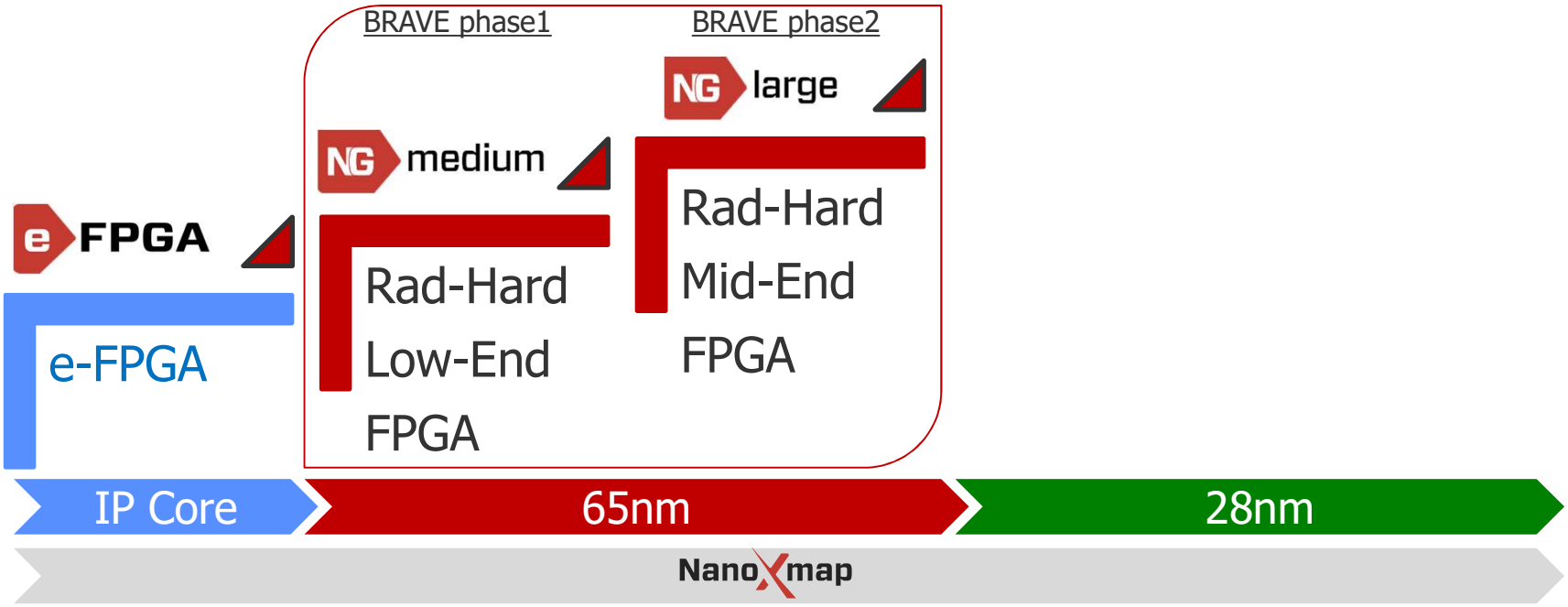
From eFPGA to BRAVE & beyond

- Phase 1: Embedded FPGA cores



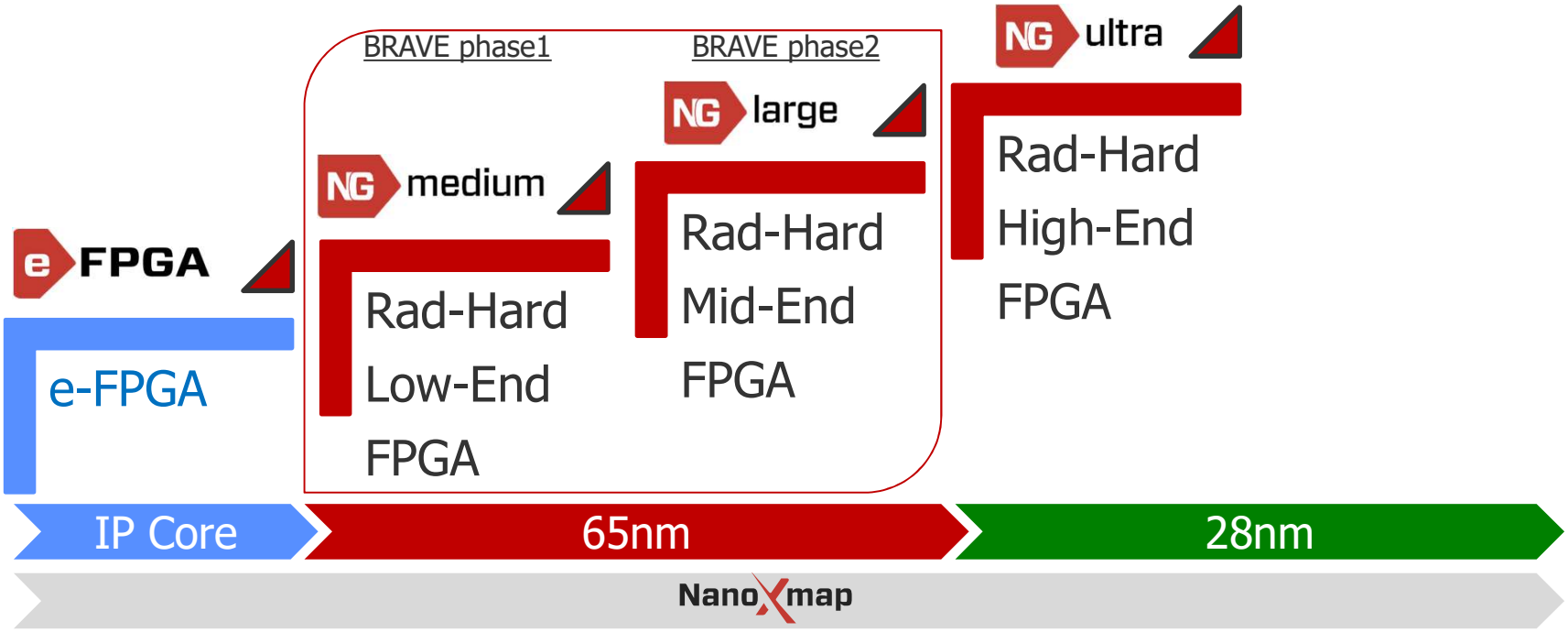
From eFPGA to BRAVE & beyond

- Phase 1: Embedded FPGA cores
- Phase 2: 65nm RHBD FPGA devices development



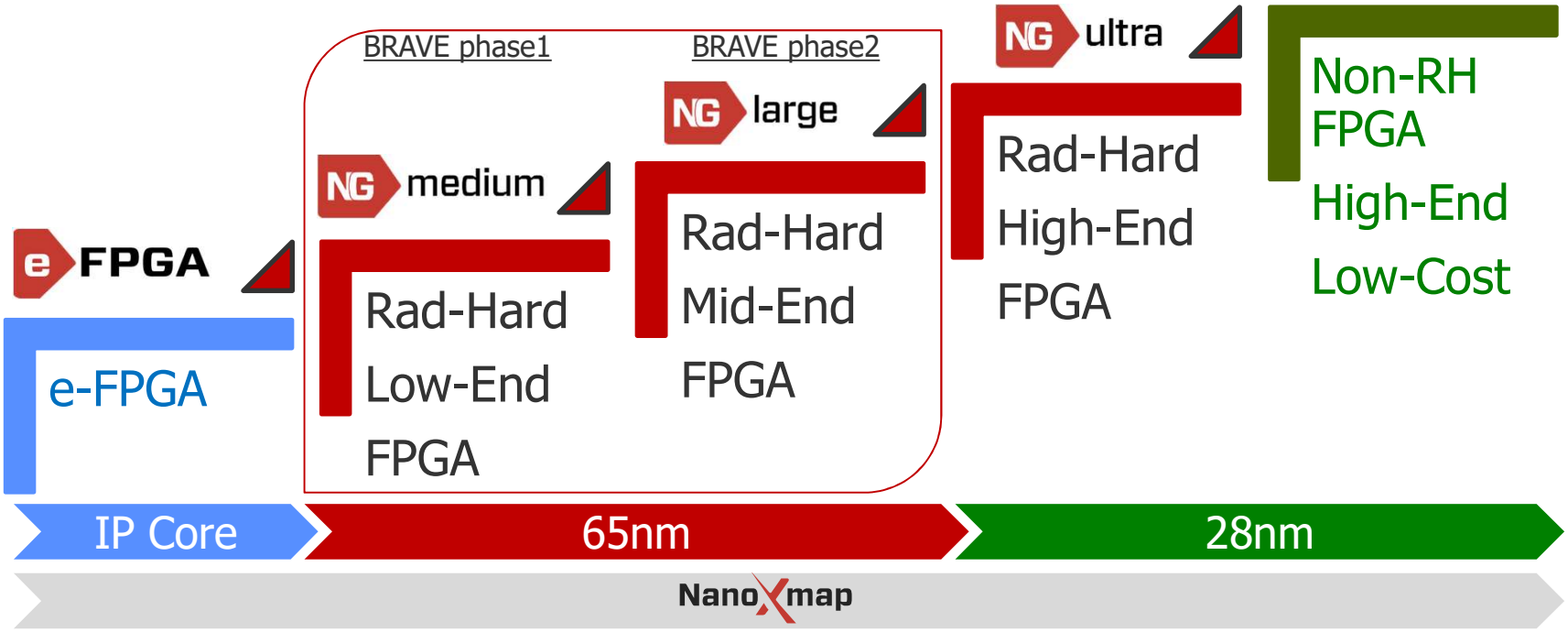
From eFPGA to BRAVE & beyond

- Phase 1: Embedded FPGA cores
- Phase 2: 65nm RHBD FPGA devices development
- Phase 3: Switch to 28nm FD-SOI

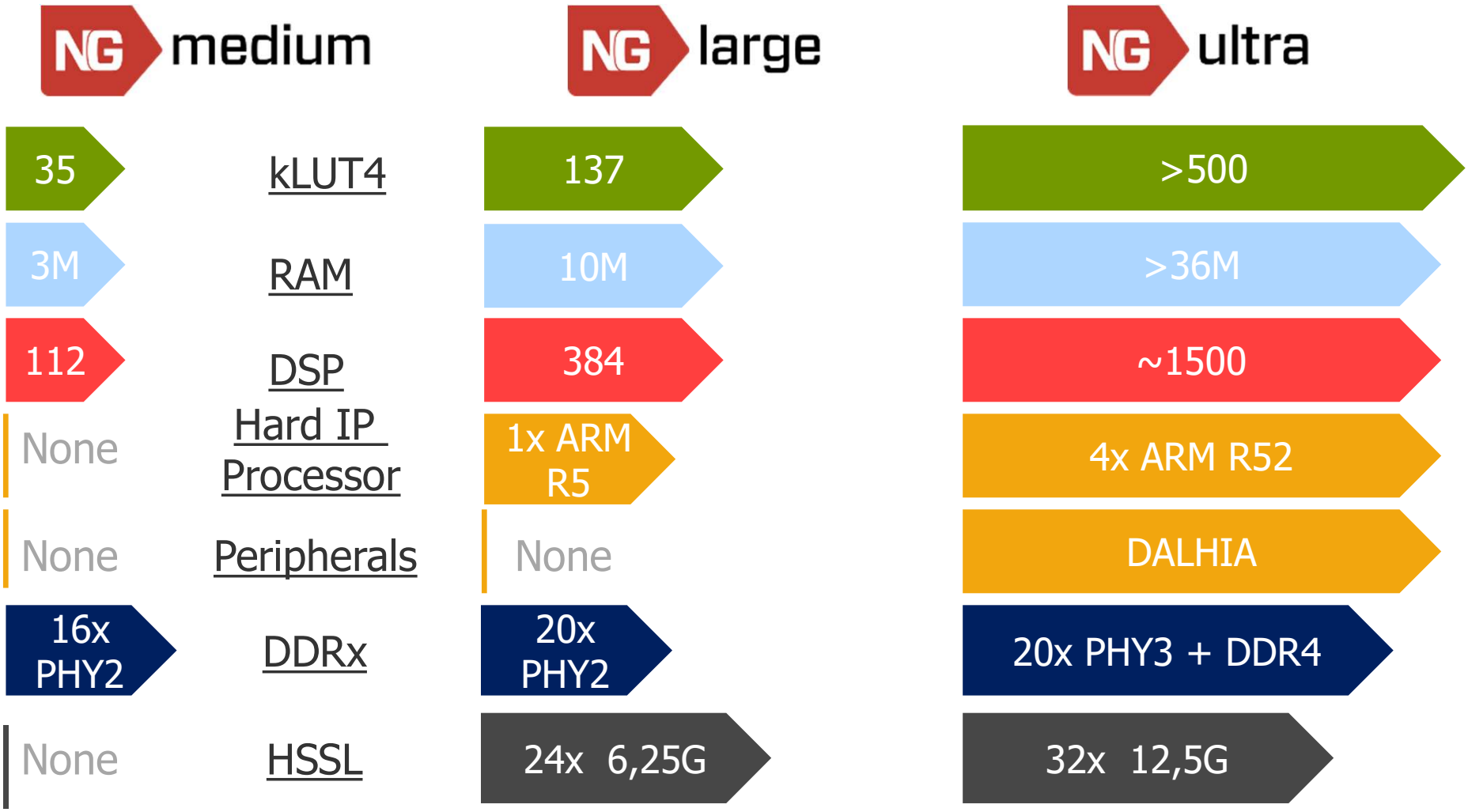


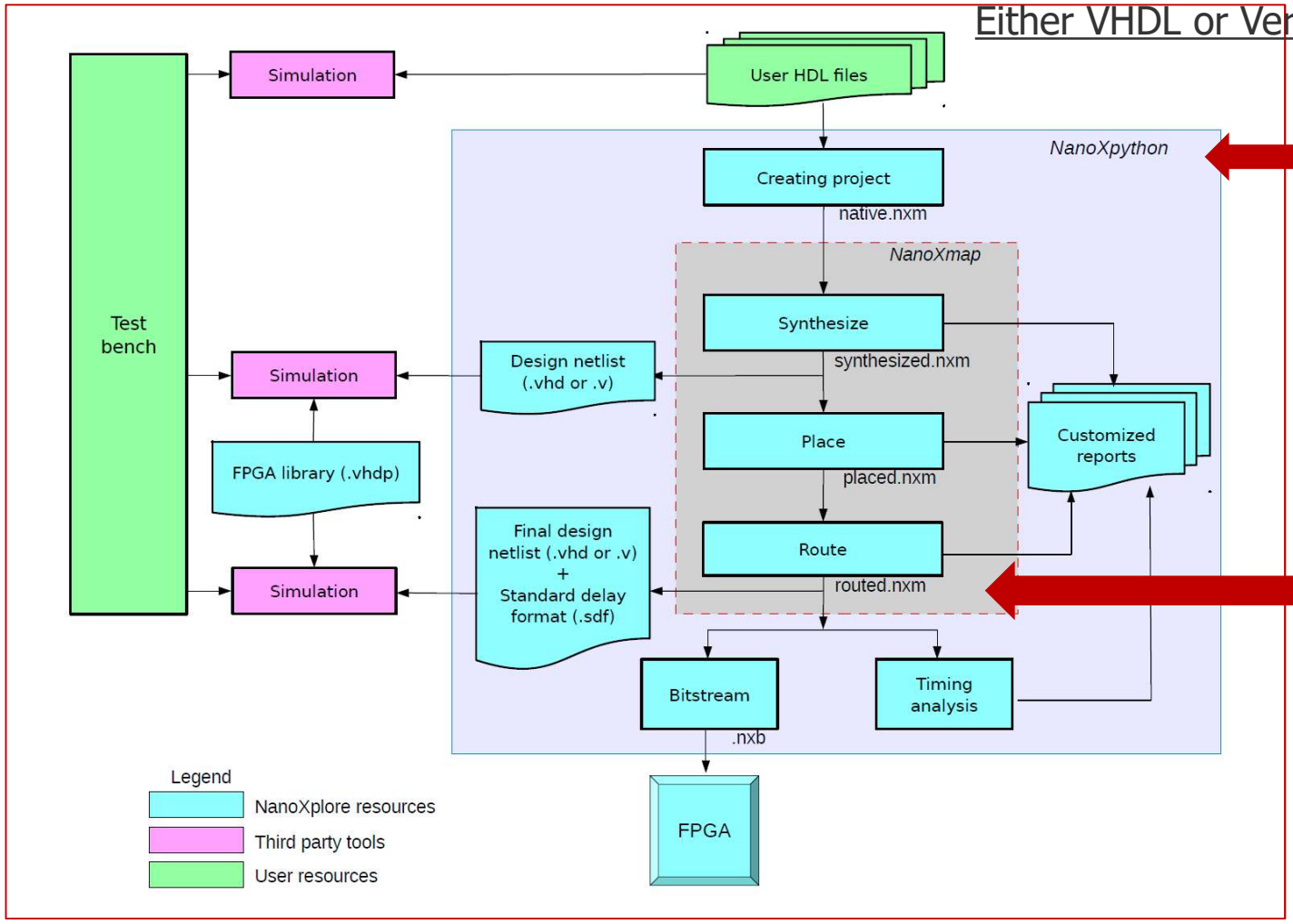
From eFPGA to BRAVE & beyond

- Phase 1: Embedded FPGA cores
- Phase 2: 65nm RHBD FPGA devices development
- Phase 3: Switch to 28nm FD-SOI
- Phase 4: Penetration of additional Niche markets with non-RH devices



RHBD FPGAs features





NXpython is a wrapper around Python executable that allows the user to control Nxmap software.
It fully supports Python sunthax, structures and external modules.

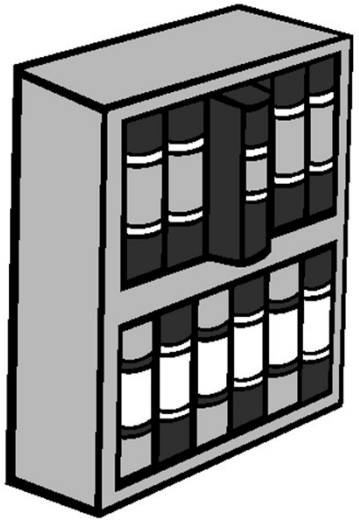
NXmap runs on 64bits Linux workstation runing on on following distributions

- RedHat enterprise Linux v6 or 7
- Ubuntu 14.04 LTS or 16.04 LTS

VM avaiable on Windows

NXcore

NXcore is NanoXplore IP core generation tool



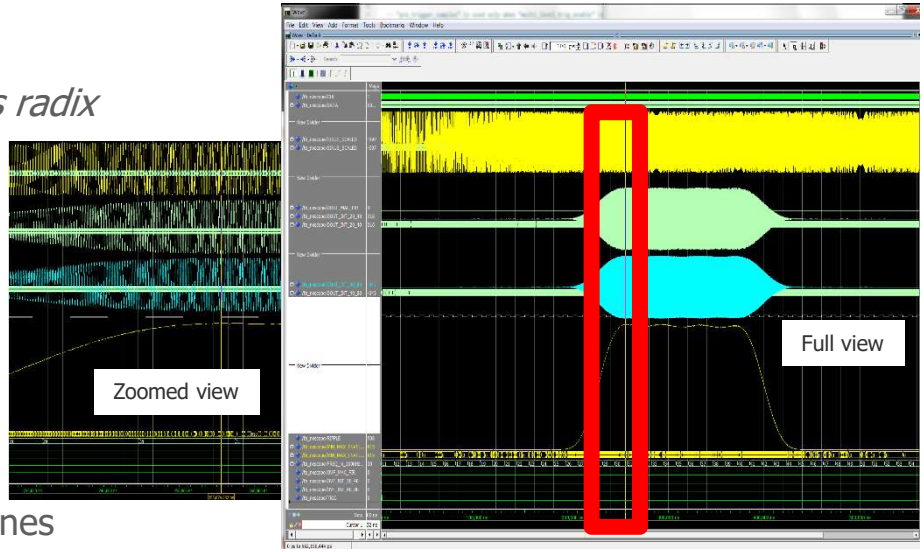
- **Planned within next NXmap versions**
  - *SpaceWire IP core*
  - *DDR Interface (DFI2.1)*
  - *Parallel FIR filters generator (sample frequency > 200MHz),*
- **Planned soon**
  - *Multi Multiplier-Accumulator (MAC sequencial filters)*
  - *Sinus/Cosinus tables,*
  - *Numerically Controlled Oscillator (NCO), Direct Digital Synthetizer (DDS)*
  - *Extended Precision Multipliers,*
  - *Complex Multipliers, …*
- **From NX Eco-system**
  - Adentis/Maya Technology*: Mil-Std-1553B BC/RT,*
  - Cobham Gaisler*: Leon2/3, GRLIB …*
  - Skylabks*: PicoSkyFT-L, and PicoLIB (UART, Timer, I2C, GPIO, …)*
  - STAR Dundee*: SpaceWire, SpW CODEC, RMAP, Routing Switch, even High Perf. FFTs, Image Processing, Camera Interface, CAN…*

NX

NXscope is NanoXplore Embedded Logic Analyser IP core

- Process
  - Nxscope is driven via ANGIE JTAG adapter and NXbase2 (delivered with EK),
  - Create your own ZLA IP core with NanoXplore tools
  - Instantiate the IP Core in the source code of your design
  - Implement the design and check the results
  - Generate the bitstream
  - Launch the Logic Analyzer GUI
    - *Configure the FPGA with the bitstream*
    - *Configure the graphic waveform and signals radix*
    - *Save the graphic setup*
    - *Launch the trigger*
    - *Analyze the results*
- Features
  - Up to 64 sampled lines,
  - Up to 32 trigger lines,
  - Flexible trigger conditions
    - Detection of values and/or edges on trigger lines
    - Programmable pre-trigger samples
    - Multi conditions trigger

WaveForm display with ModelSim



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NanoXplore

From eFPGA to BRAVE & beyond

NG medium

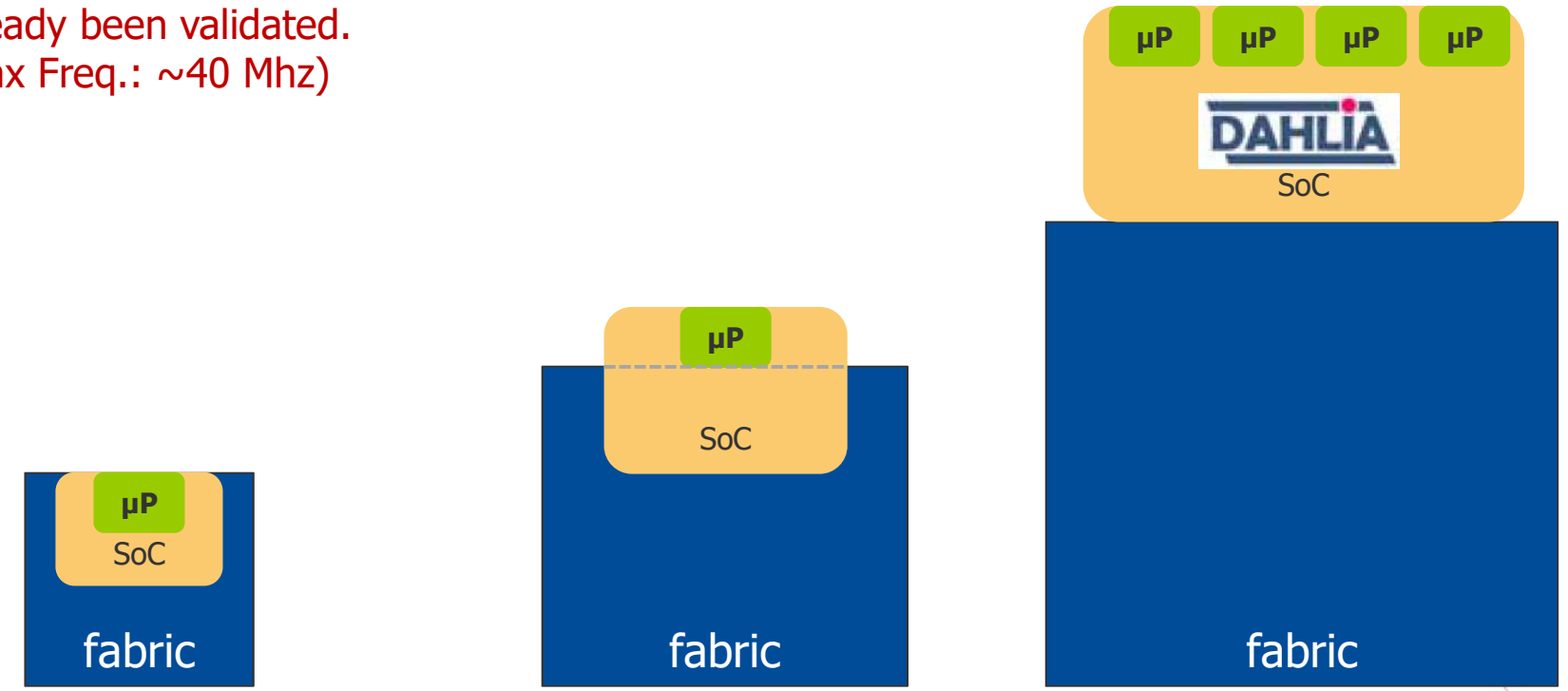
- 34K LUTs / 3Mb RAM
- A SoC can be mapped in the fabric.
- Leon3 based SoC has already been validated. (Max Freq.: ~40 Mhz)

NG large

- 137K LUTs / 10Mb RAM
- ARM Cortex R5 Hard IP
- HSSL
- µP : 200 MHz

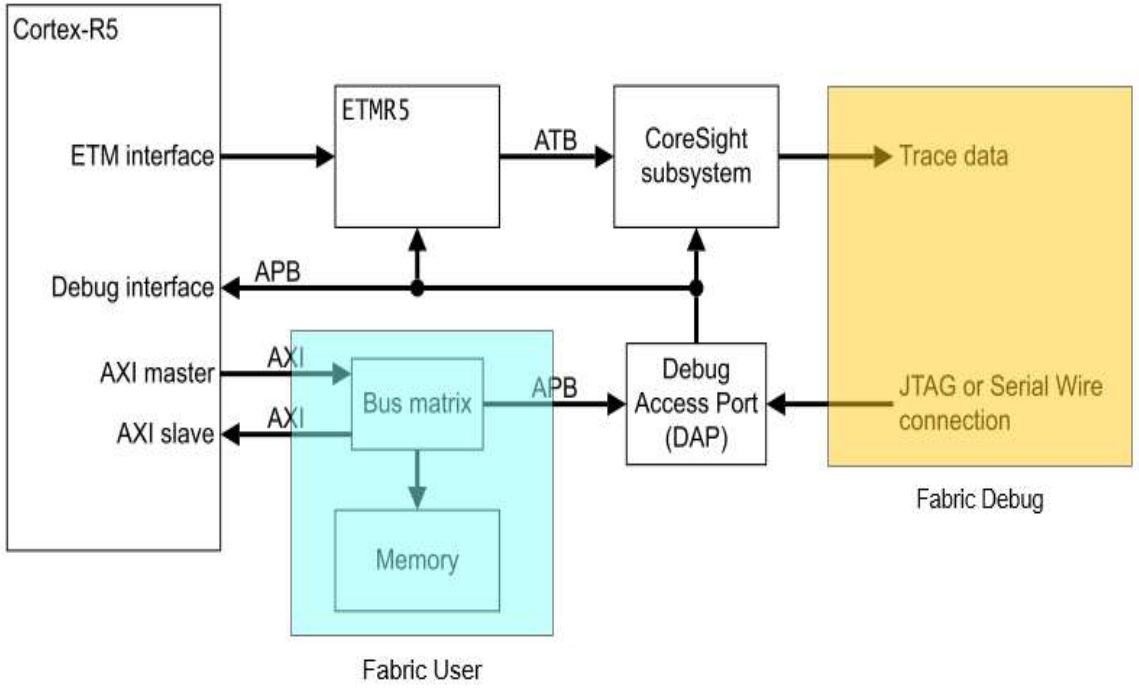
NG ultra

- 517K LUTs / 36Mb RAM
- µP : 600 MHz



NG large - Hard IP ARM Cortex-R5

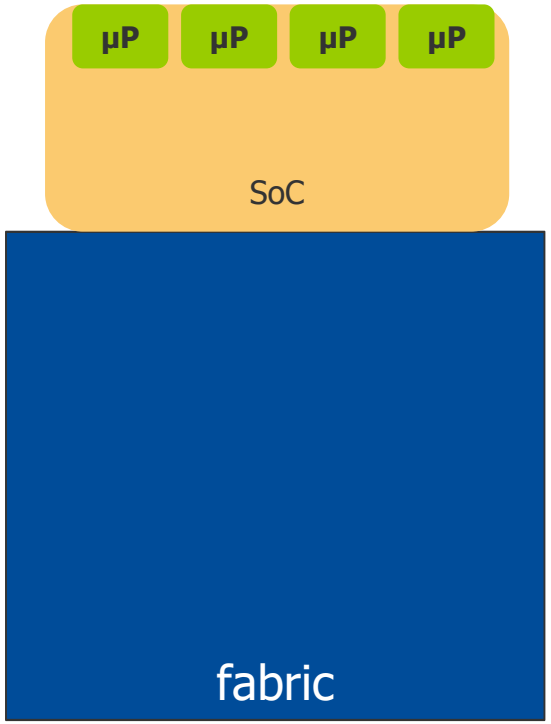
- The Hard IP Processor core NX_Cortex-R5 contains
  - Cortex-R5 CPU
  - CoreSight ETMR5
    (Embedded Trace Macrocell)
  - CoreSight TPIU-Lite
    (Trace Port Interface Unit)
  - CoreSight DAP-Lite
    (Debug Access Port)



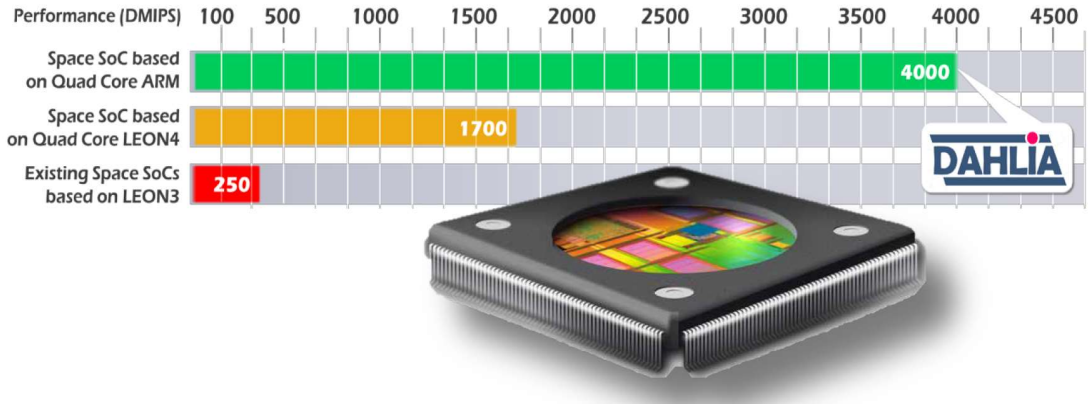
- The Bus Matrix and Users IPs (Memory, IO Controller, CoProcessor) are implemented in the FPGA Fabric.
- The Trace RAM and JTAG/Serial Wire controllers are also implemented in the FPGA Fabric.

NG ultra SoC FPGA

- NG-Ultra becomes a System-On-Chip
  - **4x** FPGA density vs NG-Large
  - Full SoC architecture based on **Double Dual-core ARM Cortex-R52**, optimized for High-Performance, Hard Real-Time applications and **designed to face Space challenges**.

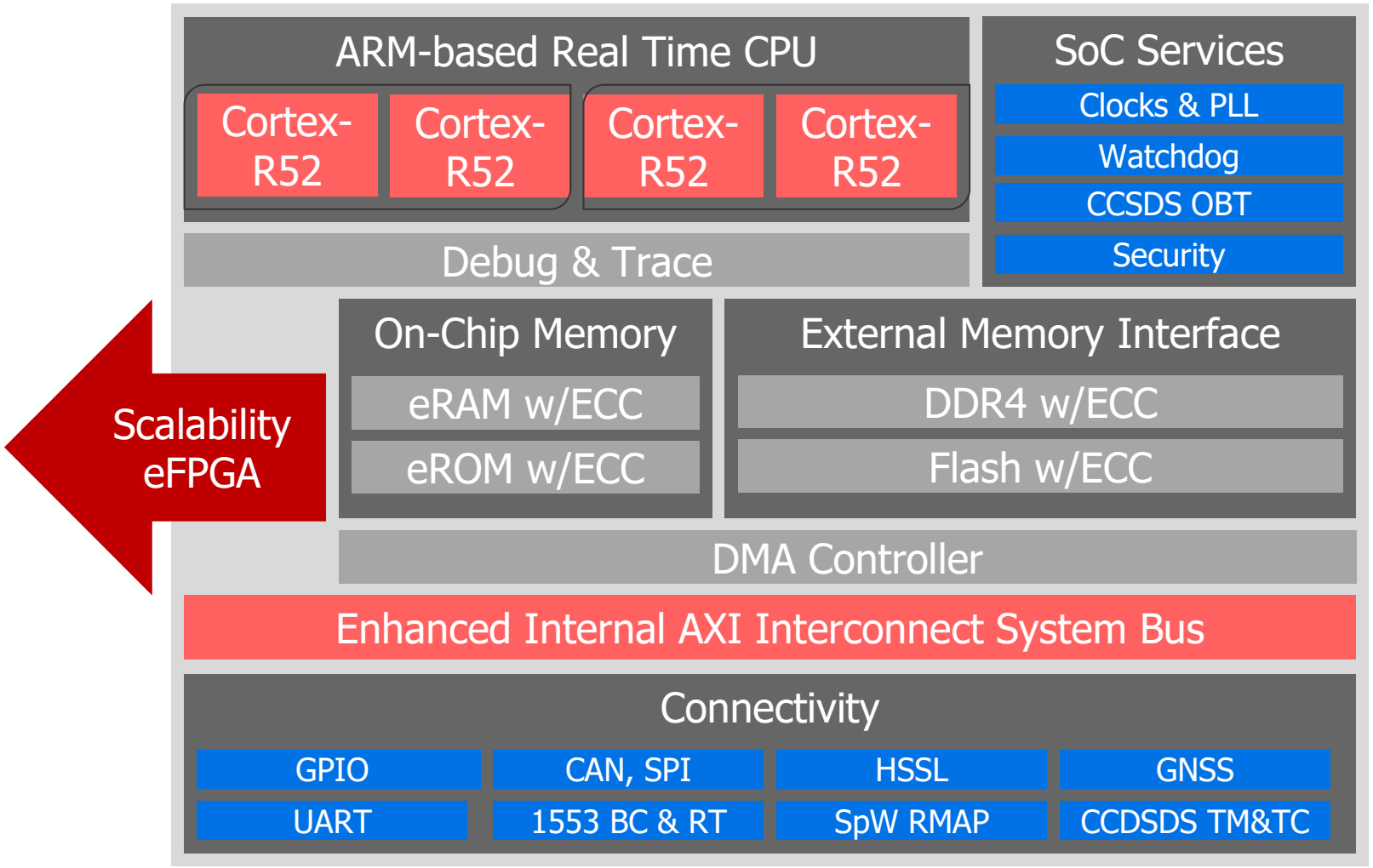


Extracted from ADS DASIA-2017 presentation



NG ultra SoC FPGA

Hereafter the NG-Ultra / DAHLIA SoC architecture



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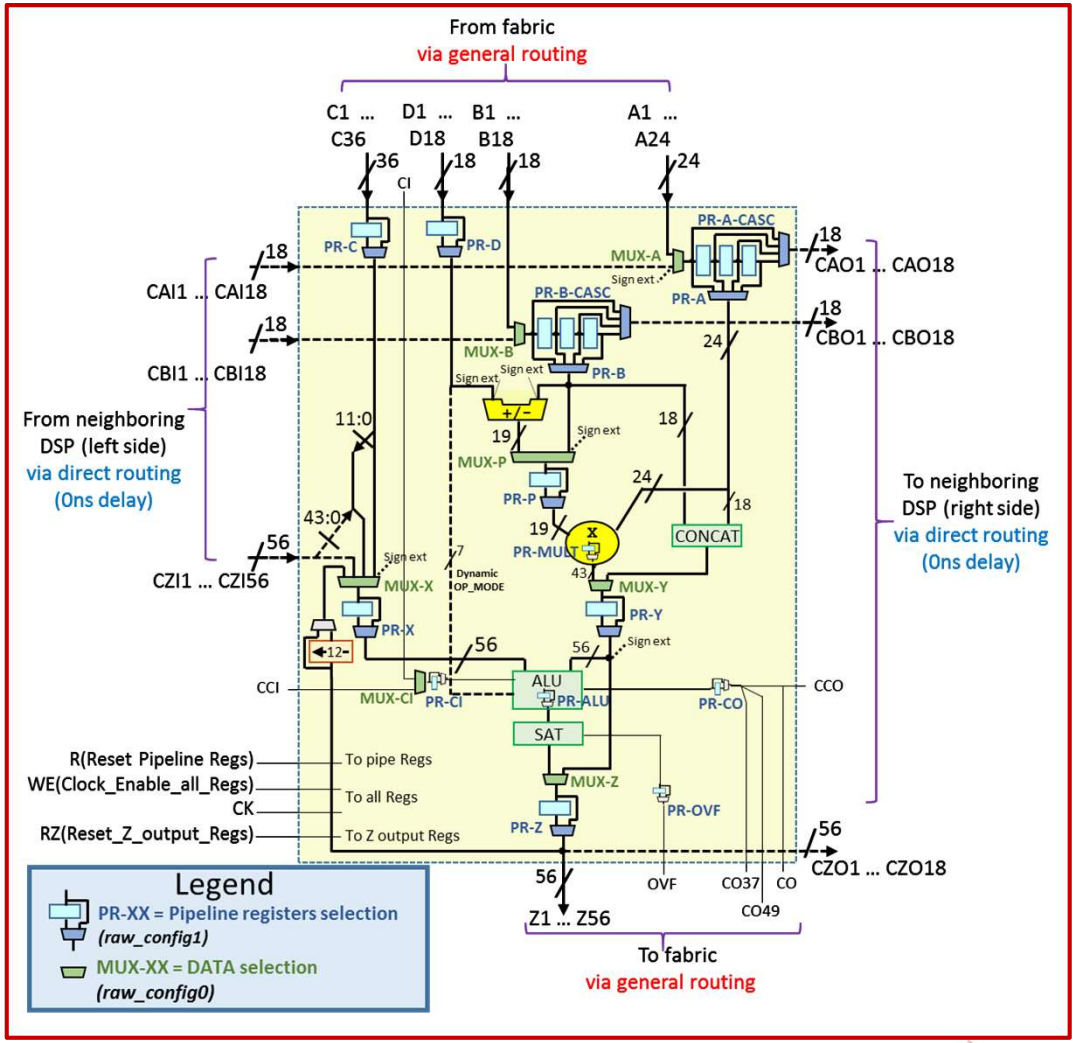
High Performance DSP Block

Allow to implement efficient high rate arithmetic operations such as

- Multiplications
- Adders/subtracters
- Filters
- Fast Fourrier Transform
- Modulation



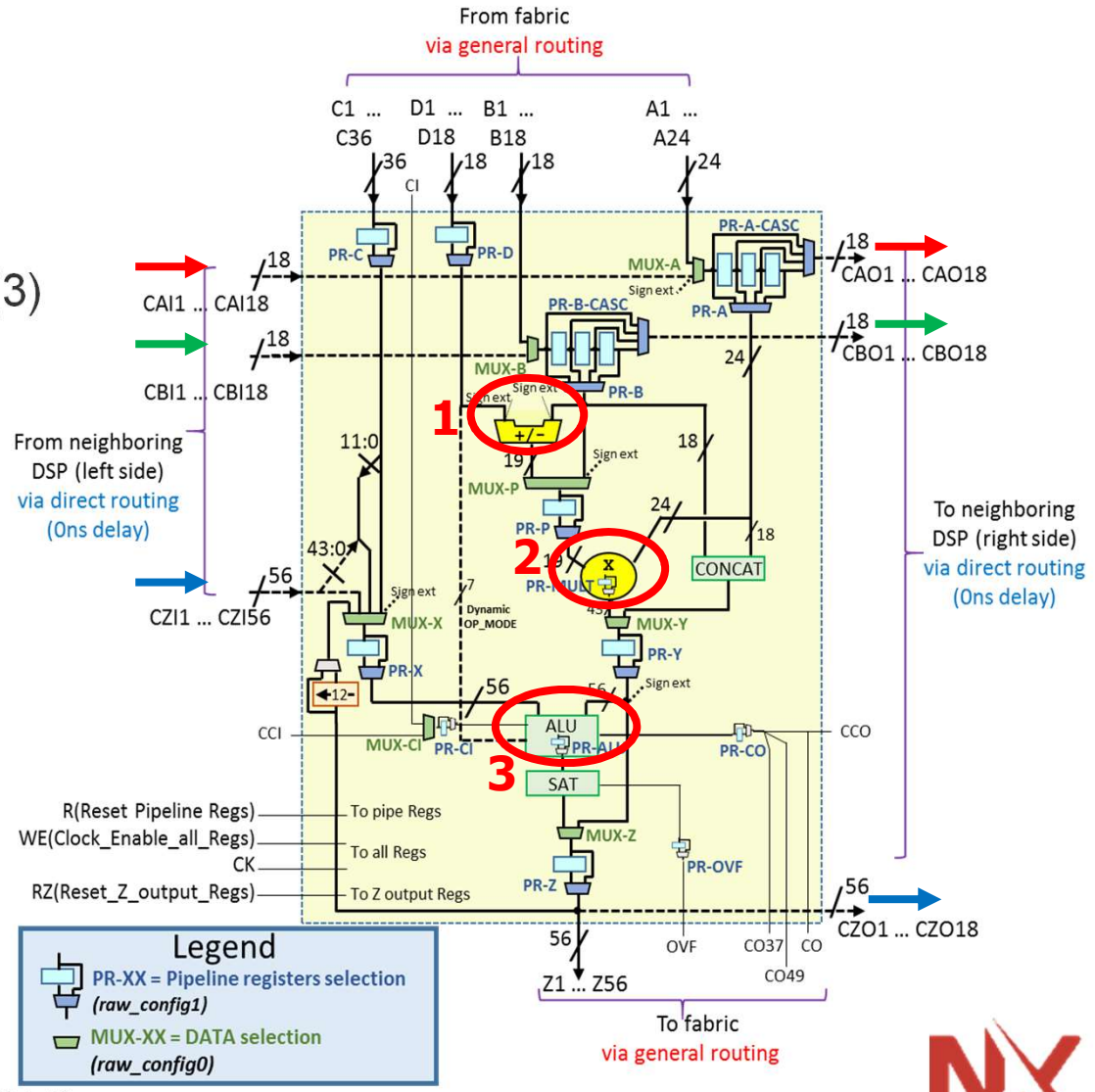
High Performance DSP Block

Three main operators

- Pre-adder/subtracter (1)
- 24x19-bit multiplier (2)
- ALU / post-adder/subtracter (3)

User's selectable levels of pipeline for higher performance

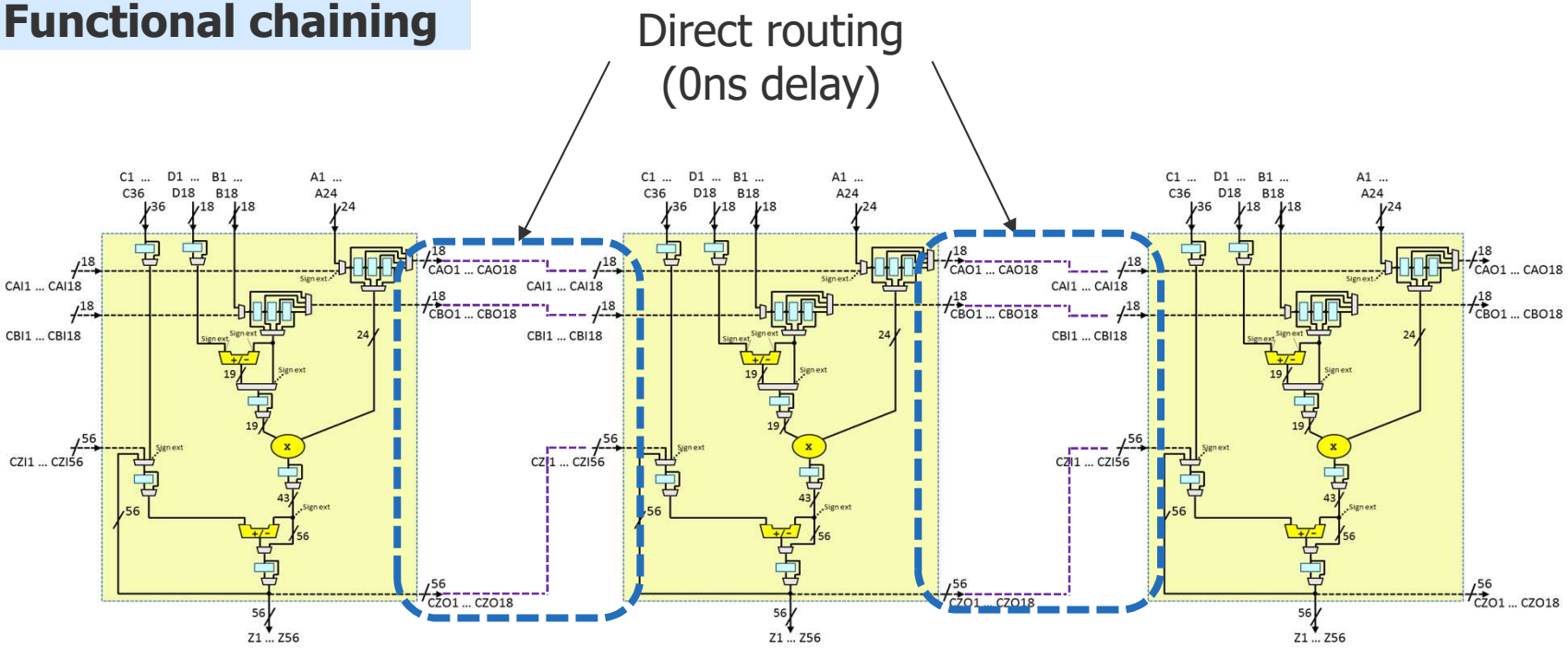
- WE input enables/disables all internal registers
- RST available for internal registers
- RSTZ for output registers (Z)



Chained DSP Blocks

- DSP blocks in the same CGB row can be chained.
- Direct 0 ns delay routing (red, green and blue arrows)

Functional chaining



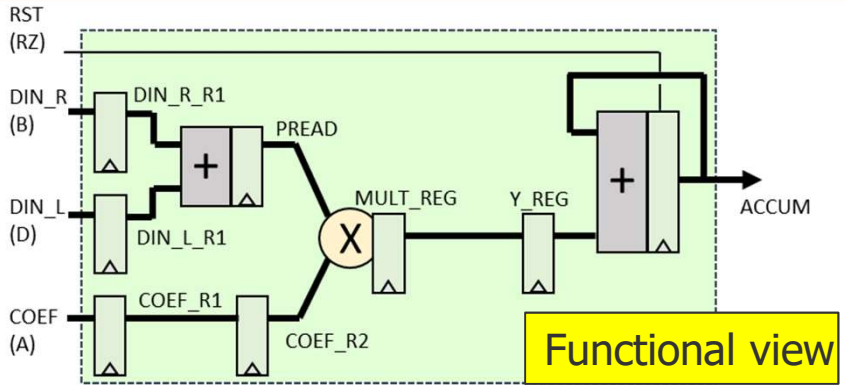
DSP Blocks – 3 solutions

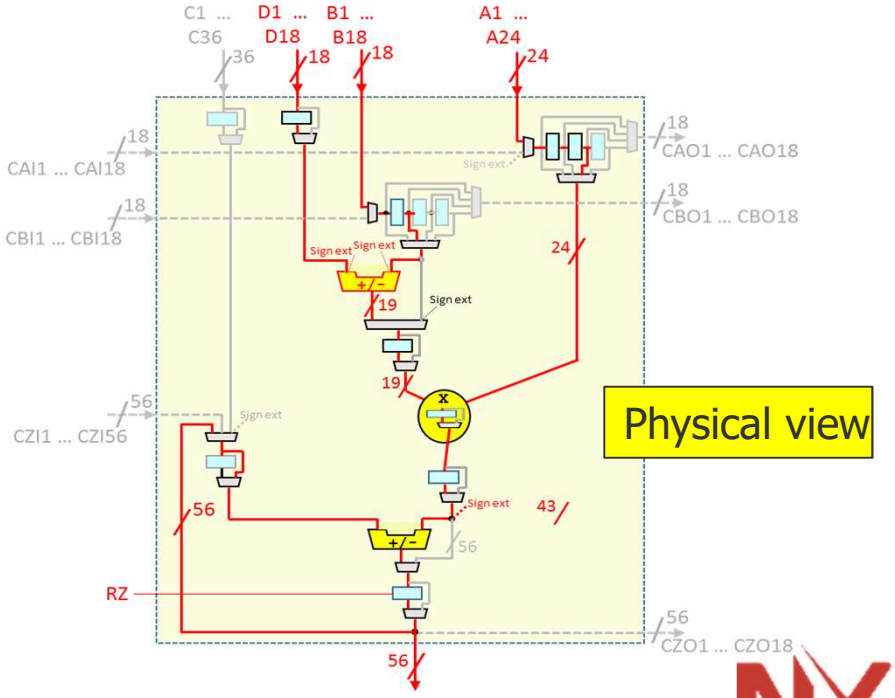
3 ways available

- **Inference** : most common constructs are supported by NXmap synthesis
- **Instantiation** : Gives access to all DSP block features – but less readable
  - Primitive NX_DSP
    - All inputs and outputs are declared as std_logic (no vectors)
    - Generic (parameters) are organized as multibit groups (raw_config#)
  - Primitive NX_DSP_SPLIT
    - All inputs and outputs buses are declared as std_logic_vectors
    - Generic can be assigned by name
- **Using** NXcore : NXcore is NX IP Core generator
  - Can be used to quickly and efficiently generate :
    - Parallel FIR filters (Transpose, Transpose symmetric, Transpose_Dual_Channel, Systolic)
    - Semi-parallel FIR filters

DSP inference

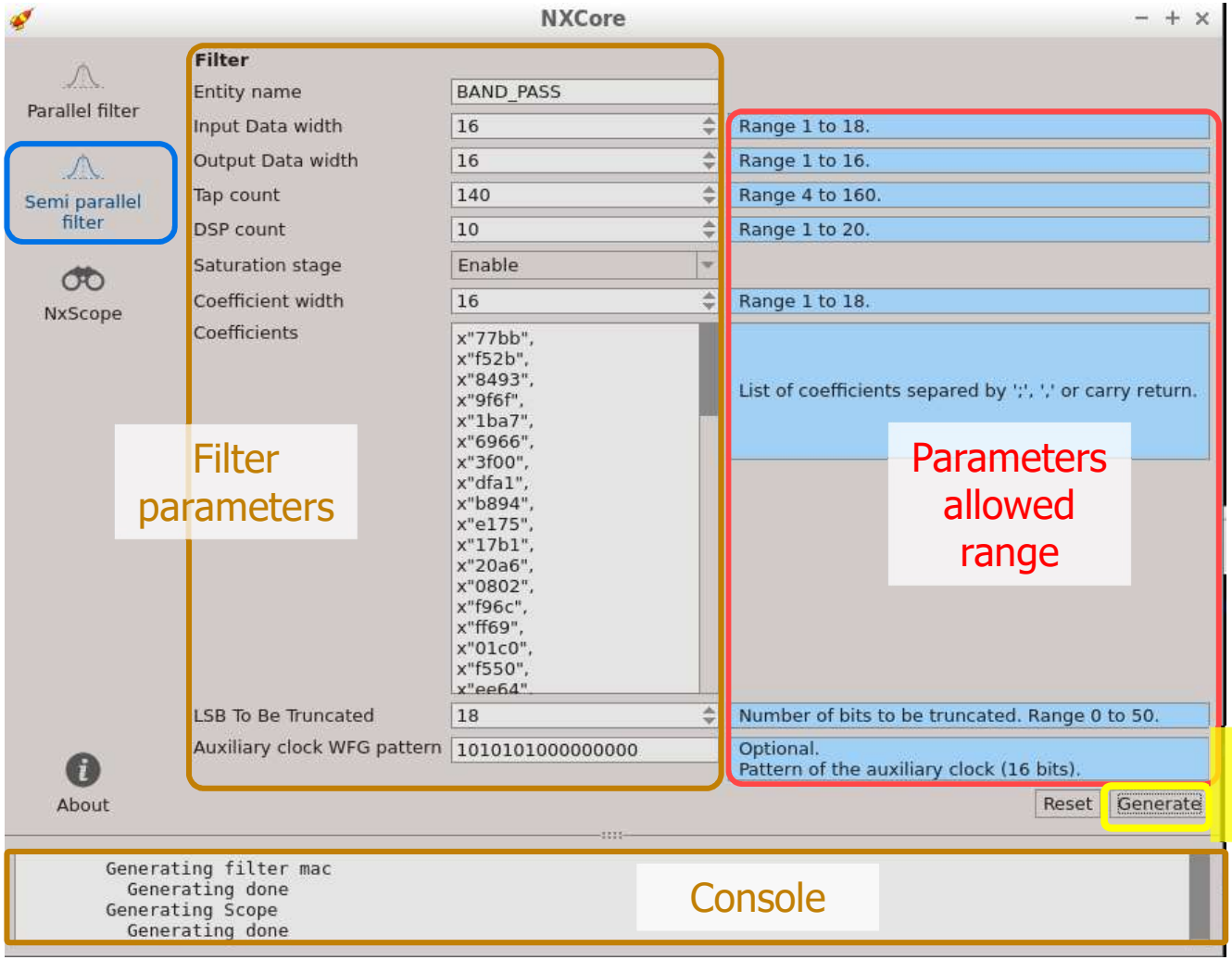
```
process(CLK)  begin
   if rising_edge(CLK)  then
      COEF_R1 <= COEF;
      COEF_R2 <= COEF_R1;
      DIN_L_R1 <= DIN_L;
      DIN_R_R1 <= DIN_R;
      PREAD <= DIN_L_R1 + DIN_R_R1;
      MULT <= PREAD * COEF_R2;
      MULT_R <= MULT;
      if RST = '1'  then
         ACCUM <= (others => '0');
      else
         ACCUM <= ACCUM + MULT;
      end if;
   end if;
end process;
```





DSP implementation with NXcore

IP type selection



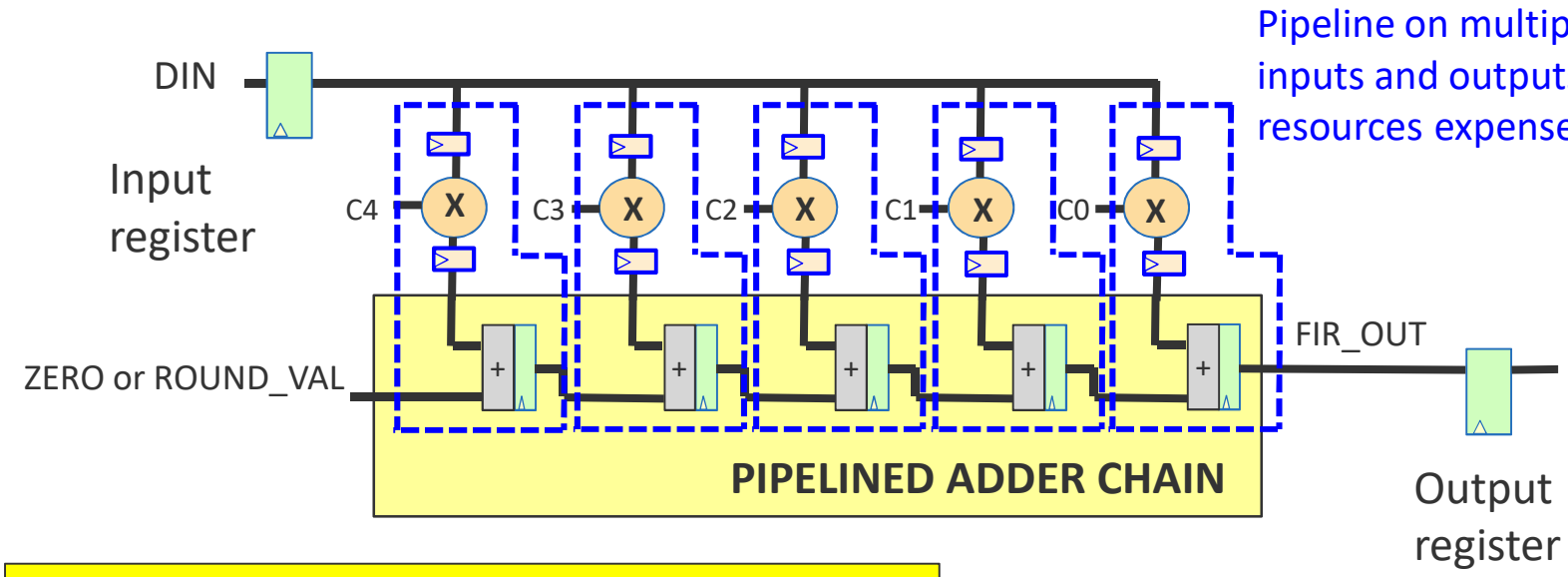
NXcore DSP functions

- **High sample rate Parallel FIR filters**
  - **Transpose or Systolic :**
    - Systolic uses less general routing resources, but has higher latency
    - N DSP blocks for N-tap filter
    - Up to 100 MHz sample rate (into NG-Medium)
  - **Transpose symmeric :**
    - N/2 DSP blocks for N-tap filter
    - 100 MHz sample rate (into NG-Medium)
  - **Transpose Dual Channel (ex : I/Q) :**
    - N DSP block for N-tap filter
    - 50 MHz sample rate (into NG-Medium)
  - **Semi-Parallel FIR filters (not yet available)**
    - Combine tile logic & DSP blocks for shared computation
    - Sample rates : 2 to 25 MHz (into NG-Medium)

- **More functions will be available into NXcore in a near future.**

NXcore // FIR Filter - Transpose

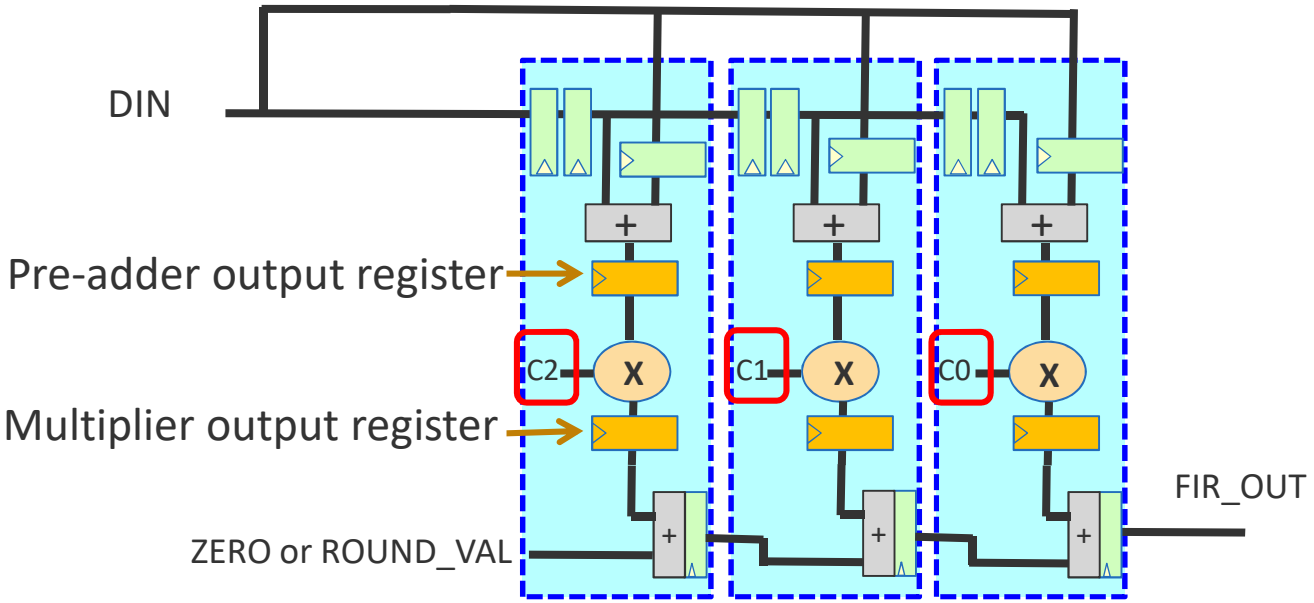
- 100% implemented with pipelined DSP chain
  - Efficient usage of resources
  - High performance
  - Performance is only limited by the input routing and load
  - Reduced latency



Coefficients order : C(N-1) left, C(0) right

// FIR Filter – Transpose Symmetric

- N-tap filter (N= 6 in this example) requires only N/2 DSP blocks
  - No additional DFFs or logic required



Observe the order of the coefficients (C3, C4 and C5 are not used)

Coefficients order : C(N-1) left, C(0) right

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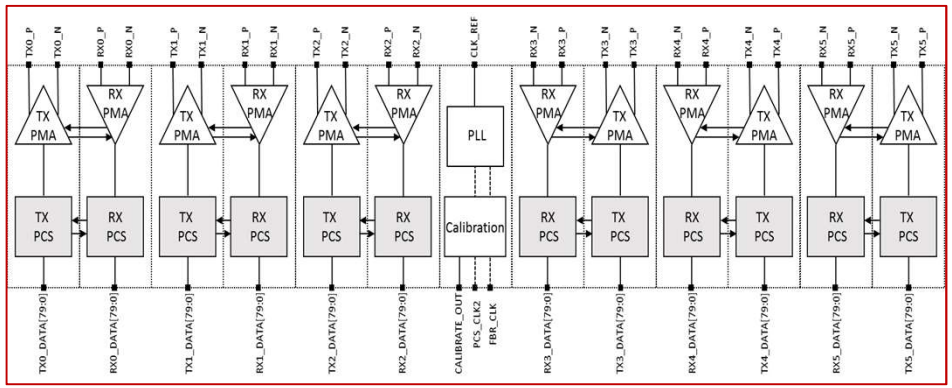
NG large - HSSL overview

- SERDES developed in C65 Space, (acc. VELOCE contract),
- 0.70 – 6.25 Gbps data rate,
- Hex HSSL architecture:
  - HSSL blocks provide multi-protocol high-speed serial link capability with multi-rate support,
  - Hex HSSLs are composed of 6 RX/TX lanes, a PLL, and a calibration circuit.

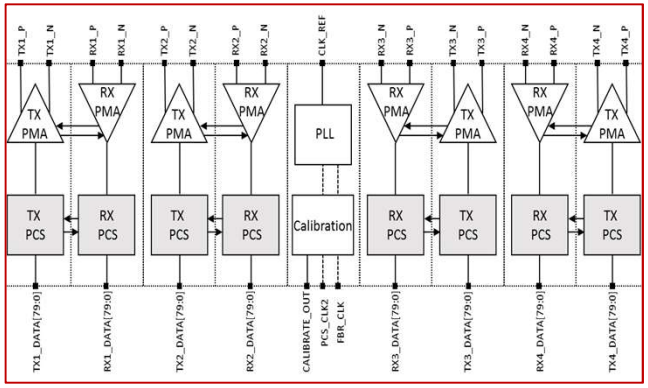


Protocol	Type	Encoding
WizardLink	1,600 – 2,500Gbps	8B/10B
JESD204B	3,125 – 6,25Gbps	8B/10B
ESIstream	3,125 – 6,25Gbps	14B/16B
Serial RapidIO	3,125 – 6,25Gbps	8B/10B
SpaceFibre	3,125 – 6,25Gbps	8B/10B

  - Each transceiver lane includes the PMA and PCS hard macros.
  - The PCS is programmable in order to become compliant with all protocols
  - The SERDES block has configurable features such as data width (up to 80 bits in parallel), equalization and protocol dependent properties.
- NG-Large will embed 4 Hex SERDES ➔ **24 HSSL 6,25Gbps**
- Here above HSSL supported protocols:

NG ultra - HSSL overview

- SERDES developed in C28 Space,
- Hex HSSL architecture:
  - HSSL blocks provide multi-protocol high-speed serial link capability with multi-rate support,
  - Quad HSSLs are composed of 4 RX/TX lanes, a PLL, and a calibration circuit.



  - Each transceiver lane includes the PMA and PCS hard macros.
  - The PCS is programmable in order to become compliant with all protocols
  - The SERDES block has configurable features such as data width (up to 80 bits in parallel), equalization and protocol dependent properties.
- NG-Ultra will embed 8 Quad SERDES ➔ **32 HSSL 12,5Gbps**

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Thank you


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