SEFUW: SpacE FPGA Users Workshop, 4th Edition

Monday 09 April 2018 - Wednesday 11 April 2018

European Space Research and Technology Centre (ESTEC)

SEFUW 2018 is organised with the support from COMET by CNES and ESA's Data Systems and Microelectronics Division

Monday 9 April 2018

Registration and Early Morning Networking Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division (09:30 – 10:00)

Welcome to SEFUW 2018 (10:00 - 10:30)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: Industrial Experiences (10:30 – 11:30)
Chair: *Mr. DANGLA, David (CNES)*

10:30	**FPGA experience and SoC design methodology at Airbus Defence & Space. (00h20')** *Presenter: Mr. RIED, Ottmar (Airbus Defence & Space GmbH)* Since years Airbus Defence and Space capitalizes on the advantages of Field Programmable Gate Array Technologies and has accumulated considerable heritage and experiences with it. This presentation provides with an overview of the application domains and the FPGA devices that address those application fields. That extends from the well-established Microsemi anti fuse FPGAs (RTSX/RTAX) to more recent and flexible reprogrammable devices (PA3, RTG4, SPARTAN-6, VIRTEX-4/5, BRAVE). Particular consideration will be payed towards the experiences associated with the European BRAVE medium FPGA. Application domains and benefits will be discussed. As all recent technologies augment significantly in complexity, in resources and functionality, new scopes and opportunities will be discussed. Regardless the technology, all recent devices have a significant rise in complexity in common. This changes also the application of the FPGAs from a dedicated function solution to a complex system on chip (SoC) with influences on the total development approach. From user point of view, the equipment complexity is inside the FPGA which integrates a large part of numeric hardware, data handling software and application software. The FPGA specification is more a system specification and is distributed in several module specifications with clear interfaces in order decreasing the complexity. So it is necessary to have a strong interaction between the system engineer who has the responsibility of the system behavior, the FPGA team and the software team. The information described in a specification is not sufficient anymore in a complex system, an executable specification which describes the functionality and can be used as a golden reference may be an answer but also the participation of the system engineer to the FPGA co-design phase should be required. In fact, fast loop co-engineering phase is necessary during the major part of the design phase to resolve the equipment complexity. From user point of view, the fast exchanges during co-design allow to make the trade-offs on various subjects such as power, timings, data accuracy, functional behavior, resources utilization. From equipment designer point of view, a potential drawback is that the design is more showed up even if the design is less risked. Finally our experiences with Mentor Vista will show an example of a tool supporting a SoC design approach.
10:50	**Jena-Optronik Experience Summary on Microsemi RTG4 designs (00h20')** *Presenter: BOTH, Johannes (Jena-Optronik)* Thanks to its robust design and accurate measurements, the Jena-Optronik RVS© LIDAR sensors are the most frequently used rendezvous- and docking sensors for ISS resupply by the European ATV, Japanese HTV and the US-American “Cygnus” transport vehicle built by Orbital ATK. The RVS sensor is limited, though, to rendezvous and docking with cooperative targets, i.e. targets equipped with retro-reflector elements. For future applications like on-orbit servicing, space debris removal or planetary landing, a more powerful 3D imaging LIDAR system is required. Following the ESA sponsored technology development activity “ILT” (Imaging LIDAR Technology) and the DLR project “LiQuaRD” (LIDAR Qualification for Rendezvous and Docking), a concept for a new powerful, yet compact and cost-effective LIDAR system was developed to both replace the previous RVS sensor and enable additional mission scenarios: the RVS3000 product family. The RVS3000 product family currently consists of two LIDAR versions: The RVS3000 for cooperative targets using retroreflectors (e.g. ISS) and the 3D imaging version RVS3000-3D, capable of performing relative navigation with uncooperative (diffuse) targets in scenarios ranging from Satellite Servicing to Debris Removal. Current developments at Jena-Optronik for

		the RVS3000-3D are aimed at integrating LIDAR image processing techniques for real-time 6 degrees of freedom (6DOF) Pose Estimation with uncooperative targets. Such integration is intended to work with the sensor through a standardized interface in order to allow the use of both third party SW and proprietary algorithms developed by Jena-Optronik. Those algorithms require a high performance computing hardware, thus, a standard spacegrade FPGA or processor is not sufficient anymore. Making a step forward towards high-performance in orbit data-processing, Jena-Optronik has developed a universal multi-purpose hardware module which is already preselected for multiple missions. The module utilizes the Microsemi RTG4 FPGA as main computing unit. It is supported by multiple persistent and high-speed memory modules. Communication is realized by up to 6 SpW ports which can run, thanks to the RTG4 integrated SpW clock recovery circuits, at up to 200 Mbps each. A main challenge for RTG4-based designs is the PCB mounting technology for the CCGA1557 package with 1 mm pitch. Jena-Optronik is currently qualifying a solder process utilizing a low-CTE PCB material together with mechanical support structures for the FPGA package. The concept has already been developed for SMT qualification of the Xilinx Virtex 5 FPGA, which was successfully completed in 2015. The second part of the presentation will focus on experience made during FPGA design process. Jena-Optronik will provide feedback on different aspects of the tool chain, RTG4 related design restrictions and Microsemi support. Finally, a summary of the design results of the current project will be presented.
	11:10	**SpaceFibre, Spectrometer and Camera: Some applications on the RTG4 FPGA (00h20')** *Presenter: Prof. PARKES, Steve (University of Dundee)* STAR-Dundee has extensive experience with demanding applications on the Microsemi RTG4 FPGA. Single-lane and multi-lane SpaceFibre IP cores have been designed and tested on the RTG4 along with other SpaceFibre IP cores. This serial interface IP runs at 3.125 Gbits/s using the internal SerDes of the RTG4. An FFT-based spectrometer has been designed which performs a 1k-point complex FFT at 2.4 Gsamples/s. An intelligent camera with both SpaceWire and SpaceFibre interfaces has been developed with an RTG4 coupled to an image sensor. The RTG4 is able to perform image compression or image processing task remotely. The SpaceFibre interface is able to send data at very high speed and to provide camera configuration, control and housekeeping services. These applications will be described.

Session: Design Flow (11:30 – 12:10)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	14:20	**Universal VHDL Verification Methodology. Setting a standard for VHDL testbenches (00h40')** *Presenter: Mr. TALLAKSEN, Espen (Bitvis)* For an FPGA design we all know that the architecture – all the way from the top to the micro architecture – is critical for both the FPGA quality and the development time. It should really be obvious that this also applies to the testbench. Most FPGA designs are split into stand-alone modules – for instance for each of the FPGA external interfaces. In VHDL these modules are VHDL entities (components), and they are normally accessed from a CPU via a more or less standardized register interface, which acts as an abstraction layer. This abstraction allows a safe and very efficient control of the complete FPGA. It is clear that this approach should also be used for the verification environment - to simplify the testbench architecture and the control of the interfaces. This way the verification structure will mirror the design structure, allowing the best possible overview, readability, maintainability and reuse. UVVM provides a very simple and powerful architecture for this – to allow designers to build their own test harness much faster than ever before – using a mix of their own and open source verification components. Constrained random and Functional coverage may be used seamlessly with UVVM, and a current ESA project will make it simpler to control these features and combine with scoreboards, error injection, monitors and more. UVVM is only two years old, but has received great feedback from both users and large international players, and is already being used world-wide. The next major step for UVVM is an on-going project with ESA to make this verification methodology even better.

		This presentation will show you 1) how simple a UVVM testbench is to understand, build and control 2) how UVVM is standardising the VHDL testbench architecture 3) how the new ESA extensions will complete the VHDL testbench environment

Tools Vendors (12:10 – 13:00)
Chair: *Mr. MANNI, Florent (CNES)*

	12:10	**Multiple-clock Domain FPGA Designs: Challenges and Solutions (00h25')** *Presenter: Dr. DOBKIN, Reuven (vSync Circuits)* Inter clock domain crossings inside multiple clock domain design must be treated carefully in order to eliminate synchronization failures and assure design reliability. For space applications, the reliability assurance is crucial, calling for employment of state-of-the art design integration and verification techniques. The problem is exacerbated by the fact that the synchronization bugs can be possibly generated by an incorrect automatic design optimization during synthesis and P&R stages, especially for designs having high area utilization, leading to low reliability designs. During the lecture we will survey common synchronization problems that arise during a design that targets a FPGA device. The survey will cover different design stages, starting from the RTL design using FPGA IP modules and down to synthesis, P&R and gate-level verification stages. In addition, we will suggest and discuss possible solutions to the presented problems at each one of the design stages. We will present a possible design methodology, leading to high reliability designs and to a shorter time to market, minimizing the time spent on synchronization bug fixing during lab testing.
	12:35	**RTL Analysis and CDC Analysis for Maximum Design Efficiency and Quality (00h25')** *Presenter: Mr. CALKINS, Scott (Blue Pearl Software. Inc)* ASIC and System on Chip (SoC) design and verification practices have traditionally been much more rigorous than that of their FPGA counterparts. Mandated by large non-recurring engineering (NRE) fees associated with the manufacturing setup, design teams set up robust verification methodologies that are rigorously followed to avoid errors that could cause an expensive re-spin. With NRE fees in the range of $100's of thousands to several million depending on the complexity and process node of the ASIC or SoC, there is no room for error. Satellites by nature are produced in low volume making them an ideal candidate for FPGAs over ASICs and SoCs, however on a satellite there is also no room for error. Unfortunately, many FPGA design flows fail to incorporate the same level of verification as their ASIC counterparts. While the FPGA vendors do supply quality tools for simulation, synthesis and place and route, they are light on verification and thus can miss or highlight problems very late in the design cycle. The more complex FPGA become, the more complex and sophisticated the tools supporting their development and verification need to be. For example, in space the SpaceWire interconnect (coordinated by the European Space Agency (ESA)) provides a high speed, low power standard serial interface for a wide range of system requirements. In this talk I will showcase how a verification methodology that includes Super-lint advanced static and formal analysis along with clock domain crossing analysis can highlight potential issues when interfacing between original content and a SpaceWire core. Super-lint identifies poor coding styles, improper clocks, simulation and synthesis problems, poor testability and other source code issues. FSM analysis automatically extracts and analyzes finite state machines for dead or terminal states and provides a visual representation. X-propagation analysis detects unknown states, often introduced into designs to implement soft resets or to implement power management schemes and are masked during RTL simulation. I will showcase how leveraging a documented verification methodology can pinpoint issues that may go unnoticed in simulation and even worse, in production.

Networking Luncheon (13:00 – 14:20)

Session: Tools Vendors (14:00 – 15:10)
Chair: *Mr. MANNI, Florent (CNES)*

	14:00	**Build and Debug Highly Reliably FPGA-based Designs (00h25')** *Presenter: Mr. JACOBSOHN, Philipp (Synopsys)* Deploying FPGAs in high-assurance applications makes it necessary to protect the device against malfunction. SEU mitigation and error monitoring circuitry is a mandatory prerequisite for any FPGA design used in high radiation environments. Designing SEU-tolerant circuits can be done in manual or automated ways by introducing design techniques such as triple-mode-redundancy and safe implementation of state-machines. Important considerations when choosing an appropriate design flow include not only “design time” as well as “designer expertise” but also “area and power increase” for the circuit as it can affect system cost and reliability of the circuit. This paper discusses mitigation techniques available for different types of FPGAs (Antifuse, Flash-EPROM or SRAM), area/power/performance tradeoffs for each technique. This paper will also talk about how to reduce such overheads with right voter logic location, pipelining of error monitoring/detection etc. In addition, it will cover the ability to add debug capabilities within the scope of triplication and allow developers to easily see each triplication and voter to verify and monitor whether the SEU mitigation techniques are working as expected. It will introduce the audience to the Synplify Premier tool which allows to automatically introduce features such as TMR to FPGAs from all major vendors.
	14:25	**Advanced Verification for FPGAs (00h25')** *Presenter: Mr. CATENACCI, Simone (Mentor, a Siemens Business)* Emerging design methodologies and increasingly complex FPGAs are creating a need for new approaches to verification to keep pace. As a result, the balance is shifting as more FPGA users want and need to adopt modern verification practices in order to be competitive but don't always know where to start or find the cost/risk too great to embark on. This session will discuss themes in the FPGA industry that are pushing the need for advanced verification, help you understand how other FPGA users in industry are adapting to this and explain how taking a new look at your verification methodologies can help you build higher quality, on-time products enabling you to be more competitive in today’s evolving FPGA market.
	14:50	**Exhaustively Verify SEU Mitigation Techniques Using Formal Verification (00h20')** *Presenter: Mr. HANDOVER, Mark (Mentor, A Siemens Business)* In recent years, Formal verification has moved beyond a tool solely for use by experts and into the mainstream. Now, targeted formal apps’ are lowering the barrier to entry for formal, enabling its use in automated design checking, clock domain crossing analysis and coverage closure to name a few. This session will briefly discuss a range of formal apps’ available before focusing on one particular use case - how automated, formal-based Sequential Logic Equivalency Checking (SLEC) techniques can exhaustively verify the effectiveness of the Single Event Upset (SEU) mitigation logic vs. transient/SEU events — as well as stuck-at and bridging faults. To illustrate this, a case study describing fault analysis of a Triple Modular Redundancy (TMR) element will be presented; including fault population reduction, fault injection, checking and classification, and collection of metrics. Finally, we will compare formal results and run time against those obtained using dynamic simulation techniques, and show how formal is able to minimize the analysis effort required.

Session: Design Flow (15:10 – 15:30)
Chair: *Ms. SANTOS, Lucana (ESA)*

	15:10	**Evaluation of MATLAB/Simulink and RTL VHDL HDL environment (00h20')** *Presenters: Mr. BRAVHAR, Klemen (ESA), Mr. VAN BEEK, Stephan (MathWorks)* The FPGAs for space are growing in complexity and performance and the design time is shortening. There are several high-level synthesis approaches that aim to help FPGA designers increase their productivity. The objective of this work is to assess the MATLAB/Simulink high-level design flow, by using 2 applications from the specification to the deployment into different FPGA platforms. For the assessment, two FPGA design flows have been used: the high-level FPGA MATLAB/Simulink and the RTL VHDL coding. The applications chosen are Vision algorithms, as

	they are highly parallelizable and therefore use all advantages of FPGA (pipelines, DSP, Memory) to reach real time data handling/ manipulation. In this manner we developed Green Screen and Edge Detection (Sobel filter) FPGA applications. In the MATLAB/ Simulink design flow we used the HDL coder/Vision HDL Toolbox to produce VHDL. In both FPGA design flows, the VHDL of the applications has been simulated to verify the functionality and then we executed the implementation on Xilinx and NanoXplore FPGAs. Several metrics have been obtained at the end of both design flows - such as resources used, achieved frequencies, overall development effort - in both FPGA technologies.

Session: FPGA Vendors (15:30 – 15:50)
Chair: *Ms. SANTOS, Lucana (ESA)*

15:35	**FUSIO RT: A New Space Modular Computer Core based on Nanoxplore NG-Medium FPGA (00h20')** *Presenters: Mr. WANG, Pierre-Xiao (3D PLUS), Mr. BERTHET, Pierre-Eric (3D PLUS)* FPGA based computer unite is quite common in space design thanks to FPGA's high flexibility, high performance and its short time to market and unit low cost. On the other side, whatever the application is, a SRAM based FPGA need to use the bitstream memory, and most cases computing memory and mass memory to build its eco system. Cooperating with Nanoxplore, 3D PLUS develops a modular computer core: a single 3D stacking module based on first European radiation hardening FPGA NG-Medium. This single module can be considered as a complete computer with modular design, with microprocessor (inside of NG-Medium FPGA), memories, input/output (I/O) and other features required of a functional computer. FUSIO RT integrates NG-Medium FPGA based on STM 65nm RH process. the FPGA has 550K Gates, integrated Space Wire interface, Multiple I/O power support from 1.5V to 3.3V, Cold sparing support, 800 Mbps I/O support, LVDS compatible mode and On-chip thermal monitoring capability. To configure the FPGA, the module integrates 128Mb radiation tolerant high speed SPI memory with Triple Modular Redundancy (TMR) with embedded bit stream integrity check. This bitstream memory is the basic configuration of the FUSIO RT module, and 3D PLUS provide the develop kit to program the SPI memory. Further than the bitstream memory, the users can select optional computing memory, radiation tolerant SDRAM – from x8 to x24b, which will add an additional stacking layer but keep the same module footprint. Along with different bus width, the SDRAM will be from 512Mb to 3Gb. Same story for optional mass memory, the module can integrates radiation tolerant Nand Flash – from x8b to x32b bus to adapt to different speed, From 16Gb to 64Gb configurations, 100K erase/program cycle and 10 years data retention. In this case, the module will add one or two additional stacking layers and still keep in the same module footprint. Moreover, as the space memory leader, 3D PLUS can provide SDRAM Controller IP core to manage the optional DRAM – max x24b wide computing memory, and also Nand Flash Controller IP core to manage the optional Nand – max x32b wide mass memory. These memory controller IP cores were tailored to 3D PLUS memories, and integrated radiation mitigation to make the memory radiation hardening by System (RHBS). Last by not least, as a modular design, whatever the module configuration selected by the users: FPGA + only configuration memory or FPGA + configuration memory + computer memory or FPGA + configuration memory + computer memory + mass memory, this modular will be integrated Inside of same footprint: BGA484 1.27mm pitch (LxW=32x32mm), but with different height (more stacking layers) , and have minimum 262 user I/Os (in case of SPI+SDRAM+Flash) available, and Temperature range: -55 to +105°C.

Session: Fault Tolerance Methodologies and Tools (15:50 – 16:30)
Chair: *Ms. SANTOS, Lucana (ESA)*

15:50	**Analysis and Mitigation of Single Event Upsets in Configuration Memory of Xilinx Kintex7 SRAM-based FPGA (00h20')** *Presenter: Dr. DU, BOYANG (Politecnico di Torino)* Radiation test has been widely used as one of verification methods able to provide accelerated,

		realistic environment especially for space applications to evaluate device and system reliability against effects induced by charged particles. As for SRAM-based FPGA, one of the popular reconfigurable devices on the market providing high performance and flexibility, Single Event Upset (SEU) in configuration memory is a major concern due to high sensitivity of SRAM cell against radiation effects. Traditional techniques such as Triple Module Redundancy (TMR) and scrubbing introduce large area and performance overhead, previously developed analysis and mitigation methods demonstrated to effectively increase the overall FPGA circuit reliability without adding critical hardware overhead. In this work, radiation test results of Xilinx Kintex7 device using Ultra High Energy (UHE) heavy ion beam is presented with preliminary analysis. The UHE beam was used to emulate the environment of the space application especially of those targeting on deep space exploration. An ARM-based SoC was used as benchmark circuit with a bubble sort application as test program. Two versions of the design have been prepared, namely 1) Plain, original version of circuit design; 2) XTMR, Plain version with Xilinx TMR tool applied. Experimental data and preliminary analysis of the radiation test show that 1) XTMR version has only 50% sensitivity against SEU in configuration memory comparing to Plain version, w.r.t. error rate cross section 2) our analysis tool VERIPlace is able to have an accurate evaluation of the system reliability, calculated as the probability of an error in output when certain of SEUs accumulated in the configuration memory, with both the Plain and XTMR version. Another version of the design with VERIPlace mitigation technique applied is planned in upcoming test for verifying the mitigation effectiveness.
	15:35	**Fault injection for space: FT-Unshades2 updates, experiences and roadmap (00h20')** *Presenter: Prof. GUZMÁN-MIRANDA, Hipólito (Universidad de Sevilla)* Fault injection is a promising technique for predicting the SEU Architectural Vulnerability Factor (AVF) of digital designs for space applications. Unfortunately, learning and using fault injection emulation tools needs a time and effort investment that may discourage development teams from applying the technique. Furthermore, there is an understandable concern in the design community about when and by how much the technique is accurate, with respect to the real AVF values that would be obtained in a radiation test. The FT-Unshades2 fault injection platform aims to mitigate these issues so fault injection can be efficiently used, in the early stages of a design effort, to predict and mitigate SEU-induced effects on digital designs. Updates on the FT-Unshades2 fault injection platform will be presented, with also the typical workflow provided by its Graphical User Interface. Experiences on using the platform on real designs for space applications and how to extract the most relevant information from them will be presented. Finally, version 4 of the platform, which will support the new European Space-Grade FPGA, NG-MEDIUM, will be presented.

Networking Coffee Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division (16:30 – 17:00)

Demo Session and Cocktail Reception sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division (17:00 – 18:45)
Chair: *Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)*

Tuesday 10 April 2018

SEFUW Intro – Opening Remarks (08:50 - 09:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: FPGA Vendors (09:00 – 10:00)
Chair: *Mr. FERNANDEZ-LEON, Agustin (ESA)*

09:00	**Xilinx On-Orbit Reconfigurable Kintex UltraScale FPGA Technology for Space (01h00')** *Presenter: Mr. ELFTMANN, Daniel (Xilinx)* Space Electronic designers have long desired to have the same capability that terrestrial based electronic system designers have for adaptation, improvement, and flexibility in their digital signal processing architecture. The initial Xilinx Virtex-5 SRAM based Field Programmable Gate Array (FPGA) technology was introduced into the terrestrial marketplace in 2007. The work on the Virtex-5QV devices with Radiation Hardened By Design (RHBD) elements began earlier (2005) than the Virtex-5 commercial product market introduction. The additional work to complete the Virtex-5QV (SIRF- Single-event Immune Reconfigurable FPGA) RHBD modifications and required qualification testing led to a space market introduction of this technology in 2012. The Xilinx Virtex-5QV (SIRF), currently in use in both commercial and military satellite programs, delivers high system reliability together with advanced flexibility and processing capability in a RHBD product. Today the Virtex-5QV product delivers excellent SEU characteristics with on-orbit reconfiguration capabilities. However, as the pace of satellite electronic designs continue to require increasing levels of high performance on-board signal processing, the space market now needs increased levels of performance, integration, and I/O capabilities. In November of 2017, Xilinx announced the plans to deliver the next generation of radiation tolerant FPGA technology for future space electronic systems. The commercial 20nm TSMC Kintex UltraScale devices have performed well in Single Event Effect testing performed by Xilinx, NASA, and Sandia National Laboratories. With no identified need for additional RHBD modifications, the Kintex UltraScale technology for next generation space electronic architectures is targeted for market availability in late 2019, just 5 years after first shipment of the technology for commercial terrestrial applications. In this session, Xilinx Space System Architect, Daniel Elftmann will walk through product architecture, SEE characteristics, and eco-system developments associated with the next Xilinx Space product, which will be the XQRKU060-CNA1509 device.

Session: Industrial Experiences (10:00 – 10:20)
Chair: *Mr. FERNANDEZ-LEON, Agustin (ESA)*

10:00	**First Design-In Experiences of Xilinx's, 20 nm, Kintex UltraScale KU060 for Space Applications and 16 nm UltraScale+ RFSoC for Ground Segment (00h20')** *Presenter: Dr. BEDI, Rajan (Spacechips Ltd)* We compare and share design-in experiences of Xilinx's, 20 nm, Kintex UltraScale KU060 for space applications. This FPGA offers 726k LUTs and 32, 12.5 Gbps high-speed serial links, offering the potential to enable the next generation of real-time, high-throughput payloads. The KU060 can instantiate Xilinx's, TMR, MicroBlaze 32-bit RISC MPU for fault-tolerant applications as well as Vivado's IP Integrator to automate the creation of TMR designs. To complement the KU060, we also discuss and share design-in experiences of Xilinx's, new 16 nm UltraScale+ RFSoC device. This part integrates wideband GSPS ADCs and DACs capable of directly processing RF frequencies, offering huge potential to miniaturise the next generation of ground-segment satellite transceivers.

Session: Radiation (10:20 – 11:10)
Chair: *Mr. POIVEY, Christian (ESA)*

10:20	**Single Event Characterization of a Xilinx UltraScale+ MP-SoC FPGA (00h25')** *Presenter: Mr. LANGE, Thomas (IROC Technologies)* Due to the technology scaling, more and more complex applications can be implemented on

		configurable devices, such as the new Xilinx FPGAs and MP-SoCs. In addition, devices manufactured in new process technologies, e.g. FD-SOI and FinFet, show a much lower sensitivity to Single Event Effects than previous generation bulk processes. These aspects and their affordable cost, especially in comparison to Application Specific Integrated Circuits (ASICs), make configurable devices more attractive for space applications. The focus of our study is to evaluate the radiation sensitivity of a Xilinx Ultrascale+ ZU3EG MP-SoC FPGA. The device embeds 4 ARM A53 APU, 2 ARM R5 RPU cores and an FPGA based on the Ultrascale architecture. In order to measure the Single Event Effect (SEE) sensitivity of the device, it was tested under standard heavy-ion (at UCL), ultra-high energy heavy-ion (at the H8 beam line, extracted from SPS, CERN) and high-energy electrons irradiation (at VESPER, CERN) and will be tested further under high energy protons (at PSI) and low energy protons irradiation (at RADEF). Therefore, a custom test board has been designed which allows the measurement of the SEE cross-sections. Single Event Latch-UPs (SELs) are detected by the independent current monitoring on all power domains of the device under test and the observation of sudden current increases (typically signature for SELs). Further, an FPGA test vehicle has been developed which measures the SEU cross-sections of several FPGA elements, as well as the functional failure rate of the embedded R5 processor. The Configuration RAM is monitored with the help of the Xilinx SEM-IP. The Block RAM and Distributed RAM are tested by using an external tester and standard memory test algorithms. Two different shift register chains are used to evaluate the FPGA Flip-Flops SEU rates in normal and TMR configuration. In this presentation, we will describe the implemented test setup, give an overview of the used test facilities and show SEE sensitivity measured during the campaigns.
	10:45	**Ultra-High Energy Heavy Ions radiation tests on COTS FPGAs at CERN: results for Microsemi ProASIC3 and Xilinx Zynq all-programmable SoC (00h25')** *Presenter: Dr. TAVOULARIS, Antonios (European Space Agency)* The higher performance requirements of the upcoming space missions and the availability of highly integrated processing solutions, such as the Xilinx all-programmable SoC, calls for an increase in the use of COTS devices and software-defined applications. SEE characterization of these devices is at the same time a necessity and a challenge, because they present difficulties that are either not fully addressed by current testing guidelines, or may result in expensive, cumbersome test configurations. Thanks to a cooperation agreement between CERN and ESA, certain ESA projects were offered beam time from the most intense beam of ultra-high energy ions available at the Super Proton Synchrotron (SPS) particle accelerator. We present hereby the results of several radiation tests performed under the aforementioned beam on two different devices: COTS Flash FPGA from Microsemi (AP3000L-1PQG208 ProASIC3) programmed with a rad-hard soft controller; and a COTS all-programmable SoC from Xilinx (Zynq 7020) that embeds an SRAM FPGA (XC7020-CLG484) and two ARM Cortex9 processors, hosted on a Zedboard. In order to test the Microsemi ProASIC3, the PicoSkyFT soft-core, integrated into a SoC configuration with peripherals, is used for characterization. The PicoSkyFT SoC netlist is additionally hardened by a proprietary tool, which automatically applies TMR with selectable levels of triplication. A custom single-threaded firmware is used for testing, with emulated operations such as data shuffling, arithmetic operations and operations with peripheral units, sequenced in an infinite loop. The PicoSkyFT is able to differentiate between recoverable and non-recoverable EDAC errors, invalid and privileged instructions, invalid access program and data memory, invalid register file parity faults. For testing the Xilinx Zynq, two boards are used with different applications. The first one consists of a basic design that reports results from the Coremark software running in the ARM processor. Additionally, a script is used to periodically readback the configuration memory and count the configuration errors. The second mechanism focused on evaluation the programmable logic of the Zynq, by means of a high-performance VHDL benchmark based on FIR modules of varying size. This VHDL design involves parallel architectures with parametrizable number of filter taps, which can be combined to create big implementations, covering and monitoring the majority of the configurable logic blocks (CLBs). This benchmark allows for the localization of the SEE occurring by the ion hit. The processing system on the Zynq controls the filters operation and detects the errors. SEFI occurrence and SEE cross-section is extracted for both the ProASIC3 and the Zynq, contributing to demonstrate that heavy Ion irradiation with CERN's SPS Ultra High Energy source could represent in the future a viable solution for screening of components to be used in space applications.

Networking Coffee Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division (11:10 – 11:40)

Session: FPGA Vendors (11:40 – 12:40)
Chair: *Mr. FERNANDEZ-LEON, Agustin (ESA)*

11:40	**Microsemi RTG4 Radiation Tolerant FPGAs: Radiation and Qualification Update (01h00')** *Presenter: Mr. O'NEILL, Ken (Microsemi)* In this presentation we will provide the latest updates on radiation testing and qualification status of Microsemi's RTG4 FPGAs. We will also cover updates on packaging technology and screening flows. A quick overview of updates relating to Microsemi mixed signal standard products for space applications will also be provided, as these products are frequently used in conjunction with FPGAs to provide services such as telemetry acquisition and motor control.

Session: Reconfiguration (12:40 – 13:00)
Chair: *Mr. ODOUNDE, Aurelien (CNES)*

12:40	**Modern On-Board-Processing based on FPGAs for Flexible Satellite Communication (00h20')** *Presenter: Mr. RITTNER, Florian (Friedrich-Alexander-Universität Erlangen-Nürnberg)* Flexible satellite payloads are important for the use cases of modern satellite constellations. A reconfigurable On- Board- Processor (OBP) based on Field-Programmable Gate Array (FPGA) technology provides the needed flexibility and enables adaptable signal filtering, regeneration, and switching / routing by reconfiguration of the digital signal processing chain. Additionally, new powerful FPGAs reinforce the possibilities for future application. This presentation shows some details of an OBP design process with the example of the Fraunhofer OBP (FOBP), which is based on two radiation hardened FPGAs. The FOBP has a fully qualified Engineering Qualification Model (EQM) and shall be launched to a GEO within the Heinrich-Hertz satellite mission in 2021. Starting with the application field of satellite communications, the presentation introduces the system design, including requirement engineering. Afterwards, details of the top down design flow are given by elaborating the hardware, firmware (FPGA design), and the software. The presented FOBP provides a dependable, powerful, reconfigurable, and scalable processing platform for on-board processing. A live demonstration shows the FOBP in-band telemetry and telecommand capabilities. Focus of the presentation are the FPGAs of the FOBP together with the key aspects of hardware, firmware, and software design. This enables an outlook to possible applications and future FPGA-based OBP systems and demonstrates the demand as well as the high potential of FPGA-based OBPs.

Networking Luncheon (13:00 – 14:00)

Session: Reconfiguration (14:00 – 15:40)
Chair: *Mr. ODOUNDE, Aurelien (CNES)*

14:00	**FPGA Based Multithreading for On-Board Processing (00h20')** *Presenters: Mr. LOMBARDI, Pasquale (Syderal), Mr. GUERRIERI, Andrea (EPFL), Mr. BELHADJ, Bilel (Syderal)* FPGA (Field Programmable Gate Array) is an attractive technology for high speed data processing in space missions due to its unbeatable flexibility and best performance to power ratio, in comparison to software. However FPGAs suffer from two major drawbacks. First, higher programming effort is required with respect to software and, second, hardware resources need to be allocated for each implemented function in contrast to software functions which can be executed on the same processing hardware. This presentation describes the results of a demonstrator design activity about a reconfigurable platform based on a ZYNQ FPGA. The achieved objective of this activity is to show that modern FPGAs can be exploited as computing resources like any other processing platform and are suitable for data processing applications

		without being subjected to the above mentioned drawbacks. Exploiting partial dynamic reconfiguration, we have split the FPGA in different regions, each able to configure a different accelerator concurrently and independently from each other. Then, in the same way as software based multiprogrammed and multithreaded systems can dynamically create, schedule and synchronize threads, we have implemented equivalent abstraction mechanisms to create, schedule and synchronize FPGA based hardware threads. In our system, in analogy to classic processor based computing platforms where multiple software threads run in parallel on different cores, abstraction mechanisms allow a software program to run multiple hardware threads in parallel on different FPGA partitions, while not requiring additional programming effort. As a proof of concept test, we have processed Sentinel-2 Multi Spectral Imager (MSI) Level-1C data available in the Copernicus Open Access Hub to generate Level-2A scene classification map. On the same computational platform, we have achieved 40 times acceleration factor and more than 10 times better energy efficiency when using software controlled FPGA threading in place of full software implementation. The design is fully portable and can be mapped onto other FPGAs integrating partial reconfiguration technology. This activity has been carried out as a joint collaboration between EPFL LAP and Syderal in the frame of the SWIFT (SoftWare Initiated FPGA Threading) project, funded by the Swiss State of Secretariat for Education Research and Innovation (SERI) within the Positioning Measures initiative implemented by the Swiss Space Center.
	14:20	**Satellite Failure Management System by partial reconfiguration FPGA (00h20')** *Presenter: Dr. IBRAHIM, Mohamed (National Authority for Remote Sensing and Space Sciences, NARSS)* Satellite Failure Management System (FMS), is the core part responsible for handling, configuring and recovering the failures in satellite subsystems in the emergency mode. The main advantage of using FPGAs in developing the FMS is manifested in its programming flexibility and ability to implement fault tolerant techniques such as hardware Triple Modular Redundancies (TMR) and software roll-back and check-pointing techniques. The use of FPGAs would increase the overall satellite reliability when mitigated probably. The overall satellite system efficiency and effectiveness would be enhanced when compared with the current small satellite architectures which depend on discrete components. The Satellite Failure Management system (FMS) is apportioned into three main techniques, failure detection, isolation and recovery techniques (FDIR). They are all related under the integrated diagnostics concept. In this paper, we propose an approach of using FPGAs to develop the FMS detection module. In case of detecting any design failures in the FMS through telemetry data bus, the FPGA would be remotely reconfigured through the ground station. This remote reconfiguration feature would enable the implementation of evolutionary hardware on-board future small satellites. In another futures in the detection modules, can be detect an up-normal possession operation by specified upper layer signature process.
	14:40	**Controlling Concurrent Change in Aerospace Electronics (00h20')** *Presenter: Dr. FIETHE, Björn (IDA TU Braunschweig)* Space missions have to handle very high data rates due to increased spatial, radiometric and time resolutions of payload instruments already now. To be able to handle this amount of data, final physical values have to be extracted in real time by an autonomous, intelligent and reliable application already on board the spacecraft, adapting itself to the changing needs in a controlled environment. The DFG Research Group FOR 1800 ”Controlling Concurrent Change (CCC)” develops methods and architectures for embedded system platforms supporting concurrent change of applications and platform under the high requirements to real-time, safety, availability, and security. Within this group we demonstrate and evaluate the usability and capabilities of the CCC approach under the safety, reliability and availability requirements of a typical space application. This includes maximizing the use of resource limited HW/SW platforms in a multi-functional and adaptable manner. The ability of SRAM-based FPGAs to support Dynamic Partial Reconfiguration (DPR) allows a very flexible use of the available HW platform in a Time-Space Partitioning (TSP) manner within the very tight constraints of scientific space missions, even for complex algorithms. The main emphasis is given to the validation of the CCC approach onto a distributed computing platform under a typical space exploration scenario (e.g. planetary surface exploration), which includes real-time and high criticality demands, i.e. optimization has to be performed during runtime onboard. To achieve this, the demonstrator robotic platform DORIS (Demonstrator Of

		Reconfigurable Integrated Systems) has been equipped with dedicated data sources (cameras), actuators and System on Chip (SoC) processing platforms including reconfigurable HW and SW capabilities, based on ARM technology. This was also driven by the availability of rad-hard ARM-based processors for the extreme space environment, e.g. soft core in FPGAs or future NanoXplore NG large FPGA. Tightly coupled ARM-FPGA systems, e.g. Xilinx Zynq SoC, benefit from high bandwidth interfaces between hard-wired processor cores and the FPGA fabric. The Genode OS targets safety-critical applications because it enforces a strong isolation between software components. For that reason, it has been decided to use Genode OS in the CCC project. To use the DPR feature of modern FPGAs also within Genode OS, we have made it available for Genode OS running on a hybrid CPU-FPGA SoC device. A framework has been developed to dispatch tasks from software and execute them hardwareaccelerated in the FPGA fabric of the SoC. This extends the utilization of DPR to mixed-critical systems. Additionally, a newly proposed scheduling algorithm optimizes for the objectives latency/throughput and power/energy. Furthermore, we will demonstrate the usability and capabilities of the CCC approach for evaluating the error resilience of the complete system and reduction of failure rates, also for SEU mitigation. With an appropriate model, we want to calculate the reliability from a given functional graph.
	15:00	**Overlay Architectures for Space Applications (00h20')** *Presenter: Dr. SOUSA, Jose (IPbloq)* If a reconfigurable architecture is synthesized on commercial of the shelf (COTS) FPGAs it is called an overlay architecture. Overlays are portable, allows the user to abstract from the FPGA resources used, and is orders of magnitude faster to configure compared to FPGAs. In this communication we present an overlay architecture consisting of one or more RISC-V CPUs and one or more IPBloq Coarse Grained Reconfigurable Arrays (CGRAs). This architecture is designed so that it can be mapped to different FPGA sizes by using a variable number of tiled CPU/CGRA components. It targets applications that require both intensive control and data processing. The control part is implemented by the CPUs while the intense data processing algorithms run on the CGRAs. Since this architecture is implemented in an FPGA, it allows different types of parallelism: instruction, data and thread level. The ultimate goal is to achieve maximum performance at minimum energy footprint, while using as small a number of FPGAs as possible. This kind of architecture is highly suitable for space applications. First of all, applications can be developed using the C programming language, which speeds development and facilitates the intervention of domain experts who need to have no knowledge about hardware description languages and FPGA synthesis, place and route. Second, the adoption of an open source ISA such as the RISC-V ISA facilitates the access to CPU technology , which otherwise is fenced by IP rights, making it difficult for SMEs to make valuable contributions in this area. Third and last, by flexibly accelerating compute intensive tasks on IPbloq CGRAs, it is possible to map very large hardware datapaths on small size FPGAs, by partitioning the datapath into small portions that can be sequentiality mapped to the CGRA with very rapid reconfigurations. Moreover, the fast reconfiguration capability makes the present architecture ideal for fault tolerance, by being able to migrate applications between nodes. Besides presenting the architecture and programming tool, implementation results for two representative algorithms, FFT and K-means clustering will be presented.

Session: FPGAs: High Performance (15:20 – 16:20)
Chair: *Ms. SANTOS, Lucana (ESA)*

	15:20	**Review and comparison of design methodologies and hardware implementations on FPGA technologies. Case study: CCSDS compression algorithms for multispectral and hyperspectral images (00h20')** *Presenters: Mr. BARRIOS, Yúbal (IUMA/ULPGC), Dr. SÁNCHEZ, Antonio (IUMA/ULPGC)* Reprogrammable Field Programmable Gate Arrays (FPGAs) for space applications, are becoming steadily more common in space applications due to their high flexibility to change dynamically the functionality of the on-board system, combined with high performance and low power consumption. SRAM-based FPGAs) are vulnerable to radiation, which can cause bit flips in the configuration memory, resulting in a malfunction of the system or a functional interrupt. Nevertheless, currently several techniques may be implemented to prevent or mitigate the impact of a SEE, such as scrubbing to inspect the configuration memory or Triple-Module

		Redundancy (TMR) schemes in the logic fabric to preserve the data integrity. Moreover, the FPGA design methodology has been evolving in the last years, addressing the complexity of the hardware architecture in a higher level of abstraction than RTL traditional models. This design methodology, named High-Level Synthesis (HLS), allows generating a compliant hardware description from a reference software code (for example written in C/C++), with few modifications oriented to a hardware-friendly implementation. This constitutes a new design flow, which may potentially reduce the Time-To-Market (TTM) with respect to the traditional RTL design, taking advantage of both reconfigurability and early prototyping. However, the effectiveness of the hardware implementations by means of HLS tools has still to be assessed. This work presents a comparative study of different hardware implementation approaches using different design flows and target FPGA technologies. As target applications to conduct the study, two lossless data compression standards developed by the CCSDS (Consultative Committee for Space Data Systems) have been chosen. These standards are intended for space applications, and therefore they have been designed with the aim of providing a good trade-off between compression efficiency and computational complexity. Among them, the CCSDS-121 standard compresses of raw uni-dimensional data, while the CCSDS-123 has been specifically designed for multispectral and hyperspectral images. In addition to the two lossless standard, a proposed extension of the CCSDS-123 standard for lossy compression has been also used as additional case study. A comparative study is conducted among hardware implementations of the CCSDS-121 and CCSDS-123 compression standards on several FPGA technologies (Microsemi RTAX and RTG4, Xilinx Virtex and ZynQ families), following both RTL and HLS design methodologies (CatapultC and Vivado HLS). The work is complemented with the implementation results of the CCSDS-121 standard over the space-grade BRAVE NG-MEDIUM FPGA, the first medium-capacity, high-performance and radiation-hardened re-programmable European FPGA. The results of this work have been obtained in different national and European projects in which the research group is present, such as TRP-AO8032, part of the ESA program, the European funded project ENABLE-S3, or the Spanish funded project REBECCA.
	15:40	**Image compression on reconfigurable FPGA for the SO/PHI space instrument (00h20')** *Presenter: Mr. HERNANDEZ EXPOSITO, David (Instituto de Astrofísica de Andalucía - CSIC)* In this work we present a novel FPGA implementation of the Image Data Compression standard proposed by the Consultative Committee for Space Data Systems (CCSDS-IDC 122.0-B) aboard the Polarimetric Helioseismic Imager instrument of the ESA's Solar Orbiter mission (SO/PHI). The SO/PHI telemetry constraints enforce the use of specific strategies for on-board data reduction, analysis, and compression. In this context, our CCSDS-IDC compressor is aimed at processing images of different sizes, performing lossless compression of at least a factor two during nominal operation modes, and lossy compression with several compression factors in other specific modes. The proposed CCSDS-IDC implementation is in-flight reconfigured within one of the two Virtex-4 QPro-VSX55 FPGA devices included in the SO/PHI Digital Processing Unit. The embedded architecture consists of two functional blocks, namely, the Discrete Wavelet Transform (DWT) and the Bit Plane Encoder (BPE) cores. The DWT core is accelerated by means of a light multi-processor architecture combined with a smart structure of buffers. On the other side, the BPE core is carefully pipelined to perform one pixel per clock cycle. This architecture performs lossless and lossy compression of 2048 x 2048 images with full dynamic range of 16 bit/pixel in less than 3 seconds, which implies a factor 30 acceleration with respect to a LEON-3FT processor. The final implementation uses around 50% of FPGA logic and 65% of block-RAM memory elements in contrast to other hardware implementations that use larger FPGA devices or external memory resources. To our knowledge, it is the first in-flight reconfigurable FPGA implementation of a CCSDS-IDC-compliant algorithm for an ESA mission, which introduces important improvements regarding time and use of resources.
	16:00	**Implementation of Visual Based Navigation in a CPU-FPGA architecture for planetary landing (00h20')** *Presenter: Mr. OLIVEIRA, Joao (Spin.Works)* The work presented in this article is the product of an activity with the objective of further develop and flight test visual based navigation (VBN) and hazard detection and avoidance

		(HDA) algorithms to serve the needs of future Mars and other planetary missions and raise them to a technology readiness level (TRL) of 5 (“critical function verification in a relevant environment”). The Zynq-7020 SoC was selected as the hardware platform for development. Being a dual-core architecture, one CPU was fully dedicated to the VBN, enabling the development of a fast and efficient software design, whilst leaving the second CPU dedicated to flight and mission control systems. The co-processing FPGA was programmed to handle both the required on-board sensor interfaces and the processing IP blocks that compose the VBN hardware accelerators. This work presents the performance results comparing the CPU-only version of VBN with the CPU+FPGA approach, taking into account a target frame rate of 10Hz. Performance is measured not only in terms of processing speed, but also in terms of algorithm performance degradation and impact on the navigation accuracy.

Networking Coffee Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division (16:20 – 16:50)

Session: FPGAs: High Performance (16:50 – 17:10)
Chair: *Ms. SANTOS, Lucana (ESA)*

	16:50	**Implementation of a GNSS Space Receiver on a Zynq (00h20')** *Presenter: Mr. MAJORAL, Marc (CTTC)* Currently the Agency is using space-qualified GNSS receivers based on ASIC solutions (in particular, the AGGA-family) integrated in ad-hoc instruments (receivers). Such receivers provide outstanding measurement quality required for POD (Precise Orbit Determination) performed on ground, but at the cost of high price and power consumption. In order to address the needs of low cost missions (eg: cubesats, microsat) there is a need for reducing the cost of space GNSS receivers. There is a need as well to have a higher configurability and flexibility to adapt or update, in a straightforward way, the GNSS space receiver to new missions, applications, platforms and, eventually, future GNSS signals. GNSS software-defined space receivers running on consumer based powerful SoC (System on Chip) could represent a viable alternative to ASIC based solutions. Recent studies and roadmaps show that these chips can be used in space. GNSS signal processing is a heavy task, particularly for high speed correlation functions and (optional) digital filtering at baseband. SoC merging both FPGA and microprocessors (ARM) allow the implementation of high demanding correlation tasks in FPGA, while the remaining part of the processing can be done in the microprocessor. The focus of our activity is the implementation of a GNSS Space Receiver using a Xilinx Zynq 7000 SoC. The Zynq 7000 contains a dual-core Cortex-A9 processor mated with an Artix-7 based programmable logic. The GNSS Space Receiver is based on the open source GNSS-SDR software-defined receiver. The GNSS-SDR takes care of all the digital signal processing, performing signal acquisition and tracking of the available satellite signals, decoding the navigation message and computing the observables needed by positioning algorithms, which ultimately compute the navigation solution. The software is designed to facilitate the inclusion of new signal processing techniques, offering an easy way to measure their impact in the overall receiver performance The ARM cores run the GNSS-SDR software-defined receiver. In order to run the GNSS-SDR software on real time, some functions are implemented in the FPGA part of the SoC (the Programming Logic). These functions are implemented as hardware accelerators that implement the most computationally intensive operations of the GNSS receiver. The hardware accelerator modules are implemented in the form of FPGA IP cores. The importance of FPGA IPs has grown over the years. They ease the reusability and the integration of the VHDL modules and they are a common way of distributing VHDL modules. The hardware accelerators are implemented as IPs that use the IP-XACT specification, which is widely used for packaging, integrating and reusing IP within design tool flows. In this work we present a description of the GNSS Space receiver and how it is implemented in the Zynq SoC.

Session: Industrial Experiences (17:10 – 17:30)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

17:10	**A Comparison of 65 nm Space-Grade and COTS FPGAs : RTG4 vs. V5QV vs. NG-MEDIUM vs. NG-LARGE vs. IGLOO2 vs. SmartFusion2 (00h20')** *Presenter: Dr. BEDI, Rajan (Spacechips Ltd)* We compare IP implementation and share design-in experiences of six 65 nm ultra deep-submicron, space-grade and COTS FPGAs: RTG4, V5QV, NG-MEDIUM, NG-LARGE, IGLOO2 and SmartFusion2. Two versions of the RTG4 flash FPGA containing the same rad-hard die are available to the space industry: a 1657 CCGA/CLGA device and a 352-pin CQFP part with less (166 vs. 720) I/O and fewer (4 vs. 24) high-speed serial links. Both contain 151,825 logic elements containing a TMR flip-flop and an SET filter, and their memory supports SECDED EDAC with logically-adjacent storage bits interleaved in the physical layout to protect against multiple-bit upsets. Simulations have shown that the power consumption of both RTG4 parts is almost identical as I/O dissipation is negligible and its overall proportion decreases as a function of logic utilisation. Flash FPGAs are non-volatile, do not require external boot memory and their configuration is immune to radiation effects. The V5QV, NG-MEDIUM and NG-LARGE are rad-hard SRAM-based FPGAs containing 131k, 35k and 140k LUTs respectively. Each contain twelve-transistor configuration memory cells to protect your intended functionality against radiation effects as well as other circuit, architectural and layout-level hardening to improve overall reliability. IGLOO2 and SmartFusion2 are 65 nm, flash-based COTS FPGAs whose configuration is immune to radiation effects and contain some hardened fabric logic. NG-MEDIUM and NG-LARGE are new, European, ITAR/EAR-free, rad-hard FPGAs offering on-board processing opportunities for markets with export concerns. Our design-in and comparison of 65nm FPGAs reveals insightful discoveries to help traditional and NewSpace companies design right-first-time, digital, space sub-systems.

Round Table and Wrap up (17:30 - 18:30)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

SEFUW Dinner (18:45 – 21:00)
ESTEC Restaurant

Wednesday 11 March 2018

SEFUW Intro – Opening Remarks (08:50 - 09:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: FPGA Vendors (09:00 – 10:00)
Chair: *Mr. DANGLA, David (CNES)*

09:00	**From eFPGA cores to RHBD SoC FPGA (01h00')** *Presenter: Mr. LE MAUFF, Joel (NanoXplore)* NanoXplore is a privately owned fabless company based in France, created by veterans of semiconductor industry with roughly 30 years experience in the design, test and debugging of e-FPGA cores. Thanks to that background, NX has been awarded a contract by European Space Agencies, ESA and CNES, to develop and to industrialize Radiation Hardened Sram-based FPGA devices under both ESCC and DLA quality standards in order to increase the FPGA offer. The 1st part of the presentation will start fixing the Space FPGA market size and will explain why NanoXplore is a credible solution for the Space sector. Next we will present Strategical choices in term of technology nodes, supply-chain as well as design approaches. Especially, we will address RHBD (Radiation Hardening By Design) approach targeting the lowest Soft-Error rate in order NX RH Sram-based FPGA devices becoming suitable for Critical Spaceborne applications. The 2nd part of the presentation will cover the NX product roadmap. We will first address the Low-End FPGA named NG-Medium introduced on the Space market for months, addressing features vs competition, packaging and QA level solutions vs ECSS classes as well as for sure Radiation performances and Qualification planning. Next, we will switch to the Mid-End FPGA product named NG-Large which will offer Europe a competitive solution against most complex RH FPGA devices present on the market. Last but not least, we will open the future with our High-End SoC FPGA which will become the 1st RH 28nm FPGA device, offering World-Wide customers a Flight-Model solution for Spaceborne applications validated at Breadboard level with XILINX & INTEL PSG COTS solutions. Last, we will conclude and open the Questions & Answers session.

Session: Design Flow (10:00 – 11:10)
Chair: *Mr. DANGLA, David (CNES)*

10:00	**QUEENS-FPGA: Quality Evaluation of European New SW for the BRAVE FPGA (00h25')** *Presenter: Mr. GONZALEZ-ARJONA, David (GMV Aerospace and Defence)* GMV is the prime contractor of QUEENS-FPGA project which stands for “QUality Evaluation of European New SW for brave FPGA”. The BRAVE project supported by ESA and CNES provided very promising European SRAM-based FPGAs for Space, a good roadmap that will allow Europe to avoid restrictions on access to non-European technologies and FPGAs. GMV will present the preliminary conclusions of NG-MEDIUM development environment utilisation based on the experience gained and the results obtained from the use of the NanoXplore tools following the methodology proposed under ESA-founded QUEENS-FPGA in the starting phase of the projetc. The project follows a methodological evaluation. NanoXplore is part of the team solving some bugs found, guiding on the proper use of the tools and implementing suggestions found by the alpha/beta users in the consortium. These users are GMV and NTUA. The synthesis, place&route, bitstream and HW assessment report is obtained by the implementation of a subset of circuits divided into different complexity and challenging benchmark circuits (simple basic structures, interfaces and medium-complex circuits, high-complex designs) besides the porting of existing real space-oriented implementation algorithm by GMV. Comparison of BRAVE FPGA development is performed with respect to other FPGAs consolidated in the space and commercial industry. We used NanoXplore tools following a comparison methodology proposed in the project. Due to the lack of standard benchmarks to assess performance capabilities of FPGA development environments, we proposed a quality assessment methodology based on analysis and comparison of measurable characteristics (metrics) among different FPGA frameworks using equivalent devices in terms of logic resources, performance, technology and radiation-hardness.

	10:25	**High-Performance Benchmarking of the European NG-MEDIUM FPGA (00h25')** *Presenter: Dr. LENTARIS, George (National Technical University of Athens, Greece)* “Quality Evaluation of European New SW for the BRAVE FPGA” (QUEENS-FPGA) is an ongoing ESA activity for the assessment and improvement of the programming tools of the new rad-hard NG-MEDIUM FPGA. Given BRAVE's primary target, i.e., high-performance applications, it becomes imperative to test the tool and device with computationally demanding benchmarks suitable for space missions, such as digital signal and image processing. Therefore, during the past year, an important part of QUEENS' beta testing is devoted to this task. In the current presentation, we give an overview of the procedure followed and some preliminary results. We focus on the evaluation of NanoXmap with respect to Synthesis, Placement, and Routing, when using VHDL algorithms inherited from real Vision-Based Navigation activities. Specifically, we assume FIR filtering, stereo correspondence, and feature extraction algorithms developed for accelerating rover localization and mapping. We follow a methodology to select and tune the benchmarks to fit in the NG-MEDIUM FPGA, while we assess the effectiveness of the tools in each step of the implementation process. Overall, we derive promising results with respect to the possible use of BRAVE in future space missions. Moreover, by stressing the tool with our high-performance benchmarks, QUEENS has already provided useful feedback and contributed in advancing the NanoXmap tool from user perspective.
	10:50	**An ECSS-Q-ST-60-02C compliant verification flow for scientific projects (00h20')** *Presenter: Mr. DARMETKO, Marcin (Centrum Badan Kosmicznych PAN (Space Research Centre))* Verification of a space project is a complex and time-consuming task due to requirements for high reliability and extensive documentation. Unexpected changes to design are likely to happen in scientific projects, often forcing the whole process to be repeated. Because of these reasons, automation is highly desirable in space FPGA development. The aim of the presentation is to show that automation of verification process can be worthwhile and cost-effective to implement even for small teams. It will include examples of solutions created and successfully used by the Space Research Centre team during development of STIX instrument for Solar Orbiter mission. Presentation describes the flow from requirements definition, through simulation and tests, up to documentation of results. The talk goes into the details of used software, including those created in-house. Lessons learned from the verification process will also be shown. The presented approach was created to be in compliance with ECSS-Q-ST-60-02C, although it can be adapted to other standards.

Networking Coffee Break sponsored by CNES CCT and ESA's Data Systems and Microelectronics Division (11:10 – 11:40)

Session: Fault Tolerance Methodologies and Tools (11:40 – 13:00)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	11:40	**Permanent Fault Handling in SRAM-based FPGAs (00h20')** *Presenter: Mr. RITTNER, Florian (Friedrich-Alexander-Universität Erlangen-Nürnberg)* Permanent faults are a critical issue when using SRAM-based FPGAs in space applications. Compared to temporary effects such as Single-Event Upsets (SEUs), a system reboot by performing an FPGA reset or a power cycle does not recover these faults. Usually, the occurrence of permanent faults has a low probability but is highly critical as it might lead to a system outage. In harsh environments, like space, a physical access to the FPGA is not possible, which restricts a repair or debugging possibility. To overcome permanent faults and such possible system outage, we introduce a concept for permanent fault handling based on Wireless Remote Debugging (WRD) via a RF link. The major benefit is to ensure a continuous FPGA operation for the mission life time. The fault sources when using FPGAs in space applications are radiation, thermal stress, mechanical stress, and aging effects. Radiation is the dominating share and in SRAM-based FPGAs mainly consisted by Single-Event Latch-up (SEL) and Total Ionizing Dose (TID). However, a permanent fault only becomes critical in the case of visibility, whereby we do not classify between the different fault sources as the lead to a same behavior. Our proposed

		concept is based on the Fault Detection, Isolation, and Recovery (FDIR) approach, which is consists of a coarse fault detection, for example with an Built-In Self-Test (BIST) design for all FPGA primitives, a fine-grain fault isolation for the defective primitive type, and at least a exclusion strategy with the fault recovery. The communication with the FPGA requires a WRD possibility. Automated test procedures support the FDIR process by automated execution of the test process or also isolation and recovery cycles. IT also minimizes the user interaction. For the test process itself, different primitive test concepts from the state of the art can be used. To consider user preferences and basic conditions, we developed an evaluation concept, which can be parameterized by the user and results in a score indicator. We show that permanent fault handling can increase the reliability of FPGA-based system as they are fully functional after a permanent fault affects the FPGA. Different tools were implemented to reduce the user interaction. Our evaluation concept is able to find the best solution for a given application. Generally, two main application fields are conceivable. First, systems with high overall costs and low fault probabilities (e.g. a longterm GEO mission) demand such permanent fault handling to ensure a high reliability. Systems with low costs but a high fault probability form the second application field (e.g. a CubeSat). Here, our approach is used for cyclic tests and repairs. Other application fields are covered by state of the art solutions, for example a radiation-hardened device.
	12:00	**Fuzzy-logic simulation based approach to modelling of fault propagation in FPGAs. (00h20')** *Presenter: Mr. CICHOCKI, Andrzej (Centrum Badan Kosmicznych PAN)* Safety-critical digital applications often require calculating the probability of system failure. Existing tools for verification of FPGA-based designs in terms of susceptibility to SEUs/SETs base mainly on fault injection methods, that require numerous runs in order to get proper statistics and are not exhaustive. Run-time of post P&R simulations may significantly limit complexity of analysed designs (like SST), while hardware accelerated fault-injection needs specialized hardware (FTUNSHADES). On the other hand, formal verification methods can only evaluate subsets (InFault or Questa Formal) of implemented fault mitigation techniques (eg. hardware & information redundancy only). The talk proposes a new combined approach of a "formal simulation" in fuzzy-logic domain, that can be especially helpful to determine probability of specific failures and covers all forms of redundancy (eg. oversampling, scrubbing). It maybe also used to find weak points (most fault contributive) in the design and compare different mitigation techniques. The method has been implemented as a software that takes post-synthesis netlist as an input (ProASIC3) which can be accompanied with a stimulus. Preliminary results of execution for simple designs with fault mitigation implemented are to be presented.
	12:20	**Reprogrammable Flash-based FPGA on EUCLID mission (00h20')** *Presenters: Prof. STERPONE, Luca (Politecnico di Torino), Dr. GRIMOLDI, Raoul (OHB ITALIA)* EUCLID is a cosmology mission part of Cosmic Vision 2015 – 2025 whose prime objective is to study the geometry and the nature of the dark Universe (dark matter and dark energy). The goal of the mission is to investigate the distance-redshift relationship and the evolution of the cosmic structures by measuring shapes and redshifts of distant galaxies. EUCLID space segment will be a space craft placed into an orbit of around L2 with a coverage of 15,000 deg2 in 6.25 years with step and stare observation strategy. Launch is planned for 2020. EUCLID spacecraft will host two instruments: NISP (Near Infrared Spectrometer Photometer) and VIS (VISble imager). CGS is in charge of the design of the Data Processing Units HW for both NISP and VIS as part of the Italian contribution to EUCLID mission in collaboration with EUCLID Italian Science Team. Both units make large use of functions implemented in FPGA devices. In particular, the DPU/DCU single unit adopt RTAX and RT3PE Flash-based FPGAs. In this presentation, we will provide an overview of the design features and characteristics on commercial flash-based technology. Besides, in conjunction with Politecnico di Torino, we will present the radiation hardening strategies adopted and evaluated as well as the radiation aware placement and guard gates introduction insertion.
	12:40	**Advancement on the Analysis and Mitigation of SETs on Flash-based FPGAs (00h20')** *Presenter: Dr. AZIMI, Sarah (Politecnico di Torino)* When particles hit a sensitive region of the ICs, it can lead to the voltage glitch, i.e. Single Event Transient (SET). Flash-based FPGAs are attracting more and more interests due to the

		immunity of their configuration memory against Single Event Upset (SEU). Flash-based FPGA technologies such as ProASIC3 as the golden core of several space mission project and RTG4 as the newest technology provided by Micro Chip / Microsemi are the focus of our recent research. We dedicated our study to fully characterizing of SET phenomena, identification of SET propagation scenario and its relative Propagation Induced Pulse Broadening (PIPB) effect on circuits implemented on Flash-based FPGAs. In this work, we investigated SET propagation considering the Convergence-SET. This phenomenon happens when SET pulses propagated through several paths overlaps and join together at a convergence point and worsen the sensitivity of logics in the output cone. Taking to account a typical RISC processor with 1,401 Versatile and 1,156 FF which works at frequency of 42MHz, based on our developed analysis environment for typical SET pulses lower than 1ns, 19.6% of injected SETs has been broadened while reaching to the FF. On the other hand, 4% of the injected SETs creates C-SET phenomena. Considering these analyses, we propose a mitigation solution based on charge sharing gates insertion into the circuit netlist which is able to decrease the sensitivity with respect to SET pulse propagation without any timing penalization. As a comparison between the RISC Microprocessor mitigated with typical TMR and Guard-Gate techniques and our proposed charge sharing method, timing and area overhead of 18% and 31% for TMR & GG and 0 and 27% for our proposed method has been reported while using our method shows the reduction of 19.6% regarding Wrong functionality of the circuit.

Networking Luncheon (13:00 – 14:00)

Session: Industrial Experiences (14:00 – 16:00)
Chair: *Mrs. MORANTI, Silvia (ESA)*

	14:00	**Using Open-source Spacewire and RMAP IPs in the PLATO Router and Data compressor Unit (RDCU) (00h20')** *Presenter: Dr. TONFAT, Jorge (Space Research Institute / Austrian Academy of Sciences)* In this work, it is presented how both IPs were adapted and functionally verified for the PLAnetary Transits and Oscillations of stars (PLATO) RDCU. The PLATO mission goal is to detect terrestrial exoplanets around bright solar-type stars and characterize them to determine their habitability. The PLATO instrument is based on a multi-telescope concept. The RDCU is part of the Instrument Control Unit (ICU) in charge of processing and compressing the digital data from the cameras. The data network is based on the Spacewire standard using Spacewire router chips. The IPs presented in this work are used for communication of the hardware data compressor with the Spacewire data network. The IP modifications include using a reliable clock recovery feature for the incoming Spacewire stream, adapting the IP to establish a link at 100 Mbps using a system clock of 25 MHz and improving the packet processing performance of the RMAP Target IP. In addition, it will be presented the modification of an open source RMAP Target IP to meet the project requirements. The functional verification of both IPs were performed using only VHDL. In addition, the Open Source VHDL Verification Methodology (OSVVM) and a testbench framework called VHUNIT were used. VHUNIT is an in-house development inspired by the software unit testing methodology. For the functional coverage computation, the Spacewire and RMAP ECSS standards are used as main reference. Both IPs were implemented and tested using the PROASIC3E Starter kit development board.
	14:20	**Virtex5QV - Device & High Speed Interfaces Feedbacks (00h20')** *Presenter: Mr. LAMONACA, DANILO (Thales Alenia Space Italy)* The electronic systems are becoming more and more complex and in need of new high performance programmable logic devices, with an increased number of internal resources and high speed interfaces. In TAS-I the Xilinx Virtex5QV device is going to be used on a flight unit and this presentation aims to share with the FPGA space community our experience on two specific aspects : (1) A short overview of the Xilinx Virtex5QV device, focusing from the high speed interfaces configurability (Rocket I/O and DDR2 I/F), on to the analysis of the performances and the results

		obtained by some dedicated board tests. (2) A brief user guideline approach regarding the prototyping on the equivalent commercial device.
	14:40	**Use of FPGAs in a scientific instrument development process: processing, testbenchs, simulators (00h20')** *Presenter: Mr. RAMBAUD, Damien (IRAP CNRS)* I will present the use of FPGA in the different parts of the SVOM/Eclairs project : how they are used in the instrument itself and how we implement prototypes but also how we use them to allow scientists to do more accurate simulations of the instrument by using FPGA based instrument simulator.
	15:00	**Evaluation of a New Mass Memory Controller Architecture on Space-Grade FPGAs (00h20')** *Presenter: Mr. JIA, Lei (Institute of Computer and Network Engineering (IDA), TU Braunschweig, Braunschweig, Germany)* A novel Next Generation Mass Memory Architecture (NGMMA) has been introduced for future space application within the scope of an ESA study (Contract No. AO/1-5975/08/NL/LVH) to cope with the growing demands on very high-speed and huge data volumes of future space-borne instruments. In this context, a new memory controller architecture has been developed and evaluated, which interfaces DDR3 SDRAM-based mass memory and new high-speed SpaceFibre interface. While the first implementation was based on a commercial Xilinx Virtex-6 FPGA, evaluation of the memory controller architecture on space-grade FPGAs will be given. Typically, mass memory controller architectures are dependent heavily on applied memory technologies and space application specific user interface, which leads to a proprietary design. To improve reusability and adaptivity of the mass memory controller architecture, generic building blocks, i.e. Advanced eXtensible Interface 4 (AXI4) interconnect, have been included and a novel partition-based fault-tolerant mass memory controller architecture has been developed, the so-called Partition Controller. The Partition Controller consists of Central DMA Controller, Microblaze CPU, DDR3 Memory Interface, SpaceFibre (SpFi) Interface, SpFi Interface Controllers and some other generic IP cores. It uses Direct Memory Access (DMA) transfers, which can be split into multiple single transactions by means of a Scatter-Gather (SG) operation. Externally, it allows a block-based memory-mapped random direct access to the memory partition over an on-chip interconnect. Due to higher SEE sensitivity of DDR3 SDRAMs compared to standard SDRAMs, a double symbol error detection and correction Reed-Solomon (RS) code has been included in the DDR3 Memory Interface for mitigating SEEs. The Partition Controller was demonstrated and evaluated on a so-called Memory Partition Module. A series of space-grade FPGAs can be considered to implement the mass memory controller. This will be discussed in short in the following section. DDR3 SDRAMs are operated with a 1.5 V SSTL I/O standard, which needs to be supported by the FPGA and thus limits the FPGA options. Currently, the rad-hard Xilinx Virtex-5QV and Microsemi RTG4 FPGAs support that I/O standard and thus could be used to implement the Partition Controller. The Virtex-5QV FPGA provides many equivalent features and technologies as Virtex-6 FPGA used in the demonstrator. Furthermore, the NanoXplore BRAVE NG large and the Xilinx Kintex UltraScale XQRKU060 FPGAs will be available in the near future and can be also considered as FPGA options. Additionally, a Triple Modular Redundancy (TMR) processor solution can improve the reliability of mass memory controller.
	15:20	**Comparison between Microsemi RTG4 and Xilinx SIRF (00h20')** *Presenter: Mr. VERMERSCH, Felix (SERMA)* This talk presents a comparison of the performances between FPGAs XILINX Virtex 5QV and Microsemi RTG4 from a reference space design. It presents the modifications brought to the reference design to adapt it to the new target : the Microsemi RTG4. The problems met in this porterage owed to the differences of the technologies and a comparative degree of the performances on each of the targets of a point of view: - Used Resources, - Consummate Power - IO Timing

	15:40	**Radiation Testing and End User Validation of the BRAVE NG-Medium FPGA (00h20')** *Presenter: Mr. BERROJO, Luis (Thales Alenia Space in Spain)* TAS has been involved on the Radiation Testing and End User Validation of the BRAVE FPGA within the frame of the H2020 VEGAS project. TASE is the leader of the radiation test campaign and device characterization. Positive preliminary results indicate that the device is a good candidate for Space applications, although additional campaigns are still foreseen. For End User Validation purposes TAS has exercised, on the NanoXmap set of tools, from simple examples of VHDL code to complete FPGA designs. The main goal of the activity is analyzing the NanoXmap tool behavior throughout the different stages of a typical FPGA design flow, from VHDL capture and simulation, passing Synthesis and Place& Route stages, down to postlayout Static Timing Analysis and logic level simulation and FPGA programming. Different designs have been loaded on the Evaluation Board and functionally tested. The findings obtained from the TAS testing and evaluation activities will be presented and a user perspective to identify tool potential enhancements will be provided.

Concluding remarks and closure (16:00 - 16:30)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

SOCIAL DINNER – SEFUW 2018

A non-hosted dinner will take place on Tuesday night (April 10th) at the
"ESTEC Restaurant" at 6:45pm

Price: 50 EUR
The price includes a small plates menu served buffet-style and a drink arrangement.

MENU

Selection of Starters

* *

Selection of Main courses

* *

Dessert Buffet

Example Menu 1

Starters

Marinated Salmon
Green salad with dressing
Quinoa salad with grilled Tofu
Bread & Butter

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Main courses

Salmon with wine sauce
Grilled veal steak with mustard tarragon sauce
Tomato with Quinoa and Ratatouille
Potato cakes
Courgette and eggplant gratin

Example Menu 2

Starters

Parmaham with mozzarella and sun dried tomatoes
Vegetarian Ceasar salad
Green salad with dressing
Bread & Butter

**

Main courses

Baked seabass with prawns and lemongrass sauce
Sirloin steak
Cannelloni with Ricotta and spinach
Potato gratin
Mixed vegetables

Entrance Procedure

Please be aware that in order to gain access to the ESTEC site, each visitor will have to check in at the Security Gatehouse and **present a valid ID**. ESTEC Security will make a scan of your ID.

Access to the ESTEC site is restricted to persons registered using the online workshop registration system, and presenting an original valid form of ID.

Persons not registered will not be admitted to ESTEC by ESTEC Site Security.

In case of loss of the badge, please report to the registration desk or to the organisers immediately, as badges should be worn visibly all the time.

Emergencies

In case of any type of emergency, phone the ESTEC emergency number and provide the following information: your name, location, the nature of the emergency and casualties

The ESTEC emergency telephone number is 3333.

ESTEC Facilities

Wireless Internet
The wireless service is available in the Newton Room Area and in all meeting rooms. You can find your login details at the back of your badge.
Wireless Network Name (SSID):esa-conference

If your login details are not displayed at the back of your badge, please contact the registration desk or the organisers.

Banking
There are two ATM machines at ESTEC, one across from the Coffee Corner and another in Section Ad, where ABN AMRO Bank maintains an office.

Restaurant
ESTEC restaurant is available to visitors for the Networking Luncheon.

Space Shop
The Space shop is open Wednesday & Thursday from 13:00-14:30hrs. You can find the shop near the main entrance (between reception and restaurant).

How to get to ESTEC

By car:
ESTEC is located at the southern tip of Noordwijk.

- From Amsterdam, take the A4 in the direction Den Haag-Rotterdam, then at the junction follow the A44. Take the exit Noordwijk-Voorhout, continue to Noordwijk and from there, follow the signs 'ESA ESTEC'.
- From Den Haag (The Hague), take the A44 motorway in the direction Amsterdam/Wassenaar and exit at 'Leiden' (exit 8). Follow the N206 in the direction Katwijk and Haarlem. Take the exit 'Katwijk Noord'. From there follow the signs 'ESA ESTEC' (small white traffic signs).

By Bus:
From Leiden Central station, take bus 30 to Katwijk. It stops in front of the entrance gate of ESTEC (the journey takes about 25 minutes). Please note that this bus departures four times an hour during the day, and twice an hour after 19:00. For more information or other busses please consult the journey planner at http://journeyplanner.9292.nl/.

By Plane
From Schiphol airport, either take a taxi to ESTEC (30 minutes), or a train to Leiden (15 minutes) and then bus number 30 (25 minutes). With a rental car, follow the instructions above from Amsterdam.

By Taxi Service:
For those who need to arrange a taxi transfer from Schiphol airport, or other transfers, please contact the ESTEC preferred supplier Taxi Brouwer (tel. +31-71-36 11 000 or by email at info@brouwers-tours.nl)
Book and pay in advance via https://www.taxibrouwer.nl/en/estec/ or contact ESTEC Reception (email estec.reception@esa.int or telephone +31-71-565 4000 from 08:00-18:00).

By Schiphol - ESTEC / ESTEC – Schiphol Shuttle Bus:
A shuttle bus service is available from Schiphol airport to ESTEC from Monday to Friday. You can make your reservations and payments on-line via a dedicated ESTEC page:
https://www.taxibrouwer.nl/en/estec/.

The price of a single trip is 15.00€. A receipt is sent to your email and shall be taken into the bus as proof of payment. If you wish to make reservations with ESTEC Reception (tel.+31-71-565 4000) or Taxi Brouwer (tel. +31-71-36 11 000) this should be done at least one hour in advance. The meeting point for the shuttle bus is at the large red and white cube structure in the Airport arrival area.

Schiphol to ESTEC – Departure from Schiphol meeting point
Monday to Friday: 08:30, 09:00, 09:45, 19:45, 20:45

ESTEC to Schiphol – Departure from ESTEC Reception
Monday to Friday: 15:00, 15:30, 16:00, 16:30, 17:00, 18:00, 18:30

Hotel Shuttle bus service
All visitors to ESTEC staying in one of the six major hotels in Noordwijk can make use of the ESTEC Hotel Shuttle. The price of the Hotel Shuttle Noordwijk-ESTEC is 5.00€ (one way). Payment in bus only. A receipt is given after payment. Reservations are not necessary as the shuttle leaves at fixed times. An extra morning shuttle picks up travellers at hotels Heeren van Noortwijck, Admiraal and Royal. If you travel with more than one person, please inform info@taxibrouwer.nl in advance. The schedule of the ESTEC Hotel Shuttle is as follows:

Noordwijk to ESTEC Morning Schedule
Tuesday to Friday:

1st	2nd	3rd	Morning route
07:43	08:20	08:57	Hotels van Oranje (corner Koningin Wilhelminaboulevard/Schuitegat)
07:45	08:22	08:59	Palace Hotel
07:47	08:24	09:01	Prominent Inn Hotel (corner Koningin Wilhelminaboulevard/Olieburg)
07:50	08:27	09:04	Grand Hotel Huis ter Duin (in front of the overhead roof/canopy)
07:52	08:29	09:06	Alexander Hotel
07:54	08:31	09:08	Palace Hotel
08:06	08:43	09:20	ESTEC Gatehouse (**passengers without a badge must leave the Hotel Shuttle here, passengers with badge can continue to ESTEC Main Reception**)
08:08	08:45	09:22	ESTEC Main Reception

Extra morning shuttle

08:20	Heeren van Noortwijck
08:23	Hotel Admiraal
08:30	Hotel Royal
08:40	ESTEC Gatehouse (**passengers without a badge must leave the Hotel Shuttle here, passengers with badge can continue to ESTEC Main Reception**)
08:42	ESTEC Main Reception

ESTEC to Noordwijk Afternoon Schedule - Departure from ESTEC Reception
Monday to Thursday:

1st	2nd	3rd	Afternoon return route
16:30	17:15	18:00	ESTEC Main Reception
16:44	17:29	18:14	Palace Hotel
16:46	17:31	18:16	Alexander Hotel
16:48	17:33	18:18	Grand Hotel Huis ter Duin (in front of the overhead roof/canopy)
16:52	17:37	18:22	Hotels van Oranje (corner Koningin Wilhelminaboulevard/Schuitegat)
16:54	17:39	18:24	Golden Tulip Noordwijk Beach
16:55	17:40	18:25	Prominent Inn Hotel (corner Koningin Wilhelminaboulevard/Olieburg)