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PLATO RDCU

Using Open-source SpaceWire and RMAP IPs in the PLATO Router and Data compressor Unit (RDCU)

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OUTLINE

PLATO Mission

Instrument Control Unit (ICU)

RDCU architecture

FPGA architecture

SpaceWire IP core

RMAP Target IP core

Prototype board for IP verification

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PLATO MISSION

Mission goal

- Detection of terrestrial exoplanets up to the habitable zone of solar-type stars and characterisation of their bulk properties needed to determine their habitability.

Payload

- Set of 24 normal cameras resulting in many wide-field co-aligned telescopes, each telescope with its own CCD-based focal plane array
- Set of 2 fast cameras for bright stars, colour requirements, and fine guidance and navigation.

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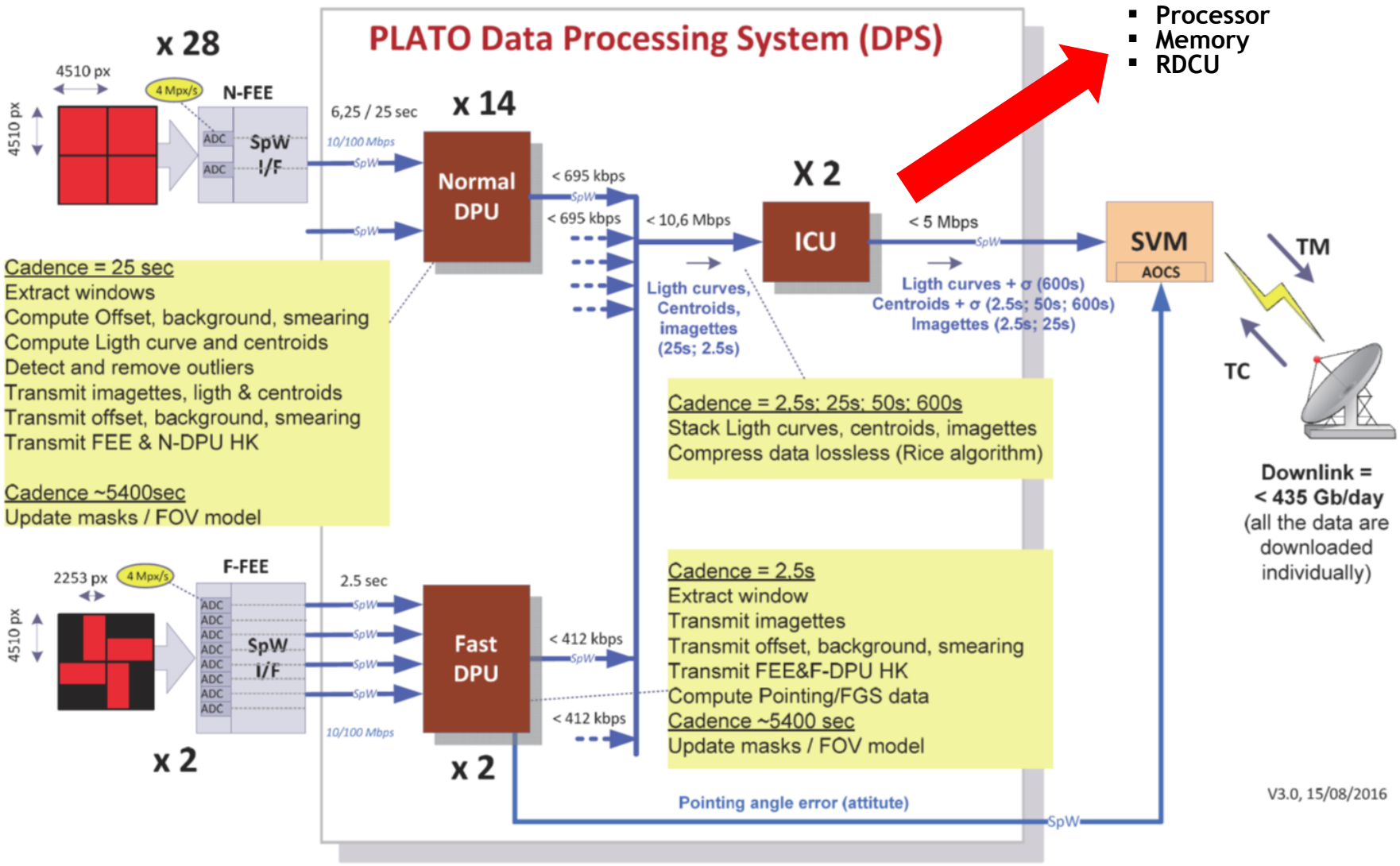
INSTRUMENT CONTROL UNIT (ICU)

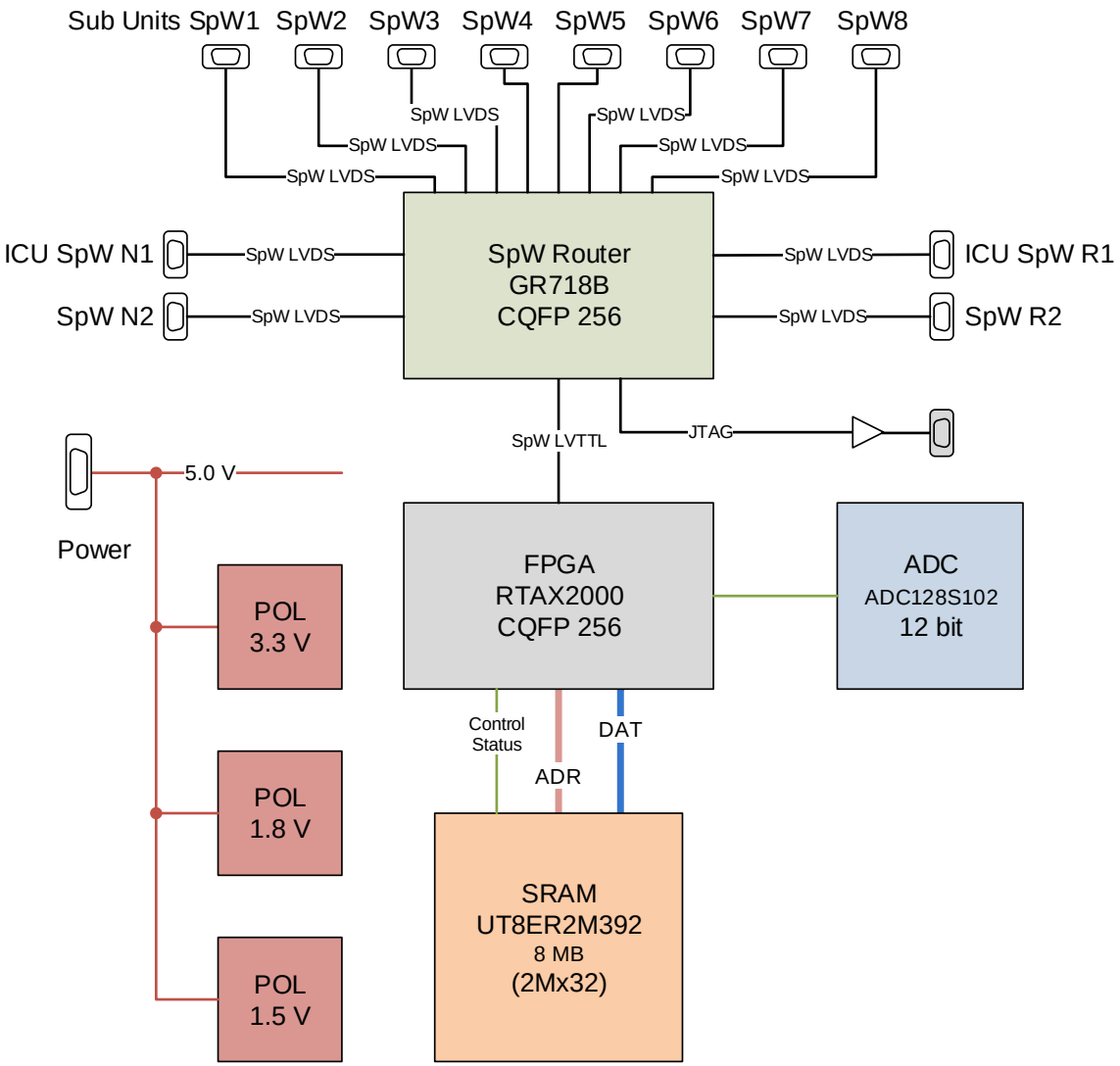


Source: "PLATO Definition Study Report (Red Book)," pp. 1–139, Apr. 2017. [Online]

RDCU ARCHITECTURE

Characteristics

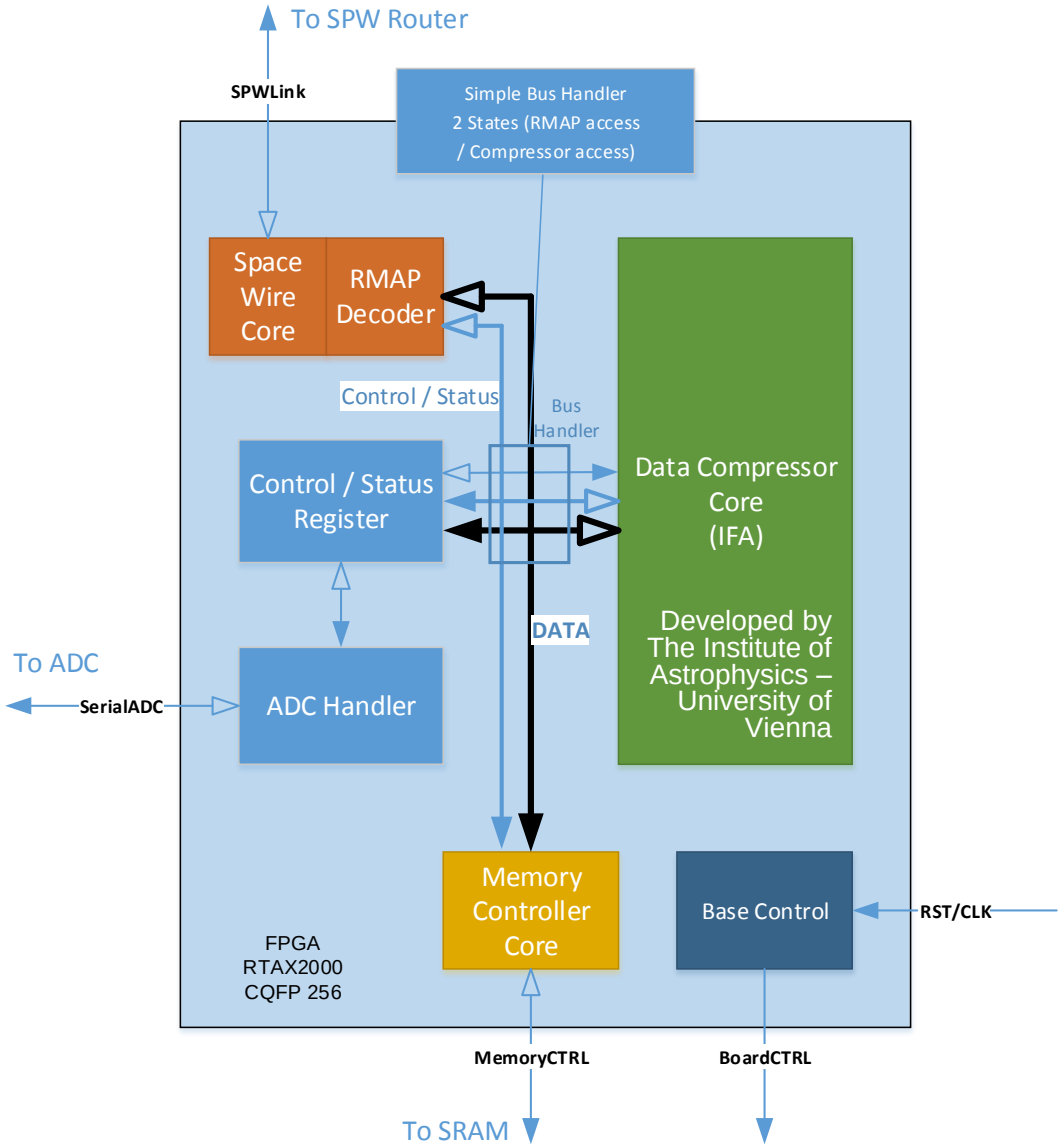
- SPW Router GR718B
  - 8 SPW links for
    2x N-DPUs, 2x F-DPUs,
    2x N-AEU, 2x F-AEU
  - 4 SPW links to ICU-Memory board:
    2x Nominal, 2x Redundant
  - 1 SPW LVTTL for FPGA
    (data compressor)
- FPGA RTAX2000S (for prototyping is used ProASIC3E)
- 8 MB SRAM memory
- ADC for housekeeping data
- PoLs for power supplies



FPGA ARCHITECTURE

Characteristics

- The selected FPGA is the RTAX2000S
- The SpaceWire link should be able to run at 100 Mbps
- The base clock frequency is 100 MHz but the system should run with 25 MHz
- A simple Wishbone bus is used to interconnect two masters (RMAP decoder and data compressor) to two slaves (registers bank and SRAM memory controller)



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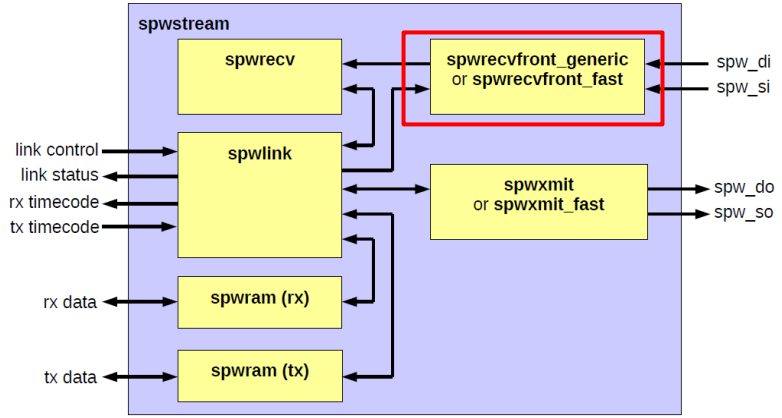
SPACEWIRE IP CORE (1/4)

Characteristics

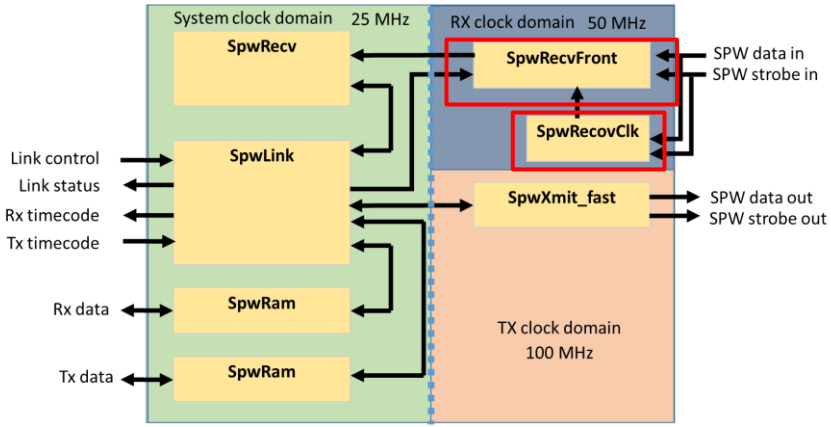
- SpaceWire Light IP from Opencores.org
- Claims to be conformal to a SpaceWire encoder-decoder of ECSS-E-ST-50-12C

Modifications

- 3 independent clock domains: System clock (25 MHz), Rx clock (50 MHz/DDR) and Tx (100 MHz)
- CDC analysis performed
- The IP was modified to be able to process an input rate of 100 Mbps using a 25 MHz system clock.
- An receiver front-end was developed to support the clock recovery feature
- SEU considerations: avoid BRAM usage, Synplify Safe FSM feature



Original Block diagram



Modified Block diagram

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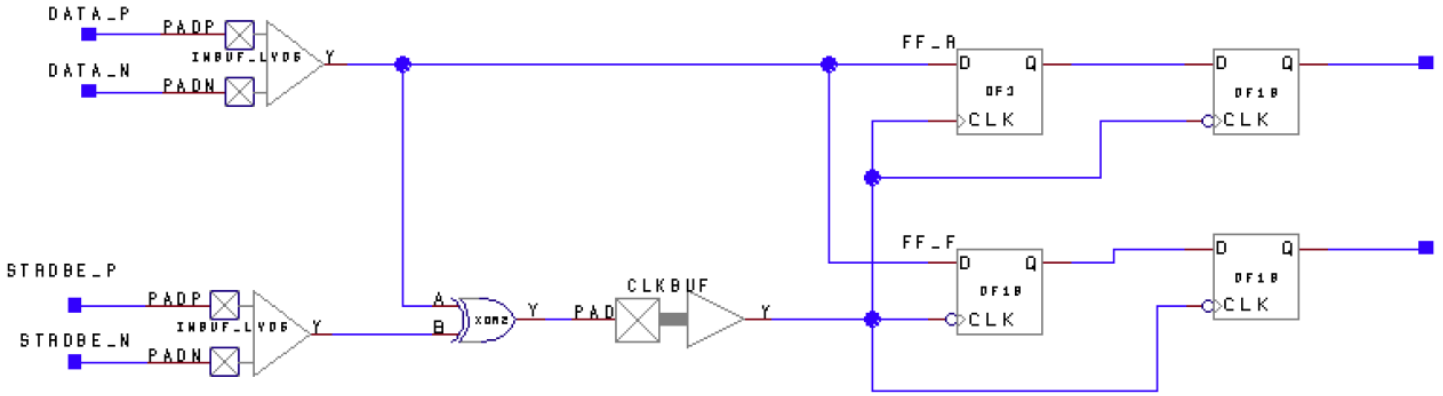
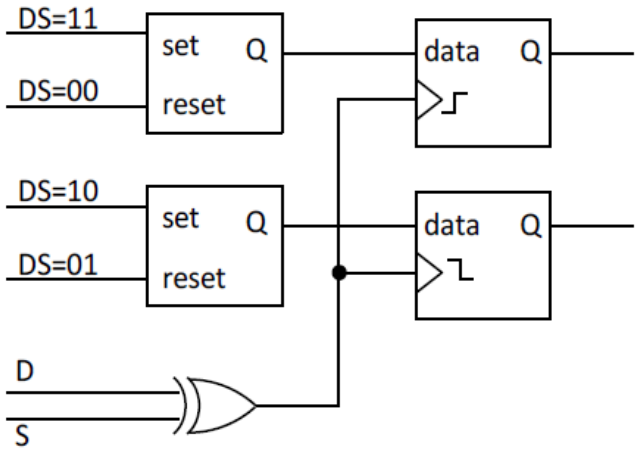
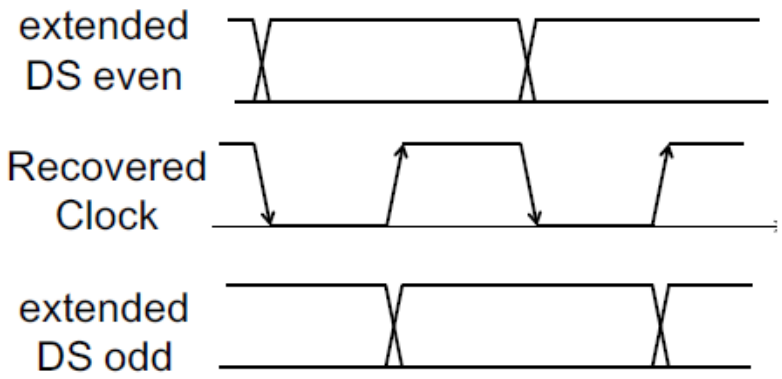
SPACEWIRE IP CORE (2/4)

Clock recovery feature



Microsemi app note: Implementation of the SpaceWire Clock Recovery Logic in Actel RTAX-S Devices





Nomachi, M. Race Condition Free Spacewire Decoder For FPGA. 2010 Spacewire Conference.

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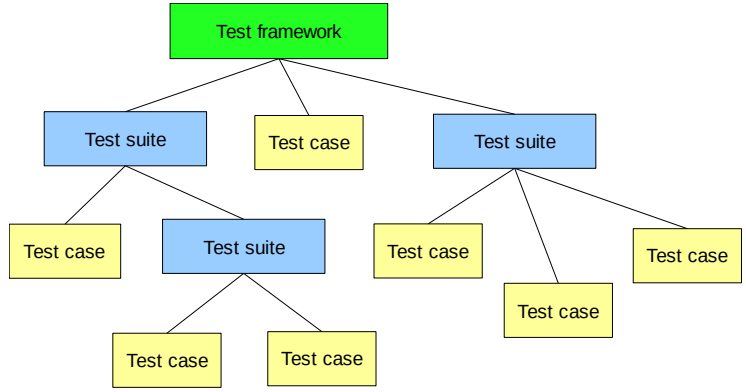
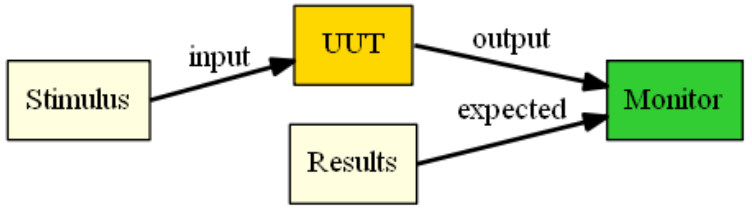
SPACEWIRE IP CORE (3/4)

Functional Verification

- VHDL VHUNIT used as testbench structure
- Functional Coverage (OSVVM) used as principal verification methodology
  - A set of coverage points were defined based on ECSS-E-ST-50-12C
- Two test scenarios:
  - Evaluation of error cases
  - Pseudo random data transfer between two IP instances



VHUNIT framework



Results

- Link control FSM functional coverage: 100 %*
- Coverage points functional coverage: 100 %
- Code coverage (ALDEC tool): 99.1%**

* excluding some error conditions that are not feasible to evaluate

** due to the generic nature of the IP

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SPACEWIRE IP CORE (4/4)

Issues found after functional verification

- Credit errors were reported to the network level outside of the run state. (violating clause 8.9.5)
- The *disable link* input should be asserted for more than one system clock cycle. If not, the IP will not be able to reset the *txdiscard* register bit. This bit is used to discard any packet being transmitted during a link error.

Limitations

- Disconnect detection: Incoming bits are processed in pairs. So, only after the first 2 bits, the disconnect detection is enabled.
- Handling empty packets: The IP does not handle empty packets. The IP was modified to quietly discard empty packets.

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RMAP TARGET IP CORE (1/3)

RMAP for RDCU

- The RDCU FPGA requires a target node of the RMAP protocol. This means that it shall be able to process RMAP commands and generate RMAP replies.
- It is not required to implement all the commands proposed in ECSS-E-ST-50-52C. We are using only a subset of commands.

Modifications on the RMAP IP

- The IP was based on shimafujigit/SpaceWireRMAPTargetIP in github.com
- The performance of the IP was improved to process RMAP packets in less clock cycles.
- The IP interfaces were adapted to be compatible with the SPW IP and our internal data bus.
- The error register was expanded to support user-defined errors.

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RMAP TARGET IP CORE(2/3)

Discrepancies found in the ECSS-E-ST-50-52C standard

- First issue: Contradiction between clause 5.3.3.4.6.a and clause 5.3.3.4.6.c, both related to a write command packet, where in
  (a) it is said to not send a reply if an invalid packet type is received but on
  (c) it is said that it is possible to send a reply if the reply bit is set in the command field.
  We have decided to implement clause 5.3.3.4.6.c.
  The same problem happens with clauses 5.4.3.4.6 (Read) and 5.5.3.4.6 (RMW).
- Second issue: Through the text it is mentioned that if an EEP is received before the header CRC, then the error status code should be 0x07. But in the table describing the error codes (Table 5-4), the EEP code is described as evaluated only after receiving a valid header CRC.
  We have decided to implement the first behavior.

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RMAP TARGET IP CORE(3/3)

Functional Verification

- A similar approach to the SPW verification is used.
- Using the ECSS standard as reference, we coded a set of RMAP packets that will trigger all possible errors related to the packet. These same packets will be used during the hardware test.

Logic Synthesis & High reliability

- Currently we have an open issue related to the implementation of the ‘safe FSM’ feature of Synplify (Synopsys).

Analysis of SEU effects

- We would like to run some fault injection campaigns (FSMs) to verify the functionality of the Synplify high reliability feature.

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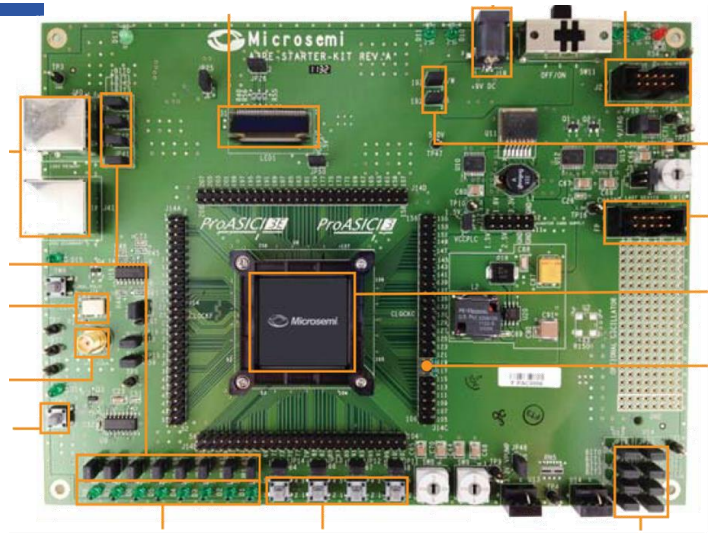
PROTOTYPE BOARD FOR IP VERIFICATION



Microsemi evaluation board

IWF adapter board

- This board will be connected to a computer using SpaceWire USB conformance tester
- Usage: send and receive data via SpW from the board

IWF Adapter board

- 2 SPW connector MDM 9-pin
- LVDS driver and receiver
- 5 Debug Header (FTSH-110-01-LM-DV)
- 8 Debug Leds
- 4 SRAM memories (2M x 32 bits)

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SUMMARY

- Both IPs are open-source IPs that were adapted to meet our requirements. So, we are not using them “as it is”.
- Testbenches developed with VHUNIT and OSVVM have give us good results in terms of code and functional coverage.
- Some issues were detected and corrected during the functional verification.
- After hardware testing, we intend to release the source codes for both IPs.

Thank you!

Q & A