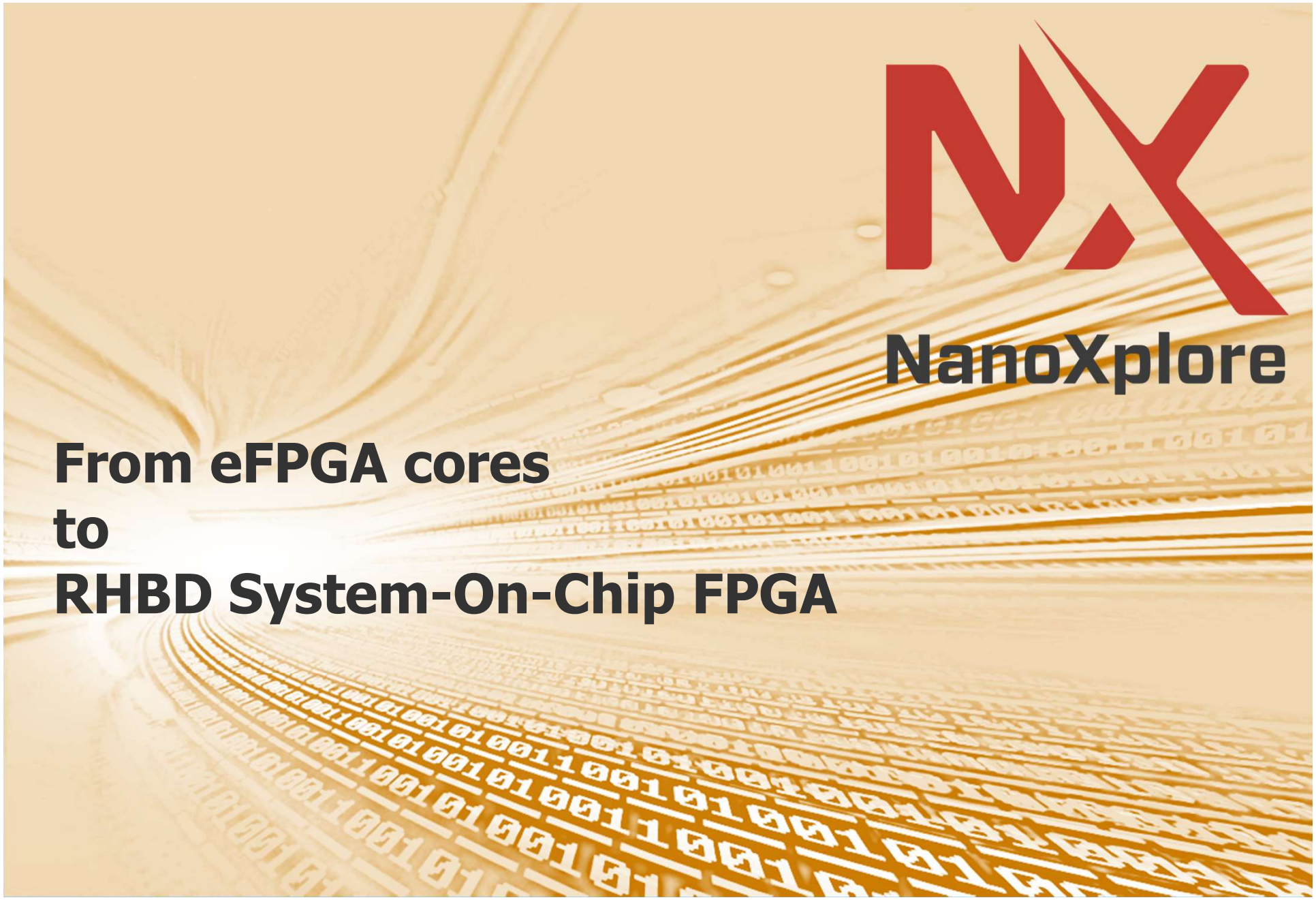
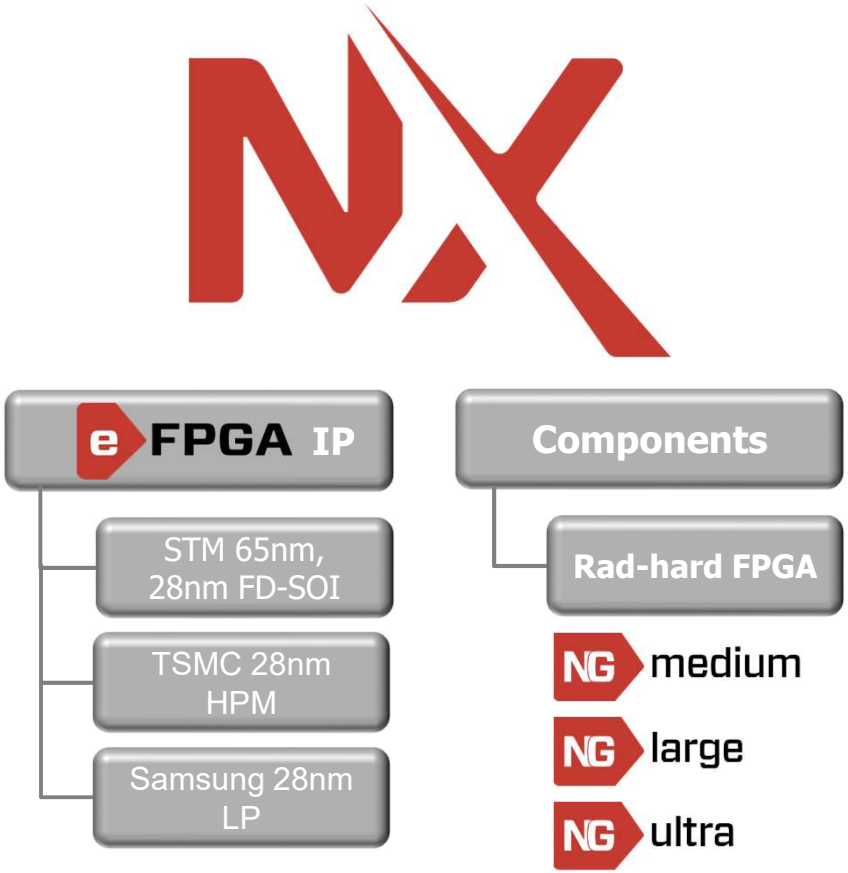


4th SEFUW – ESA/ESTEC Noordwijk (NL) – 9/11apr18

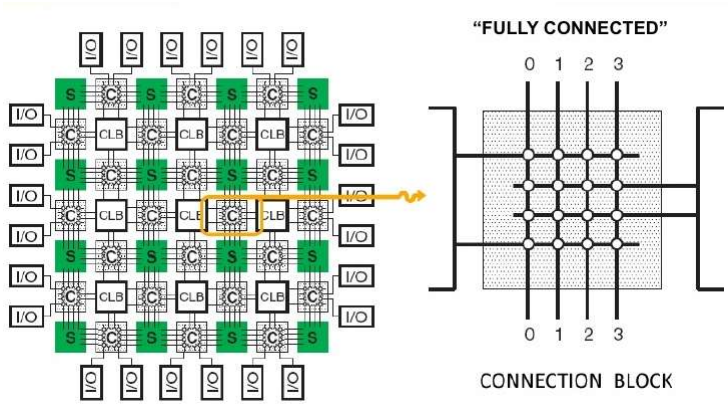
NanoXplore Overview



- **Created in 2010** by three veterans of semiconductor industry with long experience in the design, test and debugging of FPGA cores.
- **Fabless** semiconductor company headquarter in France
- R&D engineers in two offices in France:
  - Sèvres: Hardware developments
  - Montpellier: Software developments
- NanoXplore is a leader in the design of large scale programmable logic arrays for state of the art FPGA cores
- The company is focusing on 2 main activities:
  - Offer hard block embedded FPGA core IP (NX-eFPGA)
  - Developing rad-hard FPGA qualified for space applications (from BRAVE contract)

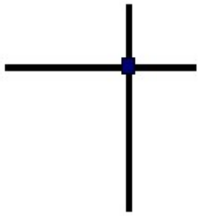
NanoXplore - FPGA architecture

- 1st of all, hereafter a basic FPGA architecture

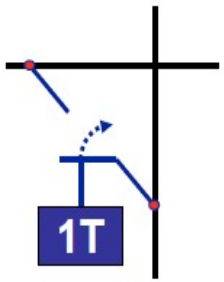


- 2nd, there are 4 different ways to do interconnection:

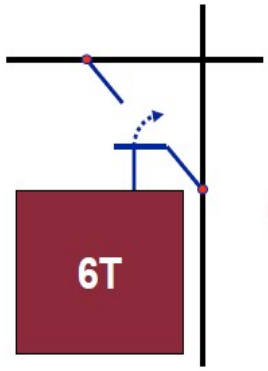
Antifuse



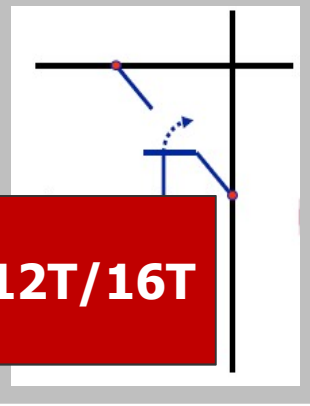
Flash-based



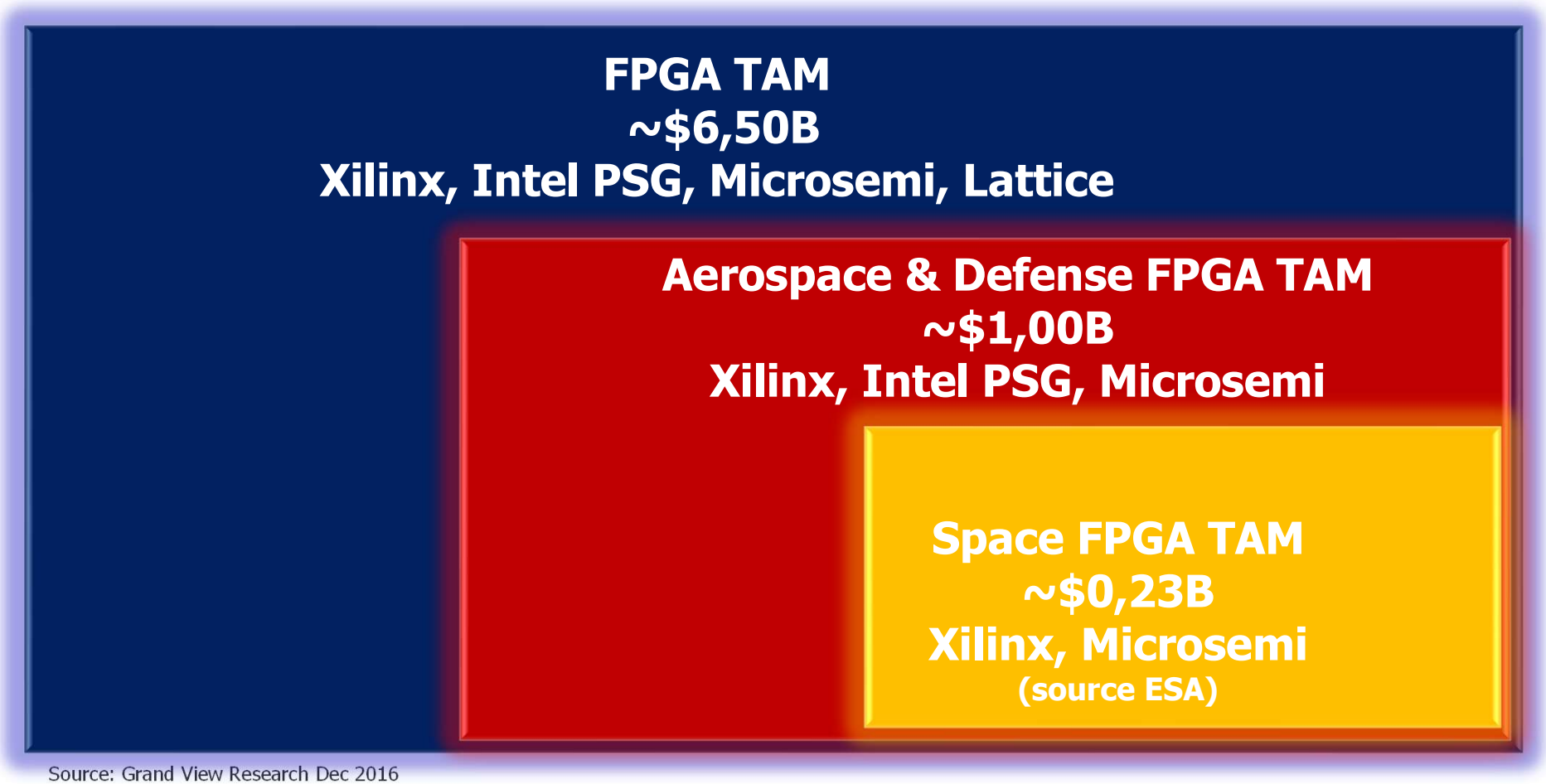
Std 6T-cell SRAM



RHBD 12T/16T-cell SRAM

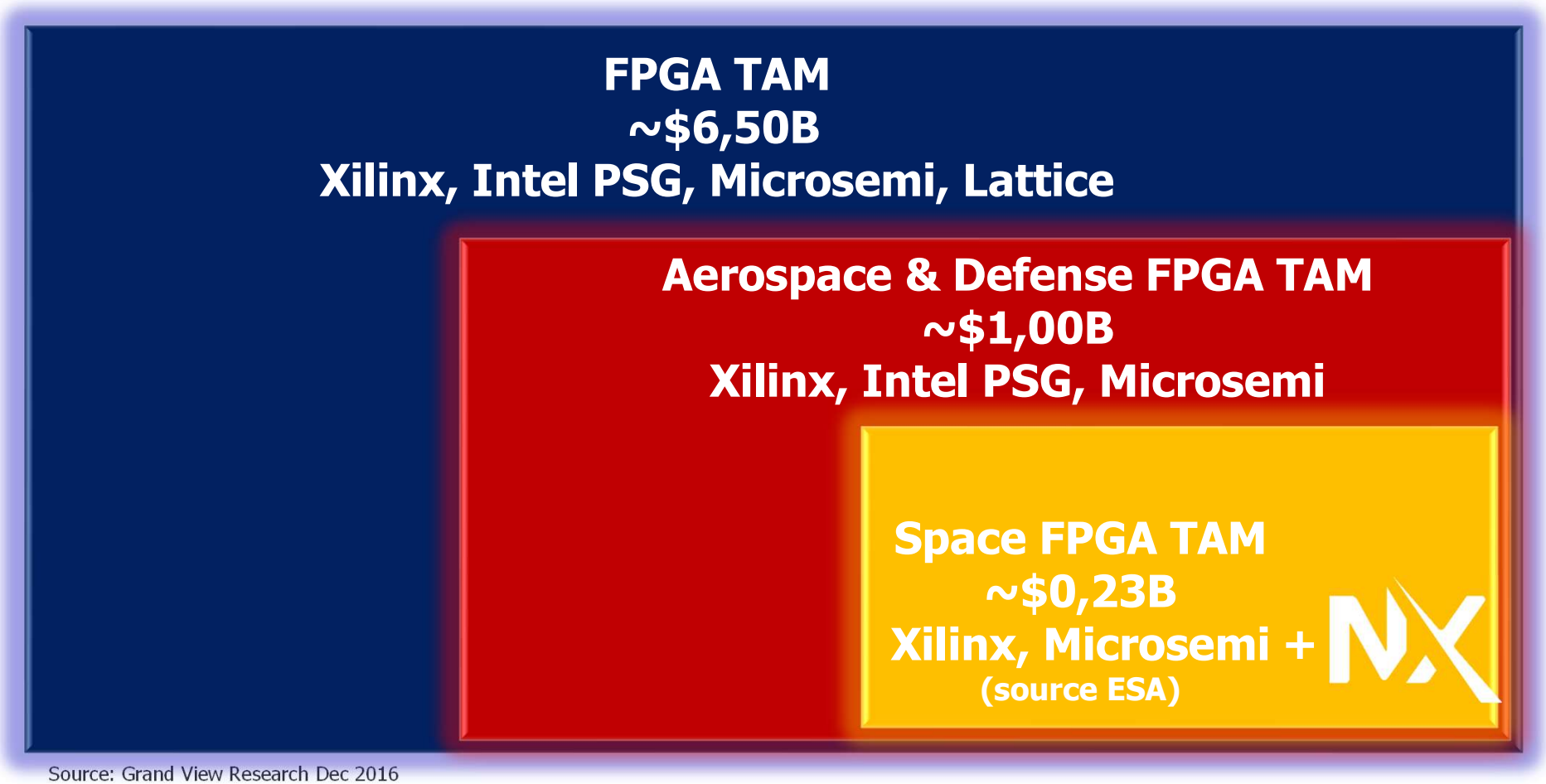


FPGA market and Main Vendors



Source: Grand View Research Dec 2016

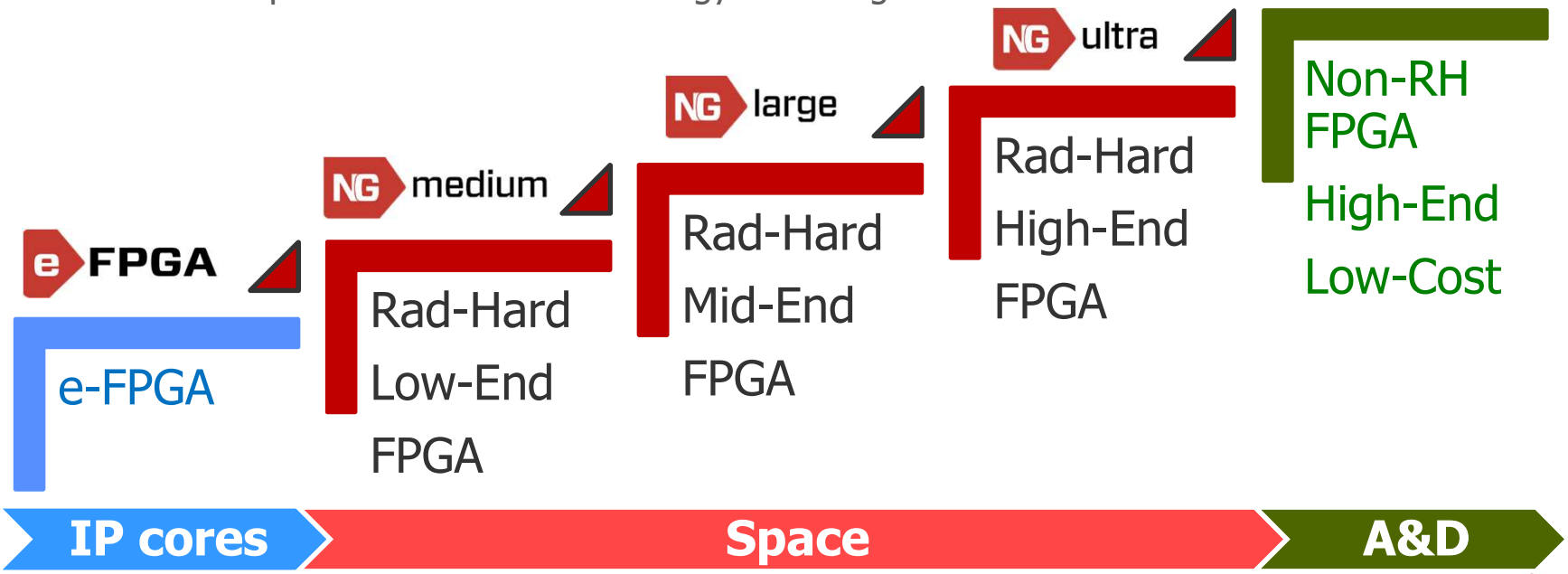
FPGA market and Main Vendors



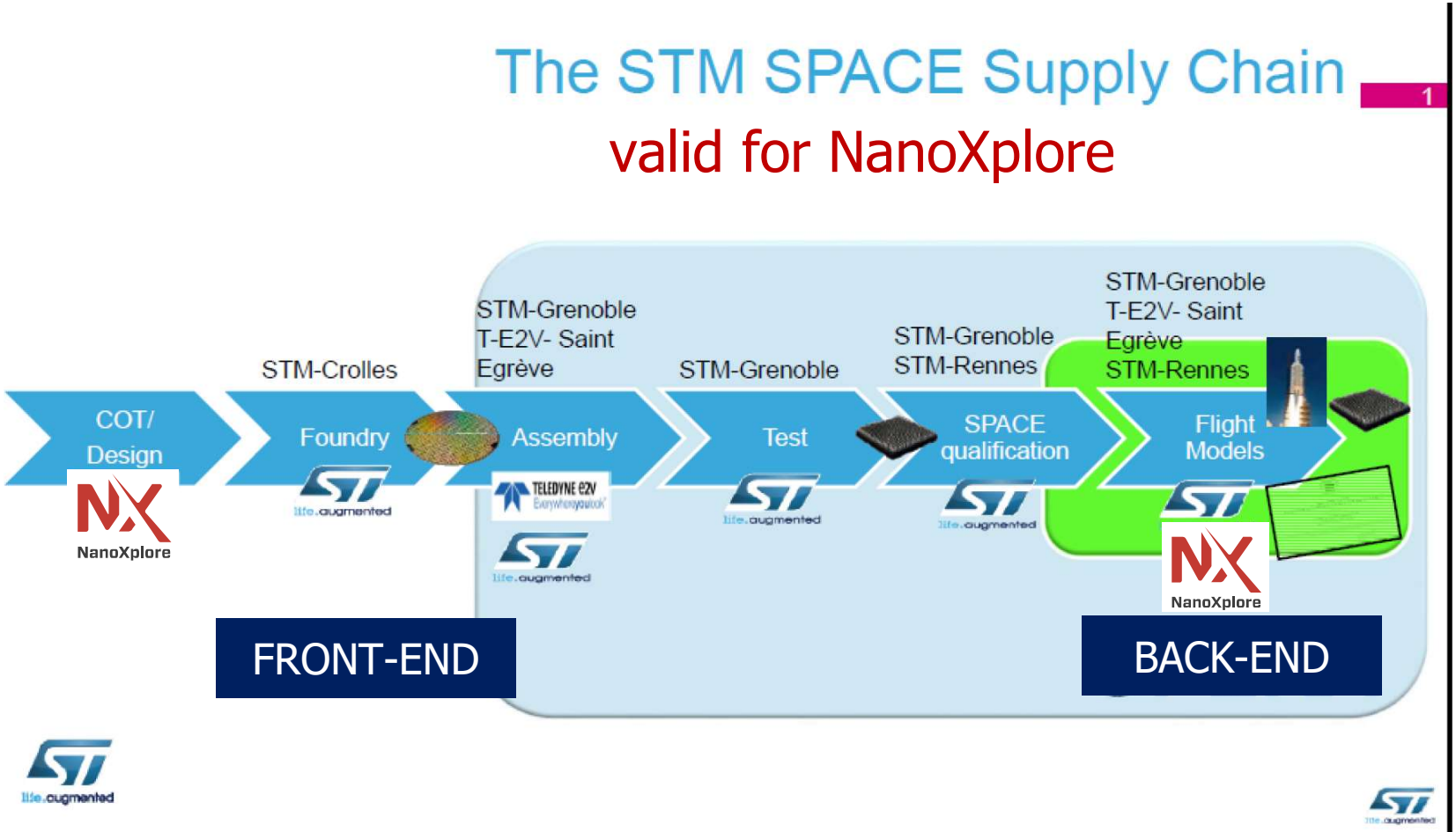
Source: Grand View Research Dec 2016

NanoXplore – From eFPGA to RH FPGA

- NX has a strong experience in developing eFPGA cores on the most advanced technology nodes.
- **Hi-rel** markets (like space) require specific features (hardening, reliability, security etc) which are not well addressed by market leaders due to limited market opportunity: **Not true for NX**.
- European funding to support that initiative: **CNES, ESA, EC, DGA, DGE, BPI** …
- Space market has many synergies with additional market such as Avionic, Military, Railway and Medical, even Automotive
  - Limited competition and clear technology advantages.



NanoXplore – Supply-Chain



Export Regulation

- NX RH FPGA devices are **ITAR & EAR-free** ➔ No Dependance to USA.
- Classified 3A001.a.2.c according (EC)2015/2420 rules.

US Dep't. of Commerce Bureau of Industry & Security	US Department of State Directorate of Defense Trade Controls	US Department of Treasury Office of Foreign Assets Controls
•Export Administration Regulations •"Dual Use" products/ technologies •Items subject to EAR •Commerce Control List	•International Traffic in Arms Regulations •Inherently military products/ technologies •U.S. Munitions List	Administration of US economic sanctions & embargoes

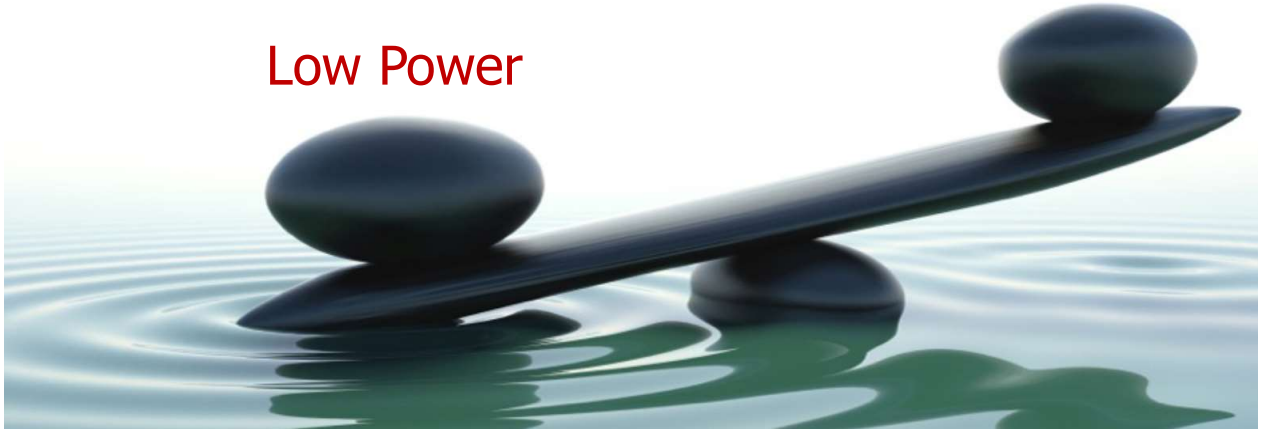
Process Technology

High Performance vs Low Power

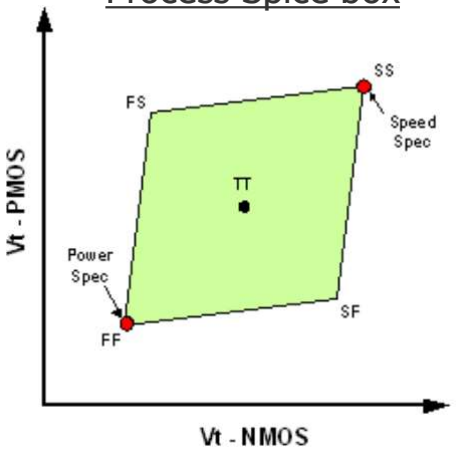
- Chip designers are challenged to choose between
  - Standard processes to meet performance goals or
  - Low Power processes to meet power goals.

High Performances

Low Power



Process Spice box

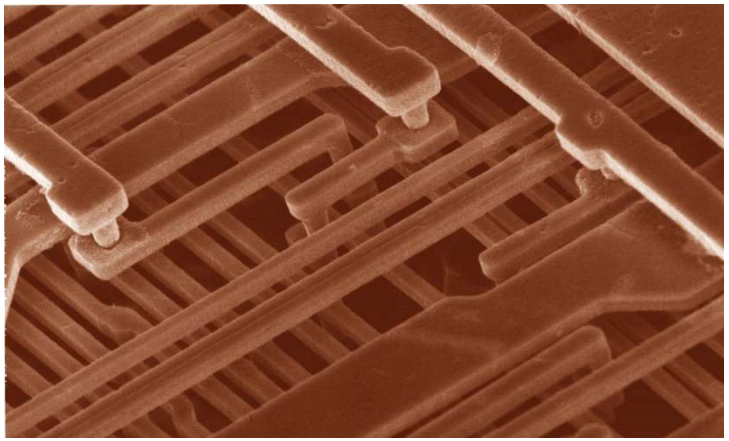


- Parts designed for a fixed supply voltage and manufactured in the FF corner will have the highest frequency, have the most leakage and provide the best performance.
- Parts manufactured in the SS corner will have the slowest performance and have the least leakage and consume the least power.

Process Technology

STM C65 SPACE Low Power

life.augmented



Features

Process

- STMicroelectronics C65SPACE (65nm CMOS)
- 3.3V IO gate oxide GO2 (5nm)
- 1.2V core gate oxide GO1 (1.8nm), triple VT transistors
- 7 copper metallization,5 thin and 2 thick
- Low-K inter-metallic dielectrics for thin metal layers
- High density SRAMs
- Compatible with flip-chip and wire bonding packaging

Radiations

- SEL-free up to LET = 60Mev/mg/cm2 at 125°C Tj and Vdd max
- SEE hardened library
- Tested up to a total dose of 300 krads (Si)

Reliability

- Library cells models with 20 years aging
- Transistor models including aging alteration
- ESD better than:
  - 2kV in HBM (Class 2 / MIL-STD-883H)
  - 150V in MM
  - 250V in CDM

Library offer

- Comprehensive library of standard logic with PVT and aging corners models
- IO pad libraries provide interfaces at 3.3V +/- 0.30V, 2.5V+/-0.25V and 1.8V +/-0.15V
- High speed IO Pad LVDS supplied at 2.5V +/- 0.25V up to 650Mbps
- Cold sparing IOs with single/double row support
- Memories generation: single port SRAM, ROM, Dual port SRAMs, BIST library, EDAC library
- Wide-range PLLs 1.2GHz with multi-phase outputs
- 6.25Gbit/s high speed serial links (HSSL)

Design flow

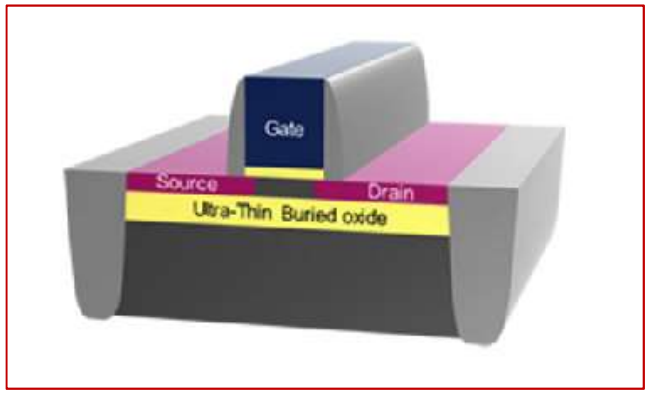
- An ST customized design flow (RTL to GDS) invoking commercial solutions (Synopsys, Cadence, Mentor…) is available for partners and certified design houses:
  - Front-End kit from RTL to gates based
  - SiPKit for IO ring generation
  - FFKit for place and route
  - SignOffKit for final verification before tape-out
- For customer owned tools (COT) flow, ST provides the C65SPACE design platform along with the DRM and sign-off kit.

Description

The C65SPACE is fabricated on a proprietary 65nm, 7 metal layers CMOS process intended for use with a core voltage of 1.2V ±0.10V.
The ST standard-cells, memories and PLL have been designed and characterized to be compatible with each other.

Process Technology
STM C28 SPACE FD-SOI

- FD-SOI substrates enable ultra-low-power features, unique cost/performance tradeoff, high-reliability and high-performance-mixed signal integration for a wide range of applications.



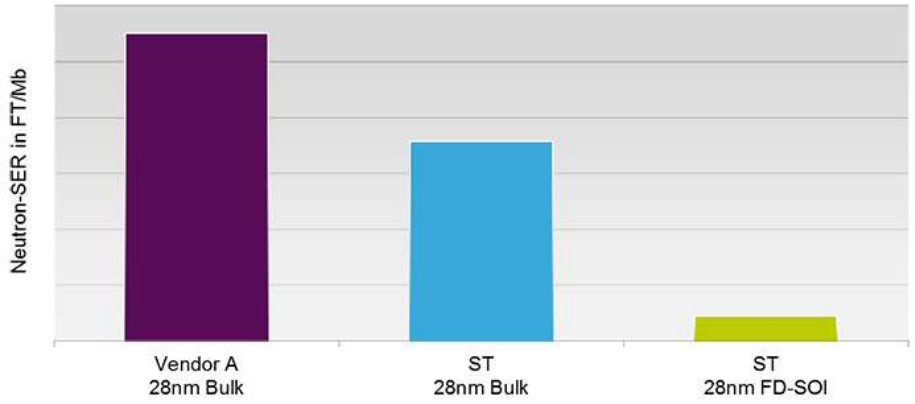
Power and energy efficiency
Ultra low leakage, wide Body-Bias & operating voltage range

Analog performance
for mixed signal & RF design

Robustness
for mission critical applications

Cost effective platform

Soft Error Rate comparison

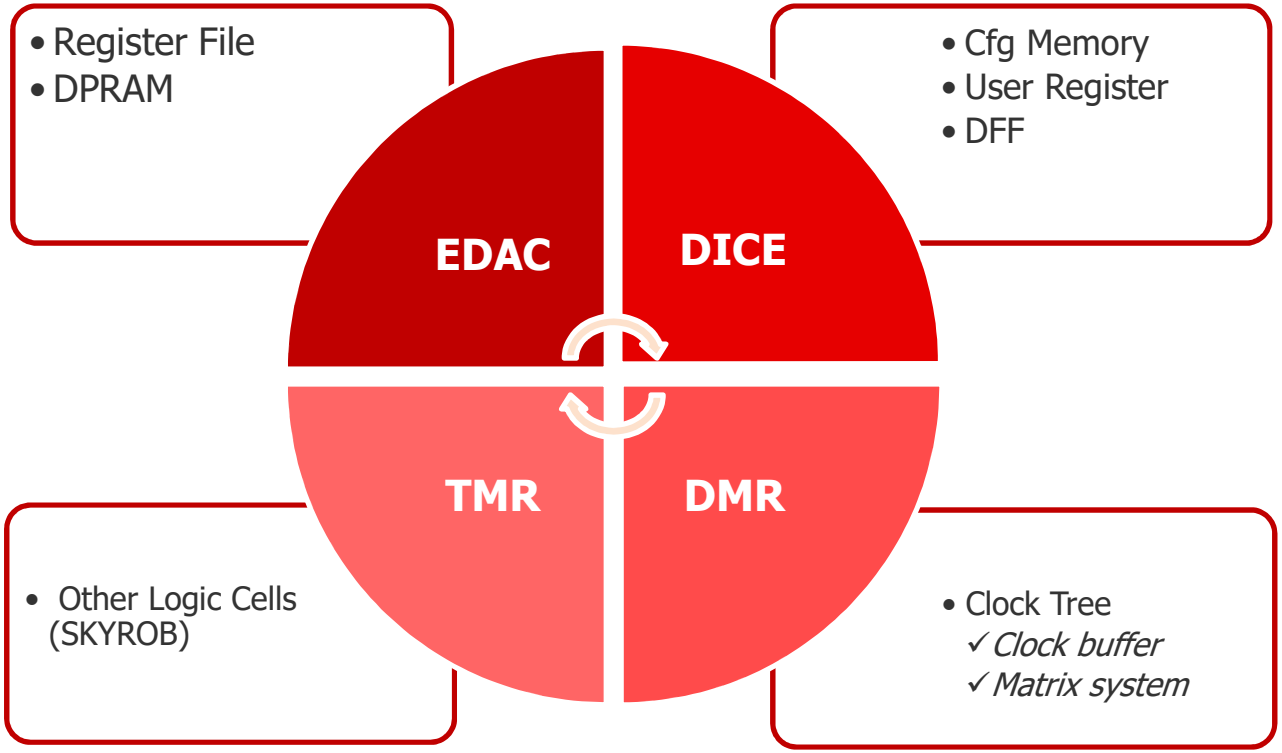


10x less
Std 28nm Bulk
vs ST 28nm FD-SOI

Source: http://www.st.com/content/st_com/en/about/innovation---technology/FD-SOI/efficiency-at-all-levels.html

NX FPGAs are Rad Hardened

All logic of NX FPGAs is hardened by design (RHBD)
and simulated with TFIT software

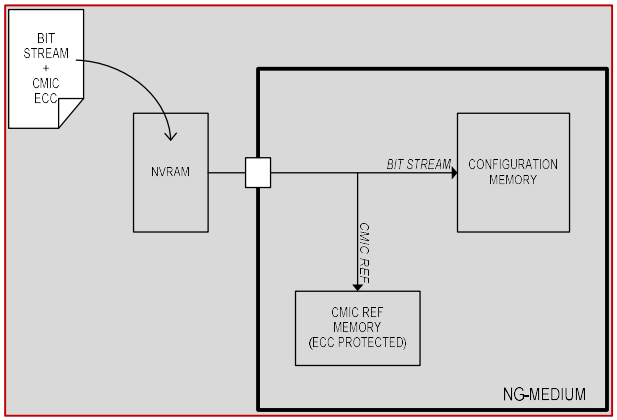


On top of it,
Embedded Configuration Memory Integrity Check ("CMIC")

CMIC Overview

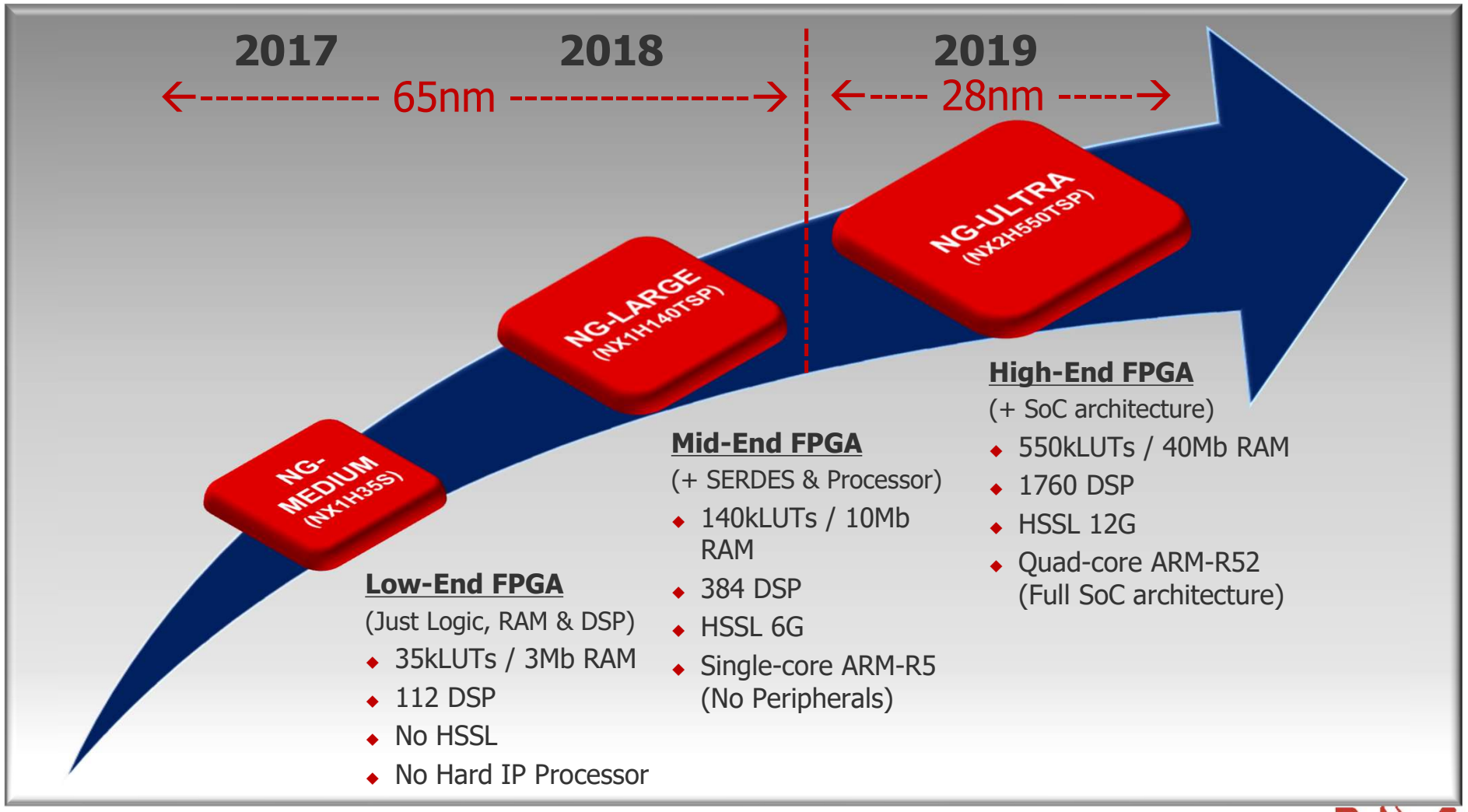
CMIC= Configuration Memory Integrity (= Scrubber Ctrl)

- The CMIC is an embedded engine performing automatic verification and repair of the configuration memory.

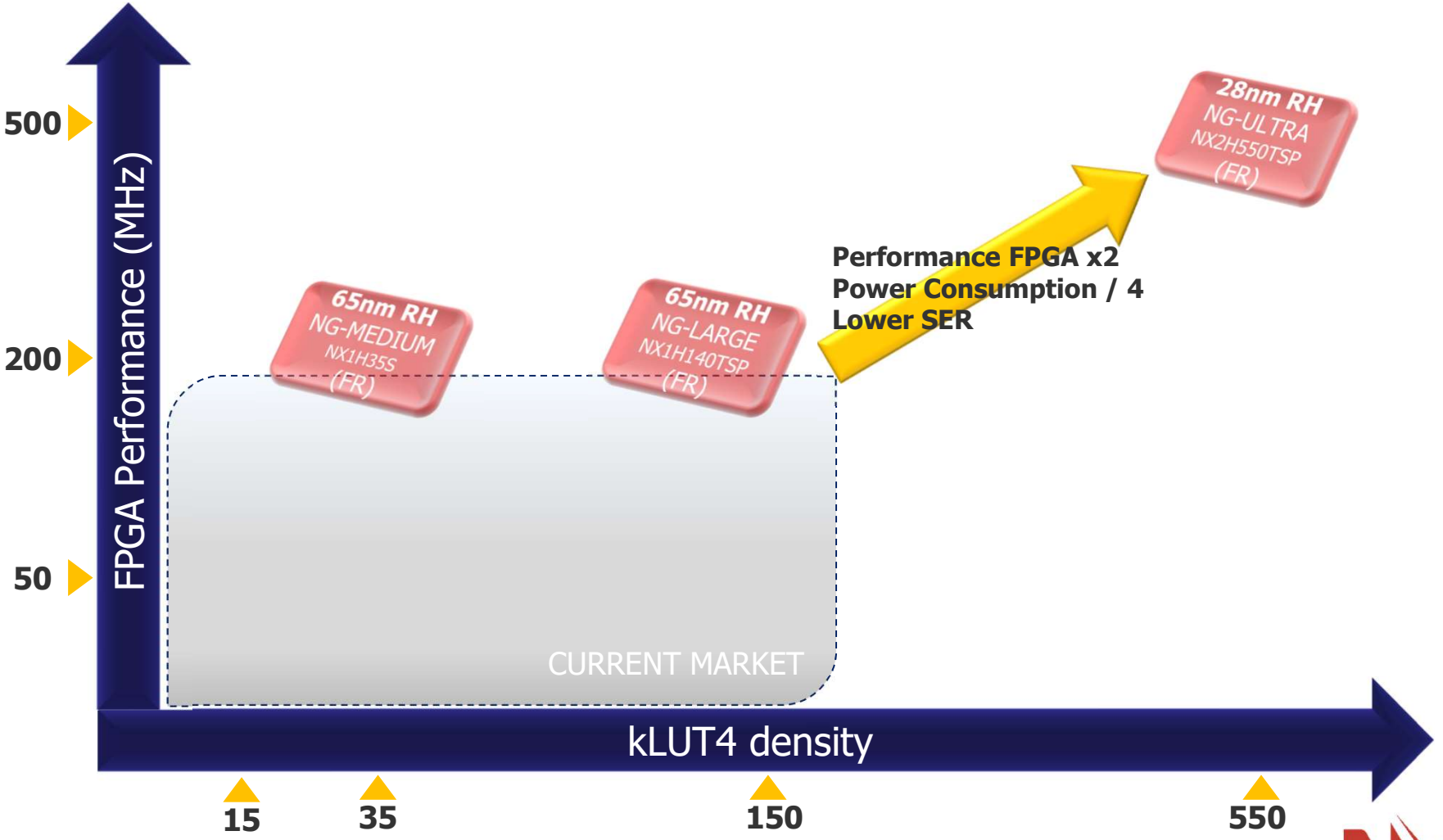


- The CMIC period can be set by the user.
- At 50MHz, the minimum period is 5.3 ms and the maximum 65 days.
- The configuration memory scan takes 4ms (+1.3ms delay).
- The CMIC reference memory is protected by ECC.
- The CMIC does not need to access the external NVRAM when performing checks and repairs at run time.

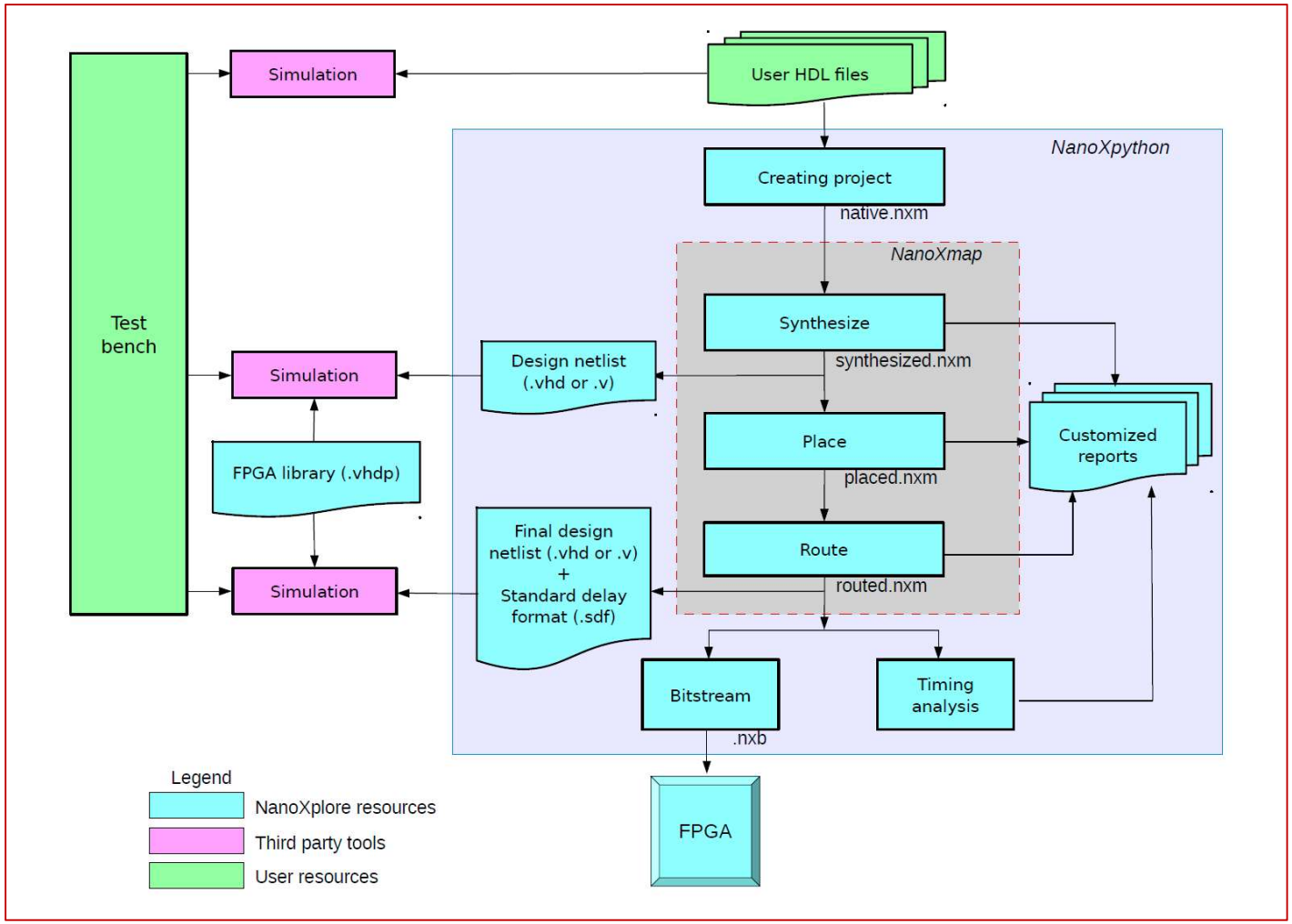
NanoXplore Rad-Hard FPGA Roadmap



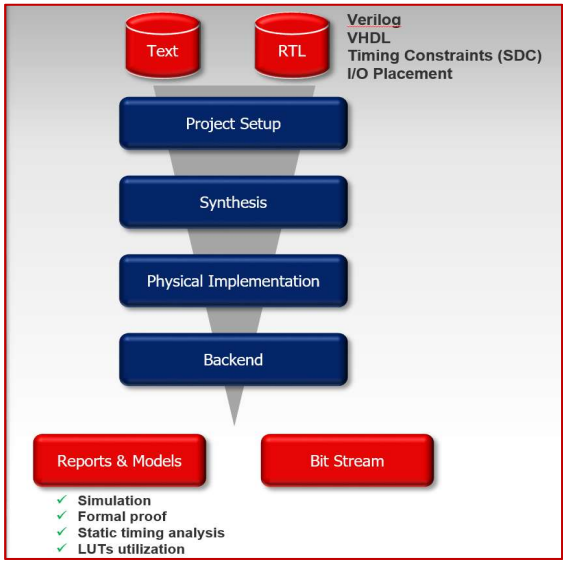
NX RH FPGA products positioning



Programming Software: NanoXmap Overview



NanoXmap Programming Software



NanoXmap-v2 targets to reach Best Performances/Features by End-2018

- H1-19: NanoXmap v3, IP Library
- H2-18:
  - NG-Large process on-going
  - Embedded Logic Analyser
- Q2-18: NG-Medium process stabilized
- Q3-17 to Q1-18:
  - NanoXmap optimation process against
    - ✓ Logic density
    - ✓ Operation frequency (*)
- 2014 to Q3-17:
  - NanoXmap development: database, algorithms, debug and flow set up from synthesis to bistream
  - Implementation of all FPGA blocks

(*) Acc. LP process

Next planned NanoXmap features

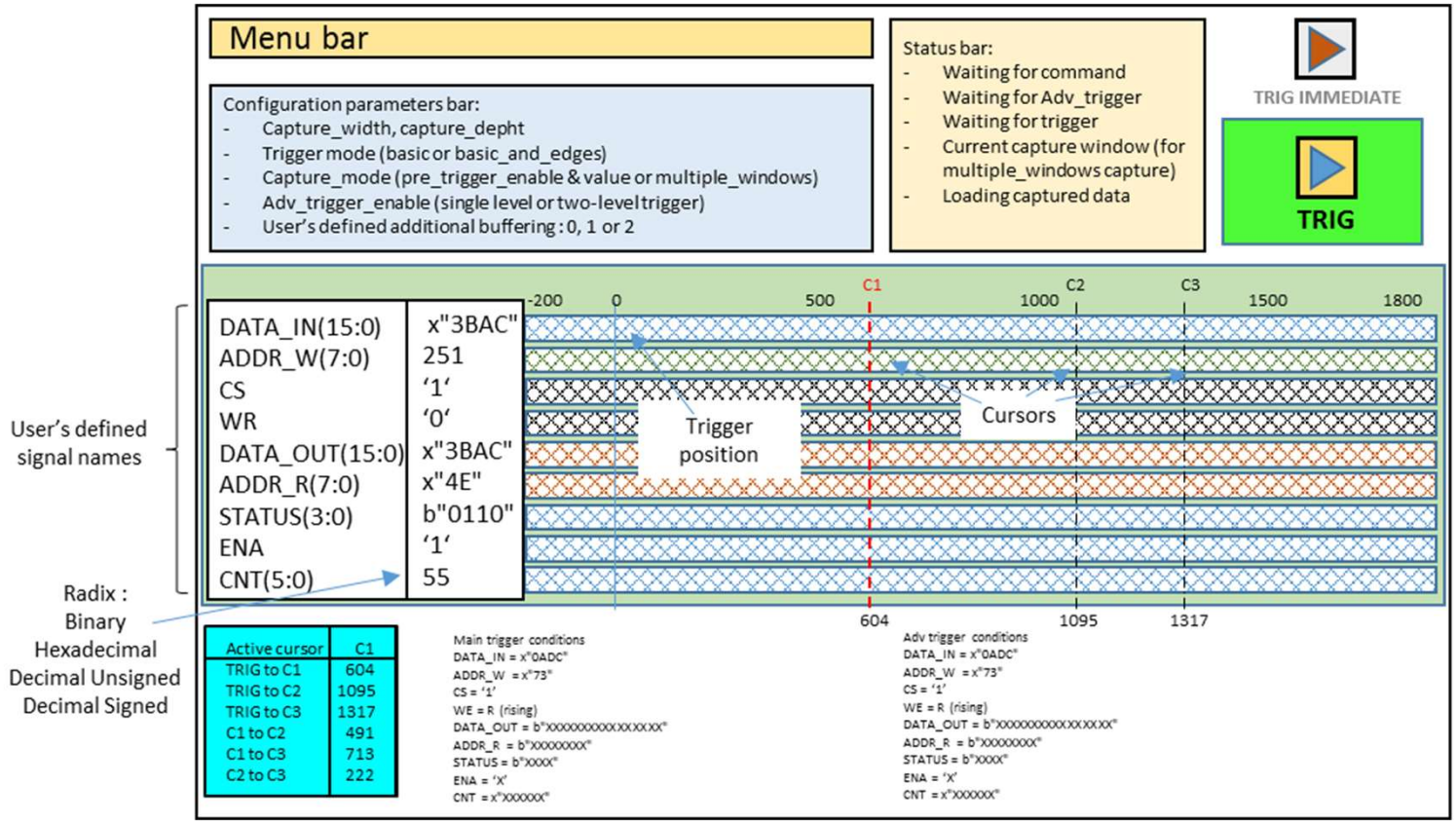
IP Library

- **Planned in coming weeks**
  - *SpaceWire IP core*
  - *DDR Interface (DFI2.1)*
- **In the pipe**
  - *Parallel FIR filters generator,*
  - *FIFO generator (Synchronous & Asynchronous),*
  - *SIN/COS lookup table,*
    even Direct Digital Synthetizer (DDS) or Numerically Controlled Oscillator (NCO),
  - *Complex Multiplier, Multiplier 24*30bits, Clock generator, etc.*
- **From NX Eco-system**
  - 3D-PLUS*: DDR Controller,*
  - Adentis/Maya Technology*: Mil-Std-1553B BC/RT,*
  - Skylabks*: PicoSkyFT-L, and PicoLIB (UART, Timer, I2C, GPIO, …)*
  - STAR Dundee*: SpaceWire, SpW CODEC, RMAP, Routing Switch,*
    even High Perf. FFTs, Image Processing, Camera Interface, CAN…

And you, what do you need?

NanoXmap Embedded Logic Analyser

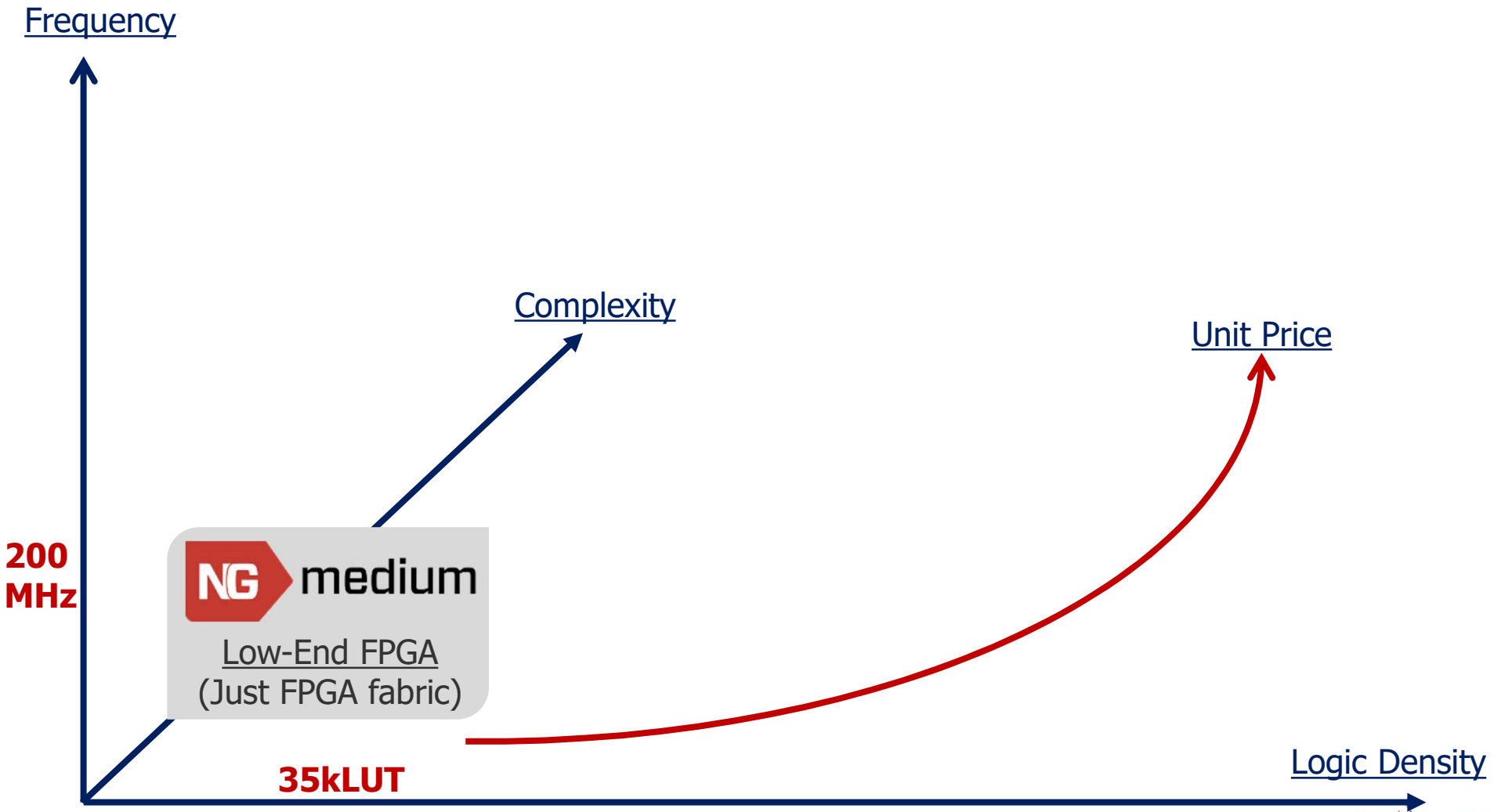
- Embedded Logic Analyser IP core (currently in VHDL)
- Expected Q3-18



1st NX Rad-Hard SRAM-based FPGA

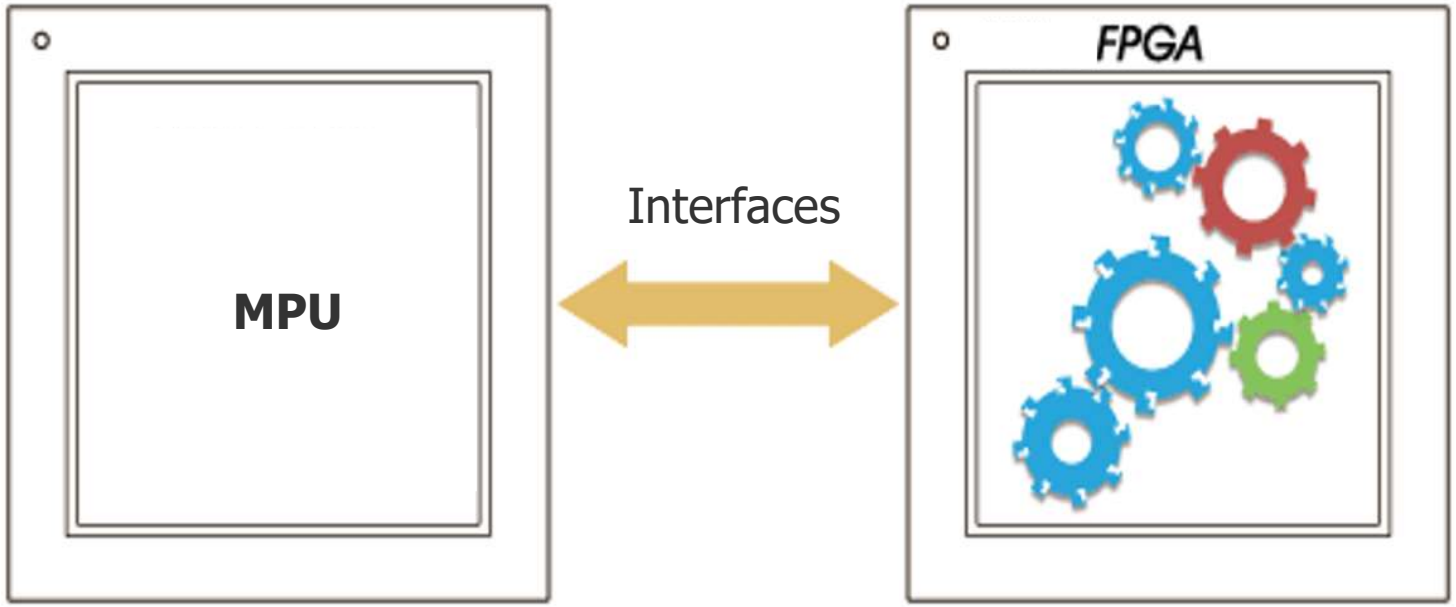
NanoXplore Rad-Hard FPGA Roadmap

Step1 – NG-Medium

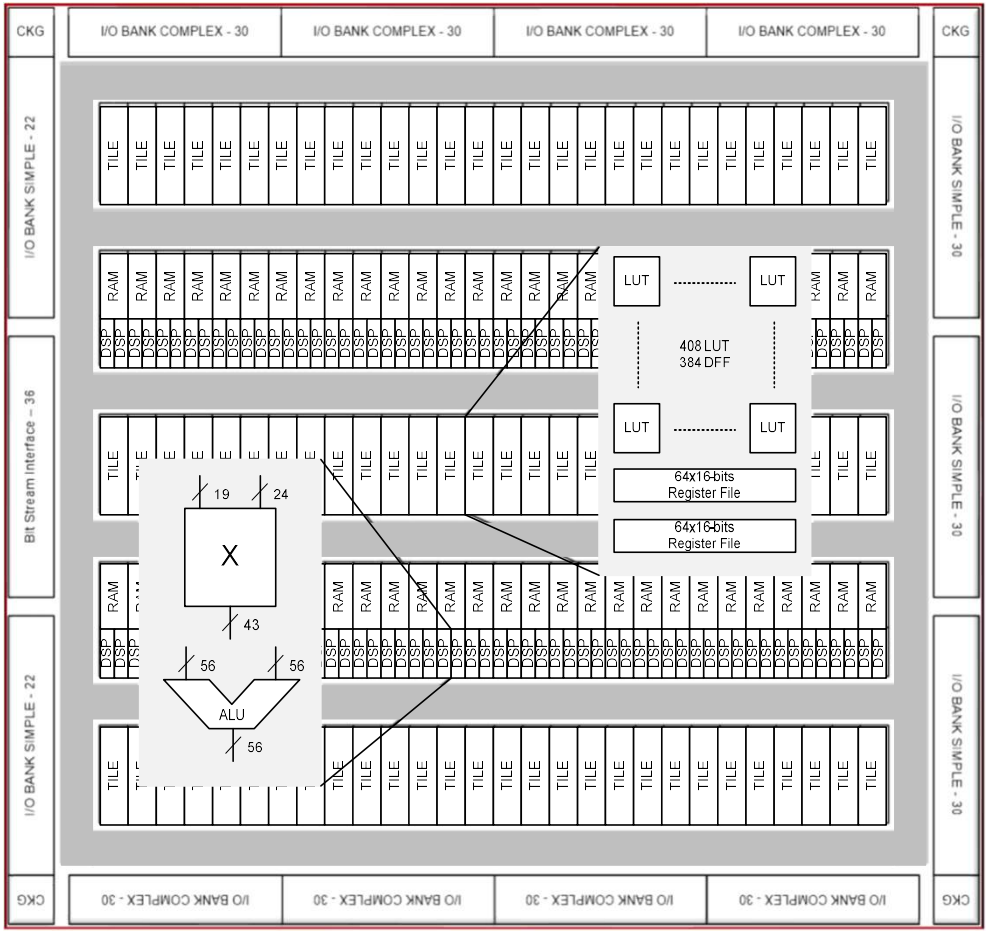


NG medium - Companium Chip

- NG-MEDIUM is ideally a Companion Chip
  - *FPGA companion chips expand the capabilities of embedded host processors by adding missing host features and by offloading high-speed processing tasks.*
  - *FPGA provides the ideal platform to add custom features tailored to specific project needs and much of the design can be re-used to support multiple processors.*



NG medium Overview



V_{core} : 1,2V - V_{IO}: 1,5 or 1,8 or 2,5 or 3,3V - $V_{AuxAnalog}$: 2,5V (I/Os, Comp, Thermal Sensors, …)

Device	Details	NX1H35S
Capacity		
ASIC Gates		**550 000**
Logic Modules	3x Tile + 2CGBs	
Register	384DFF*28*3rows	**32 256**
LUT-4	408LUT*28*3rows	**34 272**
Carry	96CY*28*3rows	**8 064**
Embedded RAM		**2,856Mb**
DPRAM	28RAM*2rows*48Kb	**2.688K**
Core Register File	28*2RF*3rows	**168**
Core Register File Bits	168*64*(16+6)bits	**168K with ECC**
Additional Features		
DSP Blocks	56*2rows	**112**
SpaceWire link I/F 400Mbps	CODEC	**1**
High-Speed Serial Link 6,25Gbps	SERDES Tx/Rx	**0**
Hard IP Processor core	ARM Cortex R5	**0**
Clocks	4 CKG * 6 CCK	**24**
Inputs / Outputs		
I/O banks	8 Complex + 5 Simple	**13**
DDR PHY (11 IOBs)	2x / Bank Complex	**16**
SpaceWire PHY (8 IOBs)	2x / Bank Complex	**16**
Packages – User I/Os		
LG625 & CG625	29*29mm / 1mm	**374**
CQ352	48*48mm / 0,5mm	**192**
FG625 (Jun18)	27*27mm / 1mm	**374**

N	X	1	H	3	5			S		-		C	Q	3	5	2		V	

NG medium - Power consumption

- Static Power consumption depends of I/O configuration
- Dynamic Power consumption depends of the design
  - % of FPGA resources usage
  - Operating frequency

    ➔ Finally the power consumption is 0,50 µW/MHz/LUT+DFF

- What about NG medium ?

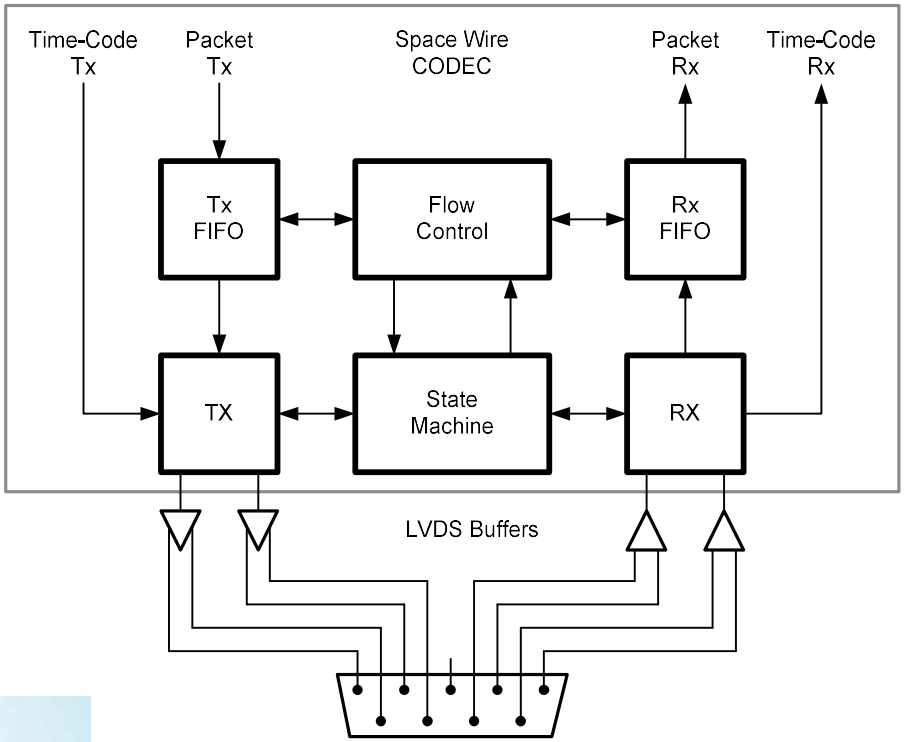
➢ Quiescent VDDcore supply current is
/ 2 versus Antifuse FPGA
/ 2 versus Flash-based FPGA
/ 30+ versus biggest RHBD Sram-based FPGA

Symbol	Parameter	Min	Typ	Max	Unit
IDD1V2	Quiescent* Core supply current	TBD	170	295	mA
IDD2V5A	Quiescent* VDD2V5A supply current	-	251	-	mA
IDD_SER	Quiescent* VDD_SERVICE supply current	TBD	20	TBD	mA

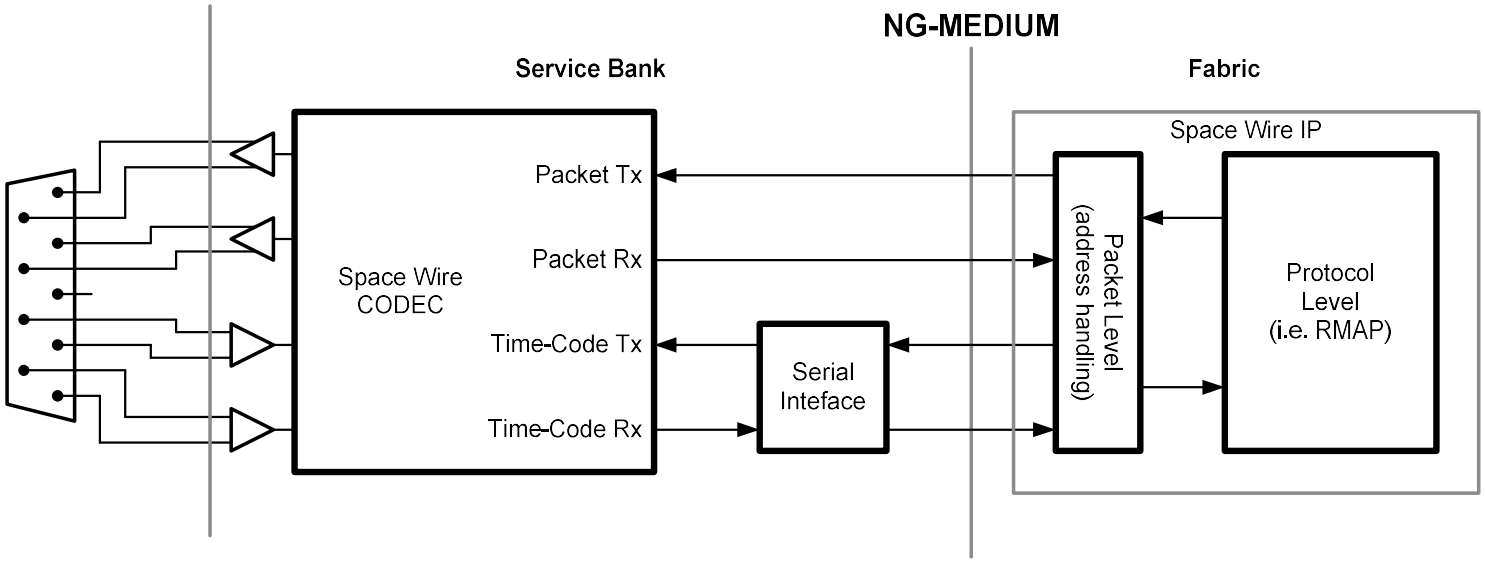
Quiescent current is measured when the chip is turned on in safe-config mode without any design.

NG medium - SpaceWire CODEC

- NG-MEDIUM includes **1x Space Wire CODEC**
- Two mode of operation:
  - bitstream download
  - User application
- Full hardware implementation
- Up to 430Mbps
- Standard common mode LVDS buffers

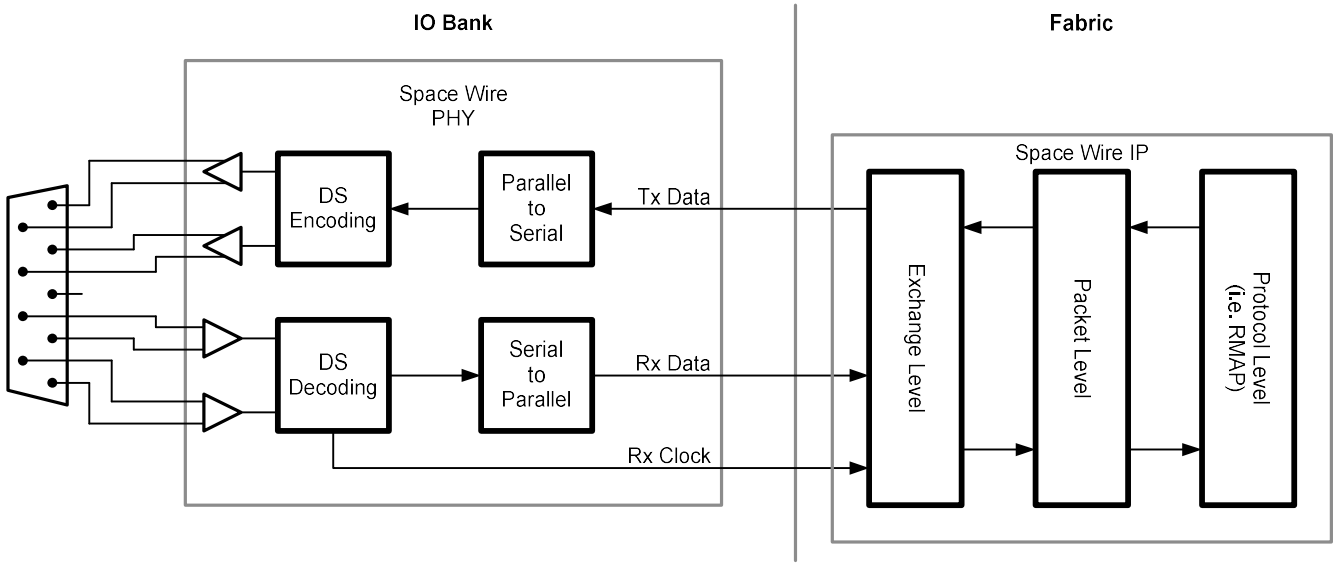


NG medium - SpaceWire CODEC in User Appls



- Packet Level transmits address, cargo and end_of_packet
- The soft IP implemented in the fabric can handle addressing and different protocols
- Time code and control signals are accessed through a serial interface

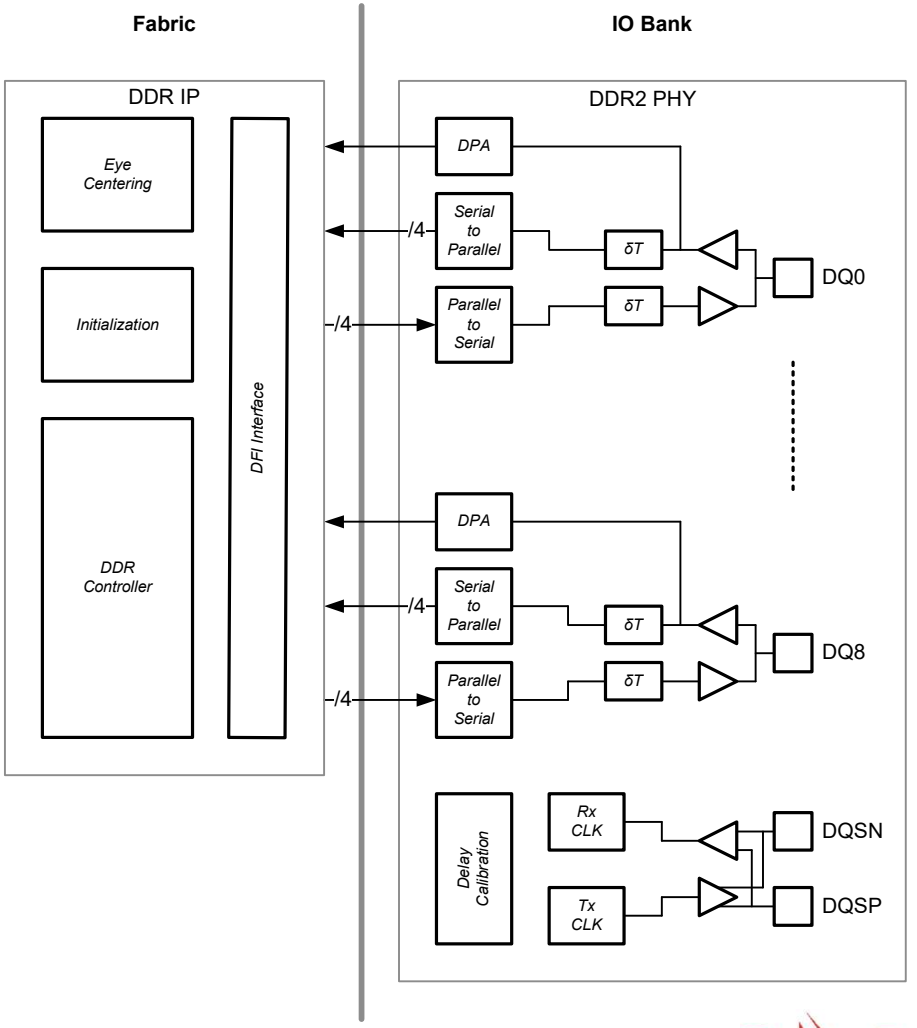
NG medium - SpaceWire Physical Interfaces



- The NG-MEDIUM includes **16 SW-PHY**
- Clock recovery and data sampling up to 430Mbps
- 10 bits parallel to serial interface
- The soft IP shall implement the exchange and packet level
- Can be used to implement various protocol (RMAP, switch)

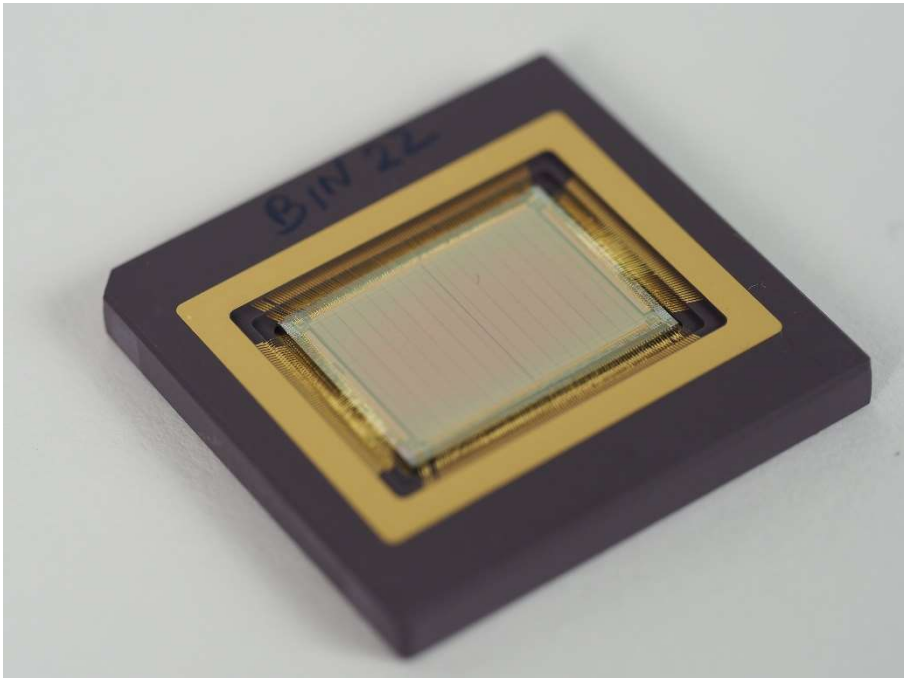
NG medium - DDR interface

- NG-MEDIUM includes **16 DDR/DDR2 PHY** (physical interfaces)
- The PHY includes the hardware to implement DDR transmission and reception up to 800Mbps
  - SSTL15/18/25 buffers
  - Differential DQS
  - Mixed analog / digital delay lines
  - Dynamic Phase Alignment sensor
  - DDR clock recovery
  - Delay Calibration
  - 4-bits serial / parallel interfaces
- The DDR IP includes
  - a DFI compliance block
  - a state machines for eye centering and initialization
  - a DDR controller

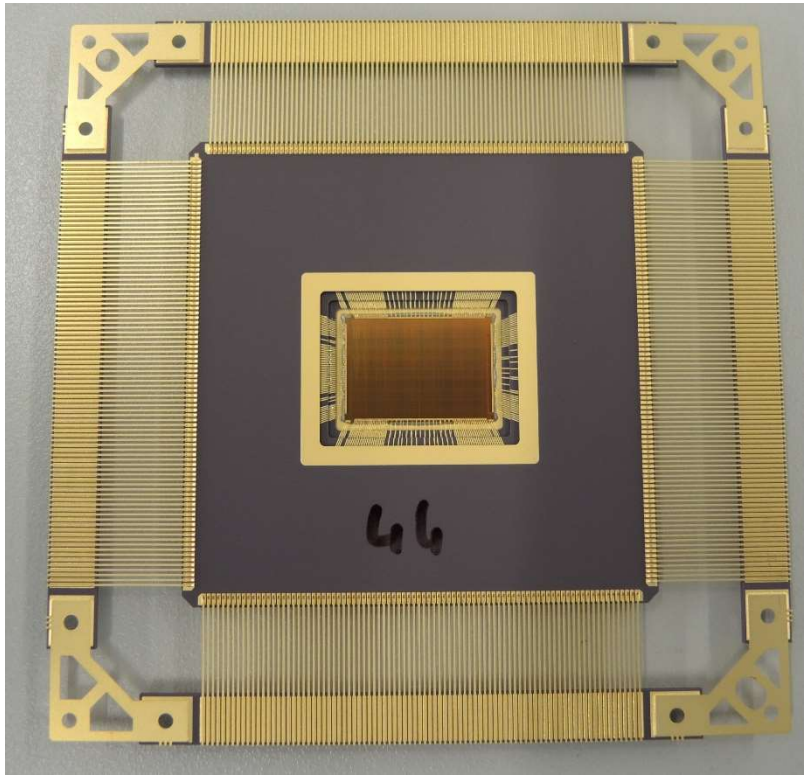


NG medium Packaging

LGA625
29*29mm body, 1,00mm pitch



MQFP352
48*48mm body, 0,50mm pitch

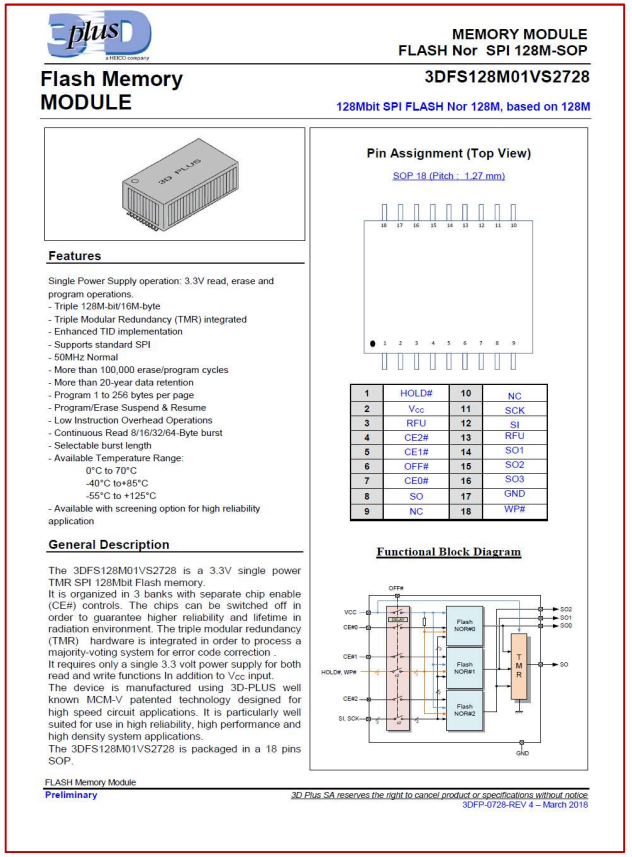


NG medium Bitstream Size

- This NX1H35S bitstream size depends on the application size (configuration) and the number of user Core RAM and Core Register Files to be initialized.
  - Maximum configuration (100%): 6.46Mb
- The maximum bitstream size is 6460 + 56 x 96.06 + 168 x 3.03 = **12210Kb**
  - So, it would require 3x NVRAM 4Mb or 1x NVRAM 16Mb.
- Configuration download would me 240ms maximum with Flash SPI @ 50MHz.
- Most applications do not require to initialize all memories. A typical bitstream is less than 8Mb.
  - These figures are just estimations. The actual size can be determined only by running the mapping software.

Bitstream Download: Cfg Memory

- Recommended Space FPGA Configuration Memory
  - 3D-PLUS Serial NOR Flash TMR'ed 128Mb / 3DFS128M01VS2728
    - 128Mbit SPI FLASH Nor
    - Single Power Supply operation:
      (3.3V read, erase and program operations).
      - Triple 128M-bit/16M-byte
      - Triple Modular Redundancy (TMR) integrated
      - Enhanced TID implementation
      - Supports standard SPI
      - 50MHz Normal
      - More than 100,000 erase/program cycles
      - More than 20-year data retention
      - Program 1 to 256 bytes per page
      - Program/Erase Suspend & Resume
      - Low Instruction Overhead Operations
      - Continuous Read 8/16/32/64-Byte burst
      - Selectable burst length
      - Available Temperature Range:
        0° C to 70° C
        -40° C to +85° C
        -55° C to +125° C



plusD

MEMORY MODULE
FLASH Nor SPI 128M-SOP

Flash Memory MODULE

3DFS128M01VS2728

128Mbit SPI FLASH Nor 128M, based on 128M

Features

Single Power Supply operation: 3.3V read, erase and program operations.
- Triple 128M-bit/16M-byte
- Triple Modular Redundancy (TMR) integrated
- Enhanced TID implementation
- Supports standard SPI
- 50MHz Normal
- More than 100,000 erase/program cycles
- More than 20-year data retention
- Program 1 to 256 bytes per page
- Program/Erase Suspend & Resume
- Low Instruction Overhead Operations
- Continuous Read 8/16/32/64-Byte burst
- Selectable burst length
- Available Temperature Range:
  0°C to 70°C
  -40°C to+85°C
  -55°C to +125°C
- Available with screening option for high reliability application

General Description

The 3DFS128M01VS2728 is a 3.3V single power TMR SPI 128Mbit Flash memory.
It is organized in 3 banks with separate chip enable (CE#) controls. The chips can be switched off in order to guarantee higher reliability and lifetime in radiation environment. The triple modular redundancy (TMR) hardware is integrated in order to process a majority-voting system for error code correction .
It requires only a single 3.3 volt power supply for both read and write functions In addition to Vcc input.
The device is manufactured using 3D-PLUS well known MCM-V patented technology designed for high speed circuit applications. It is particularly well suited for use in high reliability, high performance and high density system applications.
The 3DFS128M01VS2728 is packaged in a 18 pins SOP.

Pin Assignment (Top View)

SOP 18 (Pitch : 1.27 mm)

1	HOLD#	10	NC
2	Vcc	11	SCK
3	RFU	12	SI
4	CE2#	13	RFU
5	CE1#	14	SO1
6	OFF#	15	SO2
7	CE0#	16	SO3
8	SO	17	GND
9	NC	18	WP#

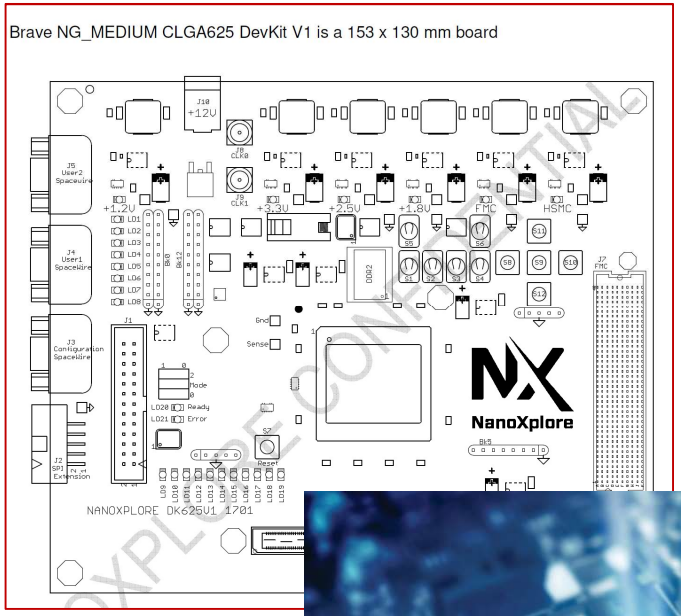
Functional Block Diagram

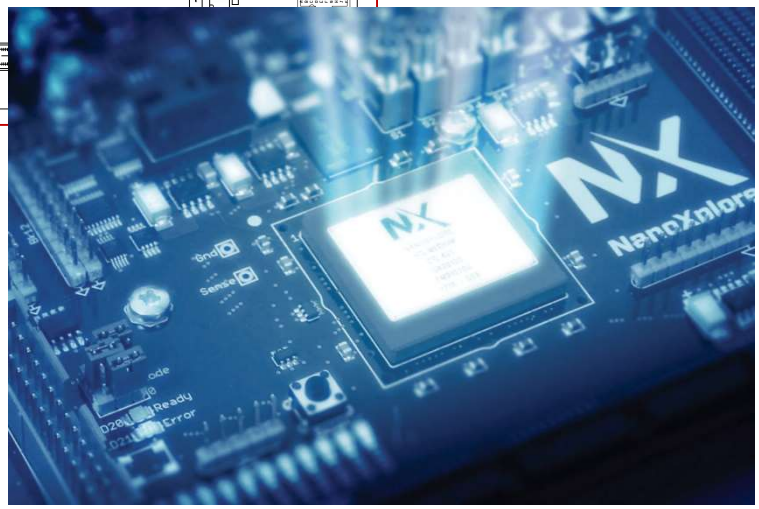
FLASH Memory Module
Preliminary

3DFP-0728-REV 4 – March 2018

- Programmable Clock 50MHz ÷ n

NG medium Evaluation Kit





- The DevKit is an evaluation board to be used interactively through
  - **JTAG**, or
  - standalone from a **EEPROM board.**
- The board configuration mode is thus selected by <u>on-board jumpers</u>.
- A 10-pin HE10 connector is provided to receive an EEPROM memory board (Atmel Dump Mode **EEPROM** or standard **SPI EEPROM**).
- An optional SpaceWire connector allows **SpaceWire** configuration.

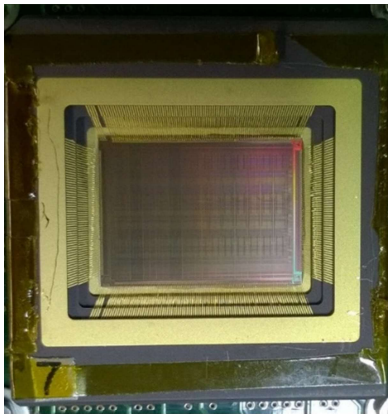
RADIATIONS
SEE campaigns

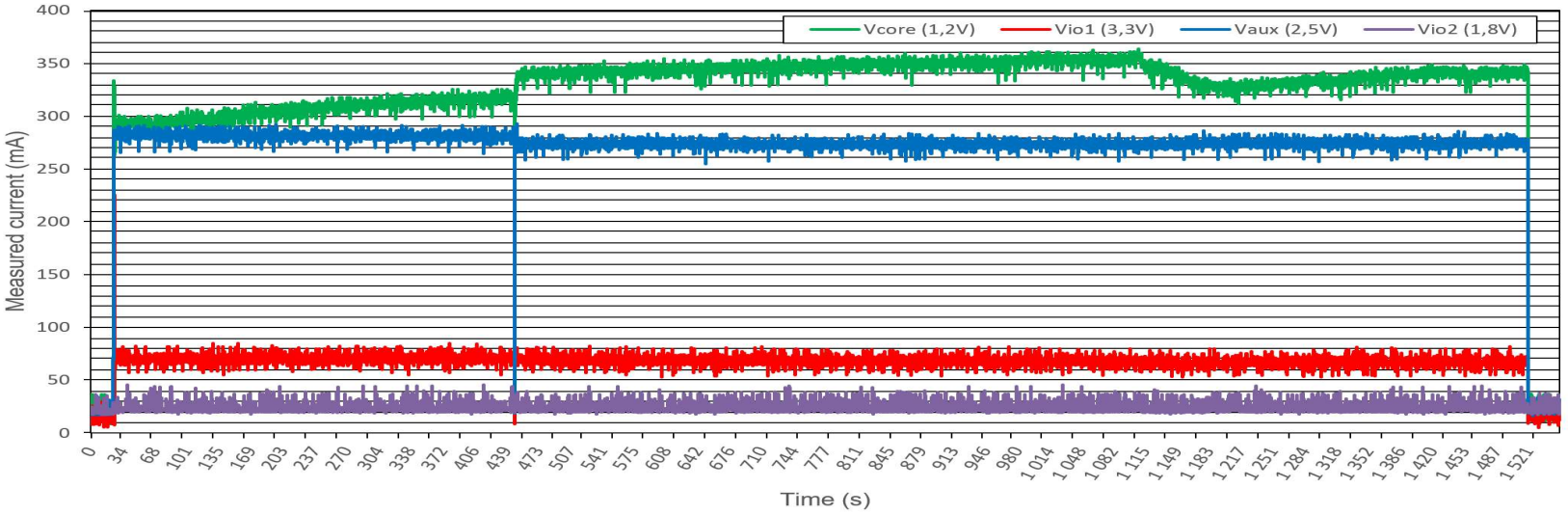
- 4 SEE campaigns done in Q4CY16 and Q4CY17
  - **OCT & NOV16**:
    - 2 UCL/HIF campaigns,
    - 1st silicon, packaged in LGA625,
    - Static & Dynamic SEU/SET/SEFI testing.
  - ***NOV17***:
    - PSI/PIF campaign
    - Latest silicon, packaged in LGA625.
  - ***DEC17***
    - UCL/HIF campaign,
    - Latest silicon, packaged in LGA625,
    - Full SEE testing (SEL/SEU/SET/SEFI)

Radiations

SEL testing

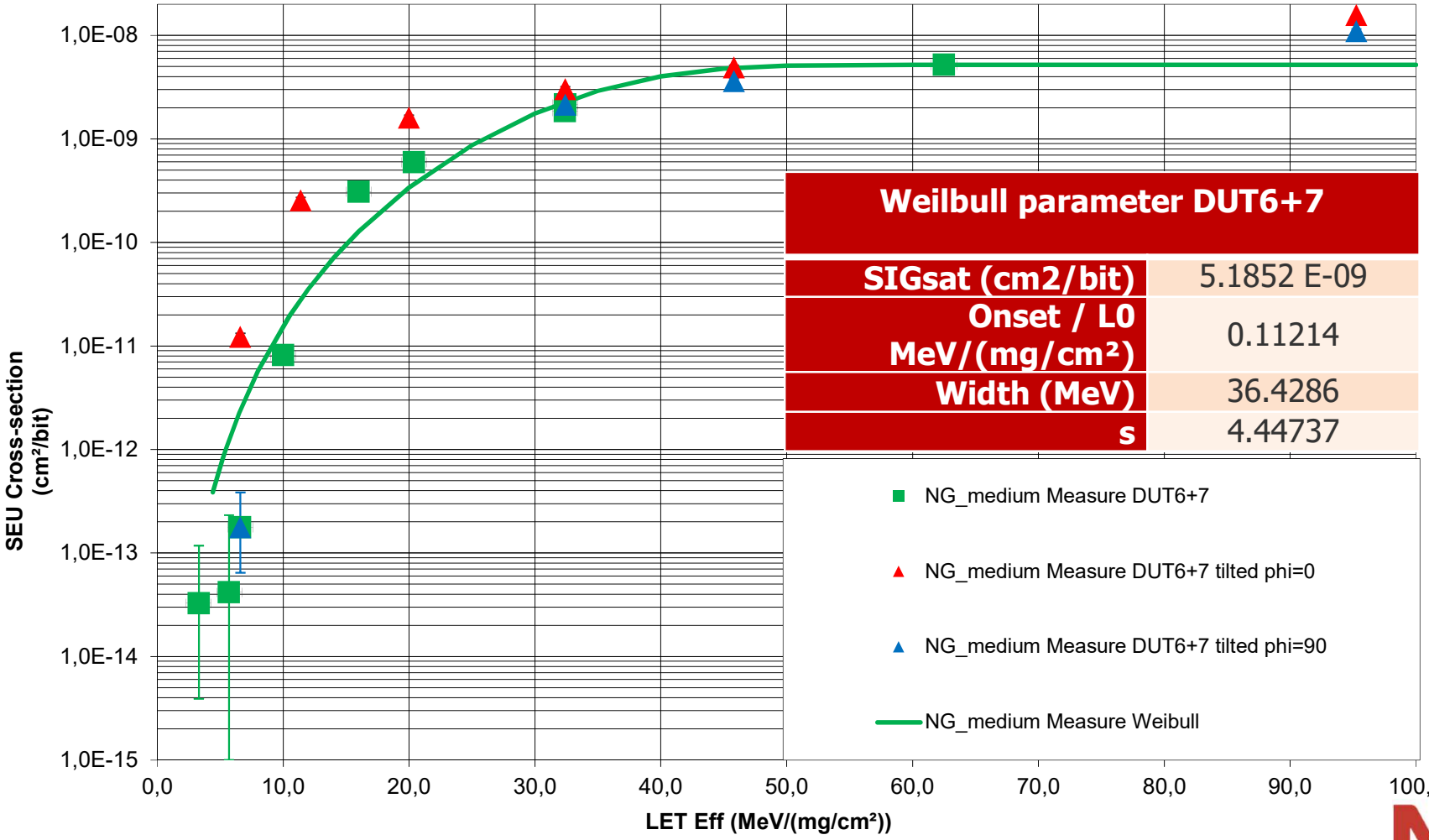
- Temperature 100° C, regulated by PID controller,
- Supply at their max value (+10%),
  - VDD1V2: 1.32V
  - VDD3V3: 3.63V
  - VDD2V5: 2.75V
  - VDD1V8: 1.98V
- Fluence over 10^7 p/cm-² with the highest LET $^{124}Xe^{35+}$
- NO LATCH-UP event was detected during the test period.





Heavy-Ions

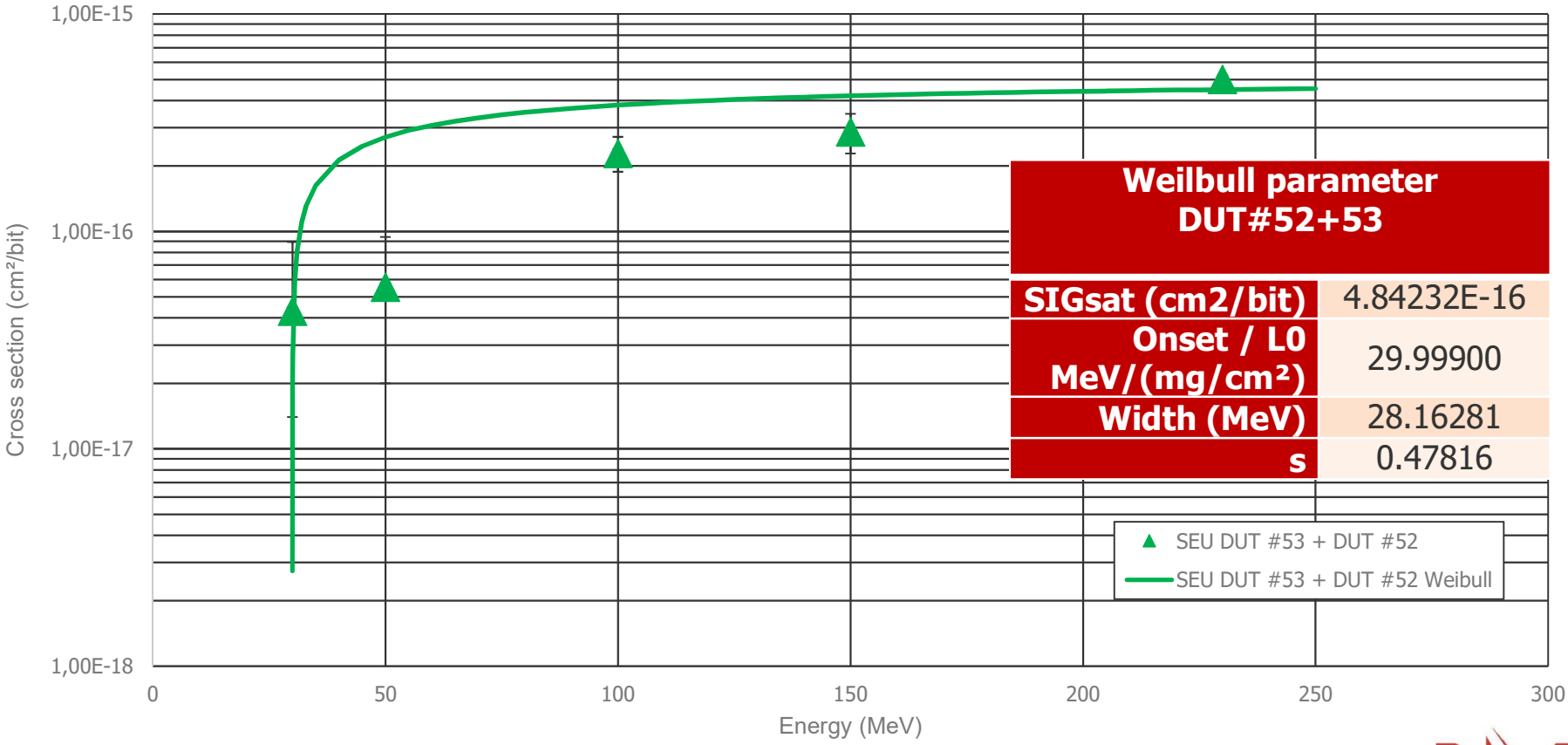
Cfg Memory Xsection



Protons

Cfg Memory Xsection

- Xsection confidence intervals of 95% (alpha = 5%) are calculated for:
  - Relative fluence uncertainty of PSI is δF/F = 5%.



NG medium Orbital Upset Rate

HEAVY IONS Weilbull	
SIGsat (cm2/bit)	5.1852 E-09
Onset / L0 (MeV/(mg/cm²))	0.11214
Width (MeV)	36.4286
s	4.44737

PROTONS Weibull	
SIGsat (cm2/bit)	4.84232 E-16
Onset / L0 MeV/(mg/cm²)	29.99900
Width (MeV)	28.16281
s	0.47816

- Orbital Upset Rate calculation (CREME 96 model, OMERE software):
  - Solar min, AE8 electron model, AP8 proton model,
  - shielding = 100mils
  - sensitive volume thickness = 2µm

Mission profile	SER (bit/day)	SER (chip/day)
GEO (35870km)	2,05E-10	1,26E-3
MEO (1000km 26768km, 63,4°)	1,30E-09	7,98E-3
LEO1 Pol (800km, 800km, 98°)	2,57E-09	1,58E-2
LEO2 ISS (400km, 400km, 51,5°)	3,06E-10	1,88E-3

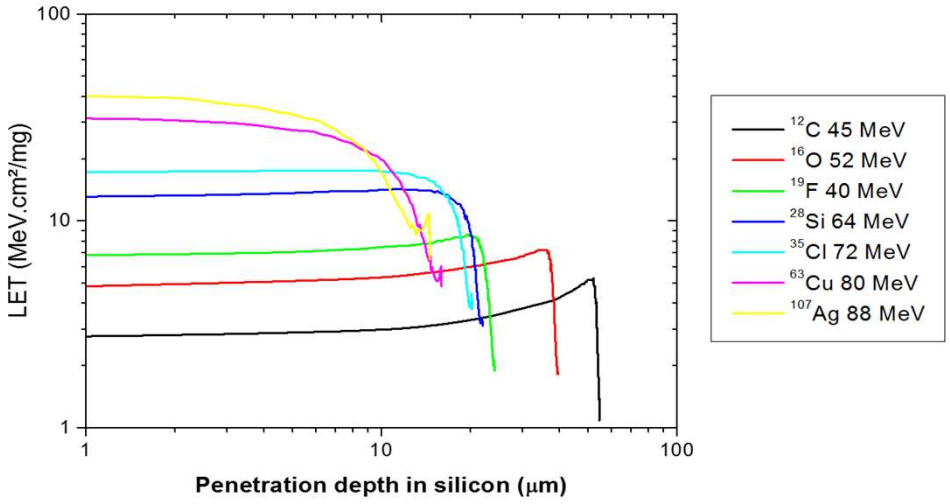
- Outside of CMIC
  - Which will correct 98% of Single Errors.
- Only a small fraction of NX FPGA memory cells are used

Less than 10%

of configuration bits used in typical design

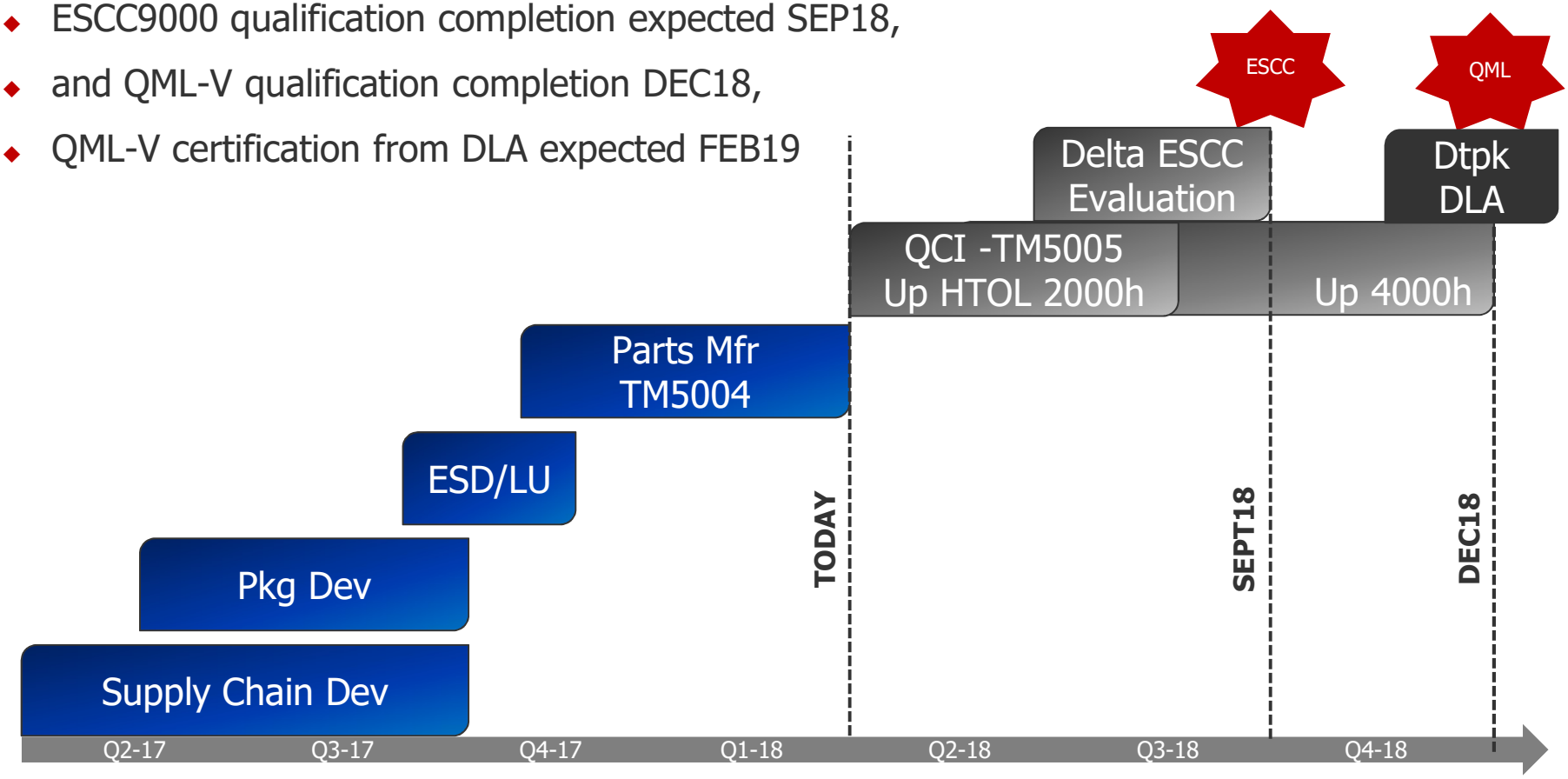
Next SEE Campaigns

- Neutrons SEE testing of PicoSkyFT design at ISIS / ChipIR by Skylabs and University of Maribor (Si), — Apr-18
- Heavy ions campaigns to be performed by UFRGS (Br), — May-18
- 4th UCL/HIF campaign to be performed ourselves, — Jun-18
- New Radiation campaign, expected from CERN at PSI & CHARM, — H2-2018
- New Radiation campaign, expected from CTI (Br) — H2-2018
  - TID (^{60}CO & X
  - Heavy Ions
  - Protons
  - Neutrons



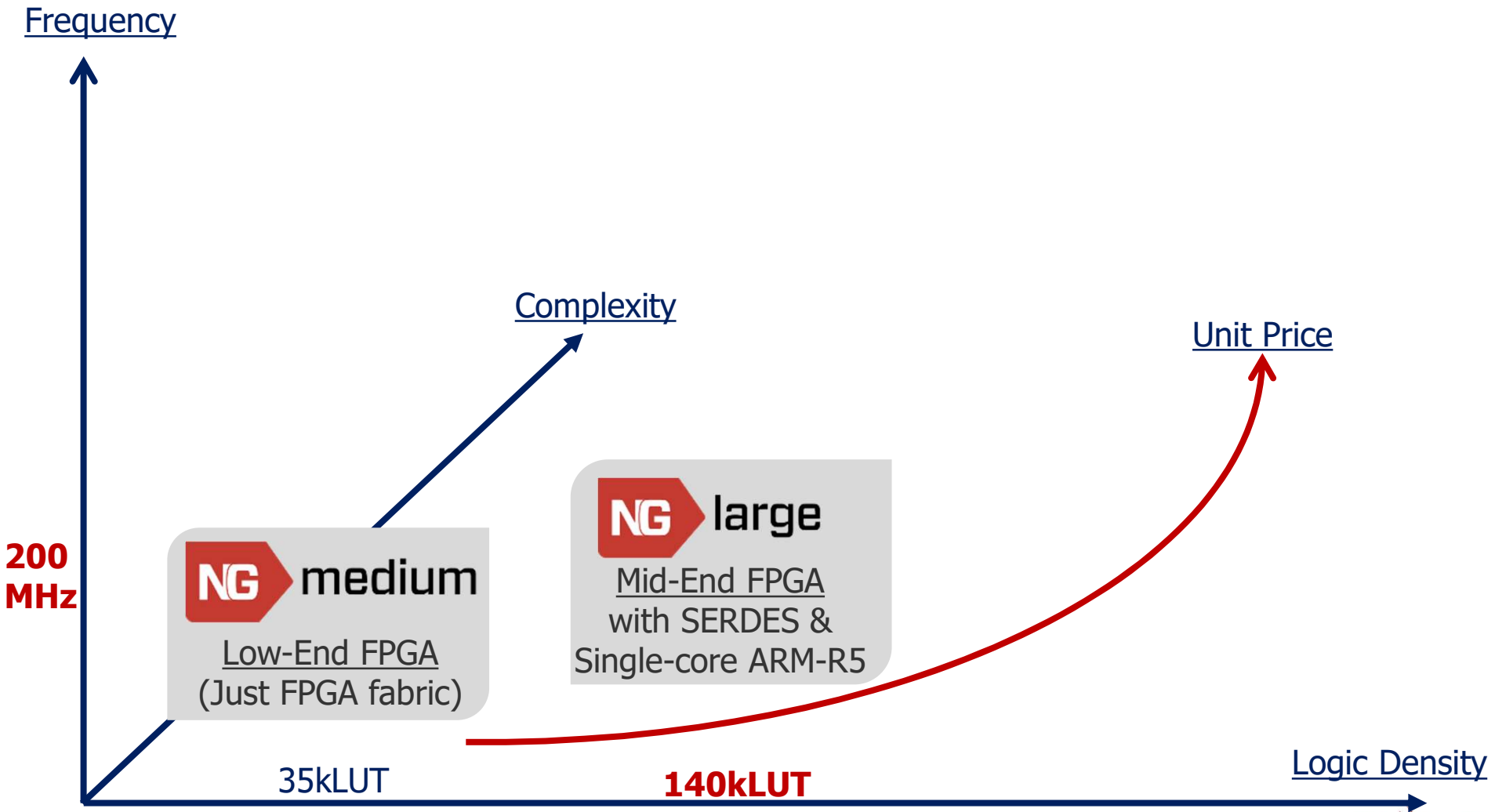
NG medium Space Qualification

- Space Qualification is running at STM on both CQFP-352 & LGA-625,
- ESCC9000 qualification completion expected SEP18,
- and QML-V qualification completion DEC18,
- QML-V certification from DLA expected FEB19



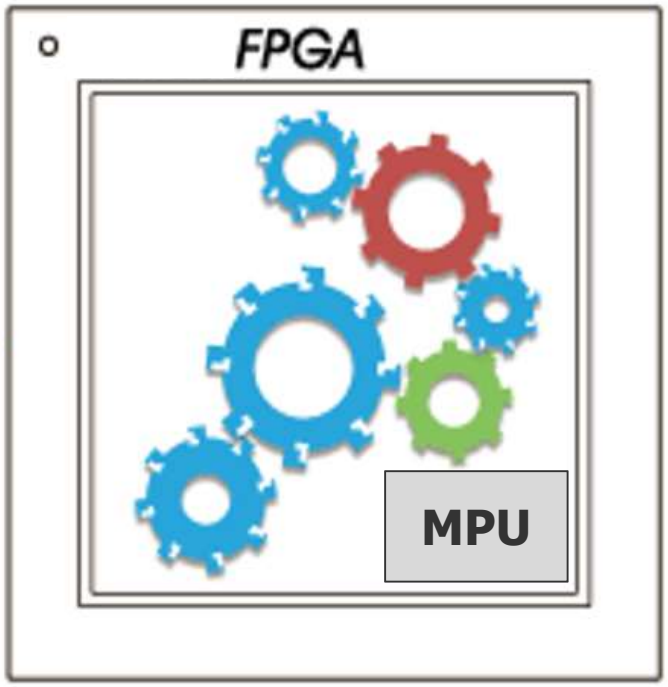
NanoXplore Rad-Hard FPGA Roadmap

Step2 – NG-Large

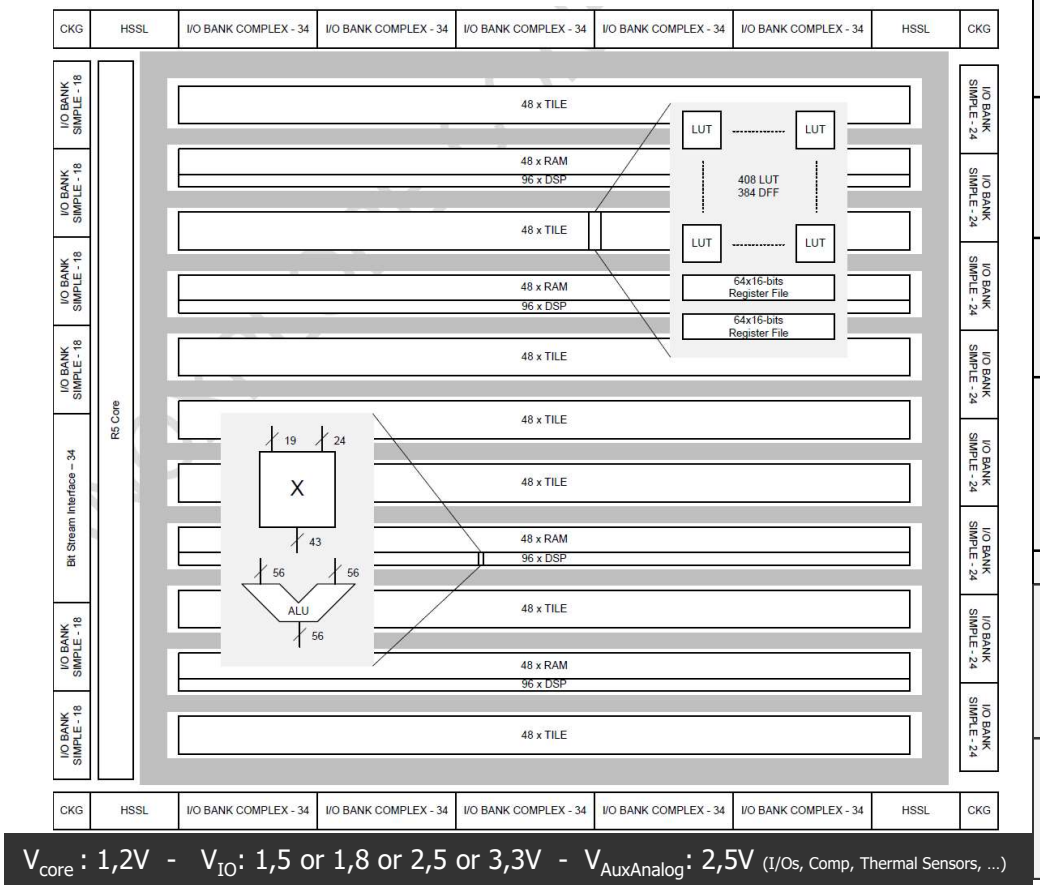


NG large - with Embedded Processor

- NG-Large replaces both MPU + Companion Chip
  - **4x density vs NG-Medium**
  - Thanks to World-Wide recognized ARM Cortex-R5, optimized for High-Performance, Hard Real-Time applications.



NG large Overview

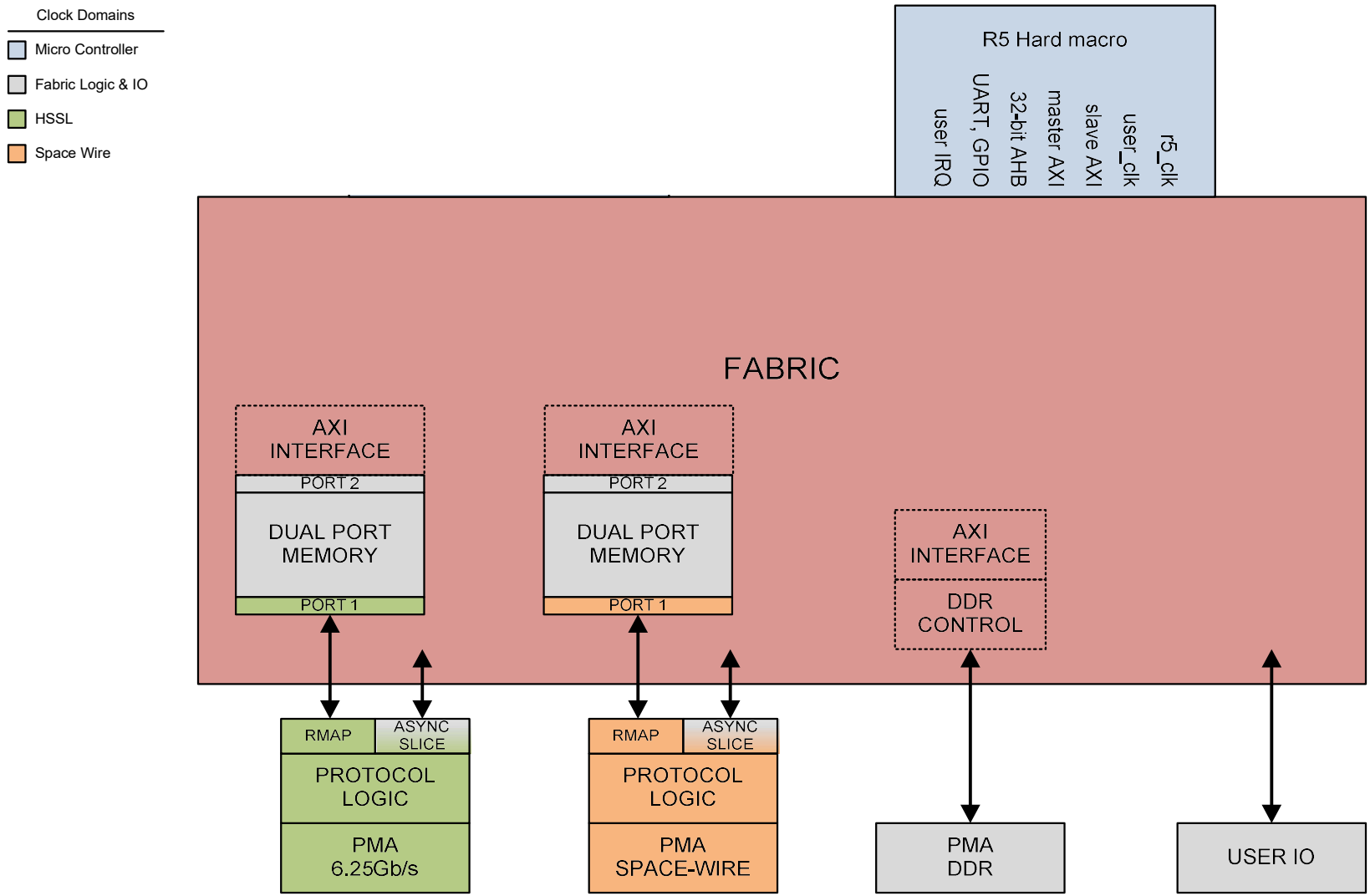


V_{core} : 1,2V - V_{IO}: 1,5 or 1,8 or 2,5 or 3,3V - $V_{AuxAnalog}$: 2,5V (I/Os, Comp, Thermal Sensors, ...)

Device	Details	NX1H140
Capacity		
Equivalent System Gates		**15 000 000**
ASIC Gates		**1 900 000**
Logic Modules	7x Tile + 4CGBs	
Register	384DFF*48*7rows	**129 024**
LUT-4	408LUT*48*7rows	**137 088**
Carry	96CY*48*7rows	**32 256**
Embedded RAM		**9,888Mb**
DPRAM	48RAM*4*48Kb	**9.216K**
Core Register File	48RF*2*7rows	**672**
Core Register File Bits	672*64*(16+6)bits	**672K with ECC**
Additional Features		
DSP Blocks	96DSP*4rows	**384**
SpaceWire link I/F 430Mbps		**1**
SERDES Tx/Rx 6,25Gbps	4 Hex x 6 SERDES	**24**
Hard IP Processor core	ARM Cortex-R5	**1**
Clocks	4 CLK * 8 CCK	**32**
Inputs / Outputs		**-**
I/O banks	10 Complex + 14Simple	**24**
DDR PHY (11 IOBs)	2x / Bank Complex	**20**
SpaceWire PHY (8 IOBs)	2x / Bank Complex	**20**
Packages - User I/Os		
LG1752 & CG1752	42,5*42,5mm / 1mm	**684**
FF1752	42,5*42,5mm / 1mm	**684**
FF1152 (TBC)	35*35mm / 1mm	**TBD**

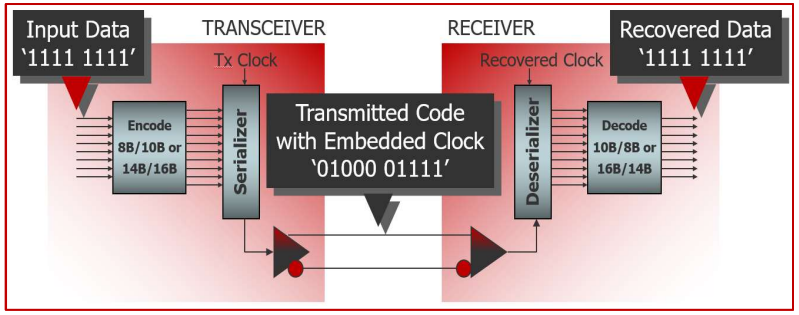
N	X	1	H	1	4	0	T	S	P	-	1	L	G	1	7	5	2	Q	

NG large Architecture



NG large - HSSL overview

- SERDES developed in C65 Space, acc. VELOCE contract,
- Take into account Space requirements, (esp JESD204B, SpF, …),
- 0.70 – 6.25 Gbps data rate,



- NG-Large will embed 4 Hex SERDES= **24 HSSLs.**
- Hex architecture:
  - HSSL blocks provide multi-protocol high-speed serial link capability with multi-rate support.
  - Hex HSSLs are composed of 6 RX/TX lanes, a PLL, and a calibration circuit.
  - Each transceiver lane includes the PMA and PCS hard macros.
  - The SERDES block has configurable features such as data width (up to 80 bits in parallel), equalization and protocol dependent properties.
- HSSL supported protocols:

Protocol	Type	Encoding
ESIstream	3,125 – 6,25Gbps	14B/16B
Serial RapidIO	3,125 – 6,25Gbps	8B/10B
JESD204B	3,125 – 6,25Gbps	8B/10B
SpaceFibre	3,125 – 6,25Gbps	8B/10B

NG large Bitstream Size

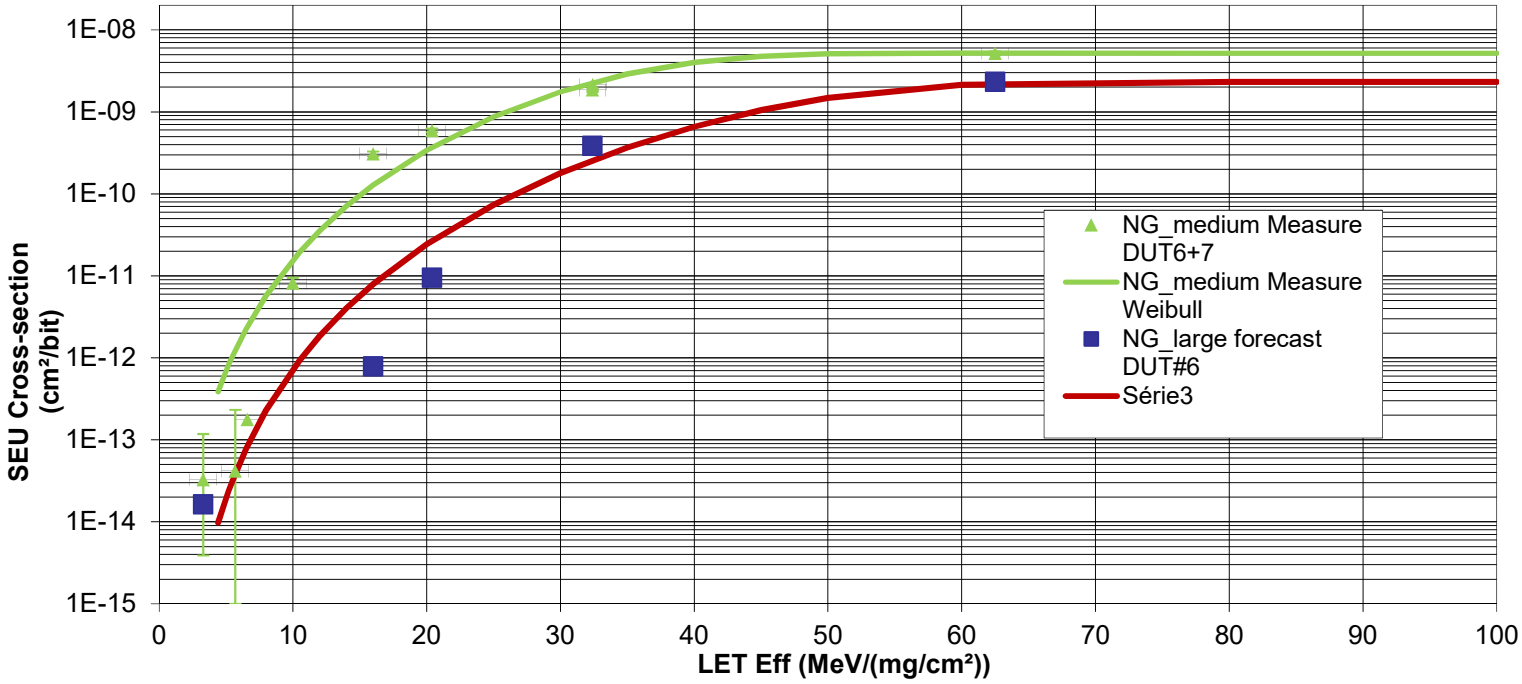
- This NX1H140TSP bitstream size depends on the application size (configuration) and the number of user Core RAM and Core Register Files to be initialized.
  - Maximum configuration (100%): 26.46Mb
- The maximum bitstream size is 26458 + (192 x 96.06) + (672 x 3.03) = **46938Kb**
  - So, it would require 3x NVRAM 16Mb or 1x NVRAM 64Mb.
- Configuration download would me 118ms maximum with Flash QSPI @ 100MHz.
- Most applications do not require to initialize all memories. A typical bitstream is less than 32Mb.
  - These figures are just estimations. The actual size can be determined only by running the mapping software.

NG large Cfg Memory Xsection

Weibull parameter	
SIGsat (cm2/bit)	2.32E-09
L0 (MeV/(mg/cm²))	0.42243
W (MeV)	49.42755
s	4.91666

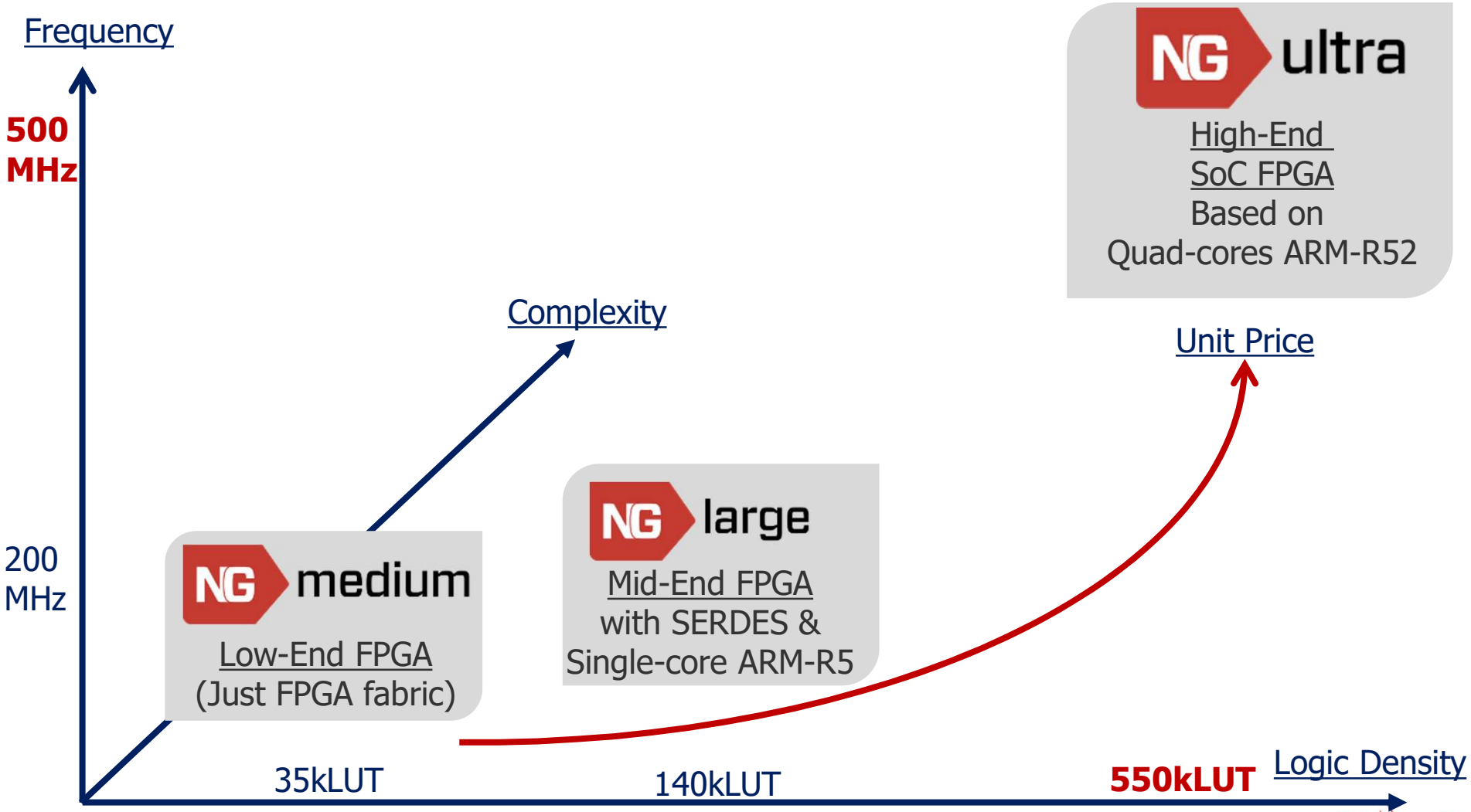
Configuration Memory SEU @ 25°C, VDDmin	SER
SEU/config/day	**8.26E-13 SEU/config/day**
SEU/chip/day	2.03E-05 SEU/chip/day
SEU/chip/year	7.4E-03 SEU/chip/year ➔ SER > 100years

NG-Large forecast of Config SEU cross-section(LET)



NanoXplore Rad-Hard FPGA Roadmap

Step3 – NG-Ultra



NG ultra SoC FPGA

- NG-Ultra becomes a System-On-Chip
  - **4x FPGA density vs NG-Large**
  - Full SoC architecture based on Quad-core ARM Cortex-R52, again optimized for High-Performance. Hard Real-Time applications.

SoC definition: It includes an Embedded Processor + Logics & RAM blocks, even analog circuitry.
Benifits: Reducing form factor, power consumption, heat dissipation, analog mixed signal integration

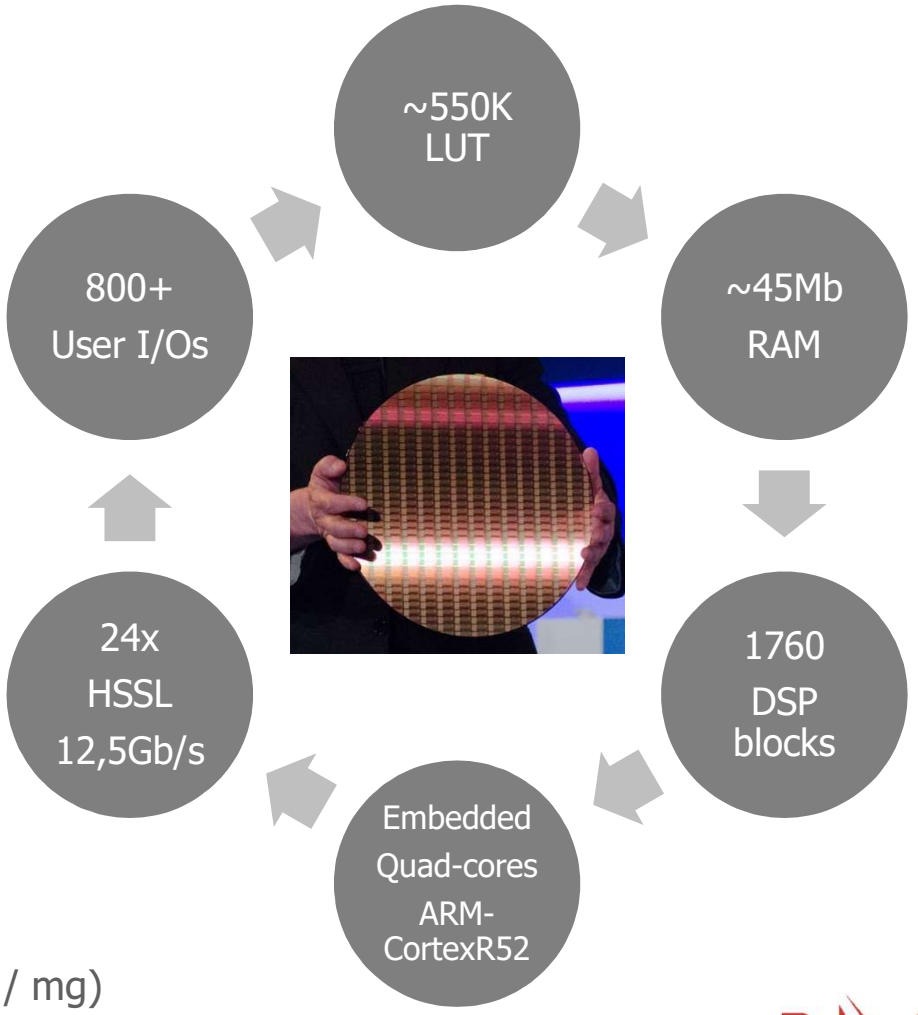
NG ultra 1st RH 28nm FPGA

1st **Rad Hardened**

SoC

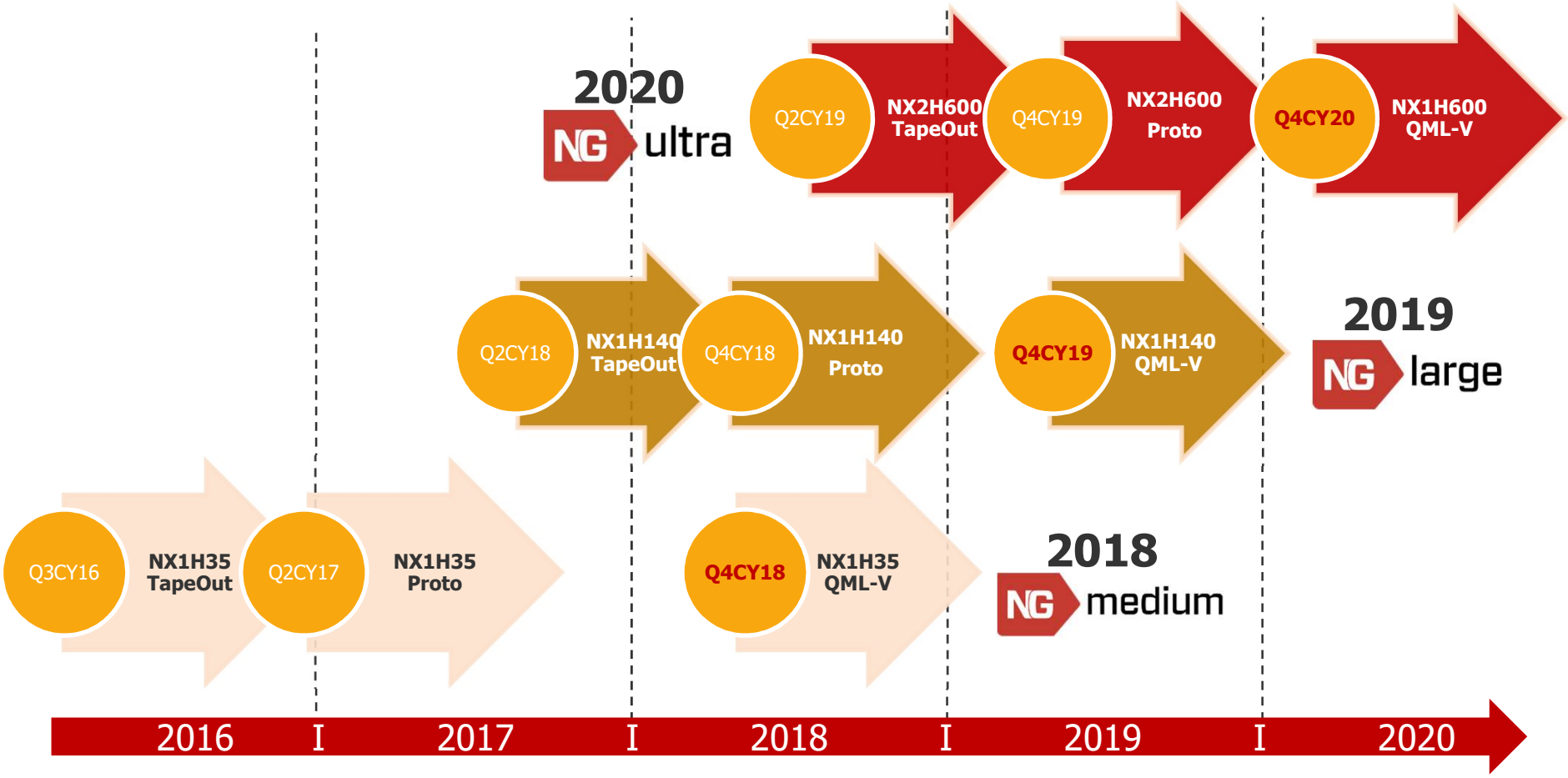
High-End FPGA

- Performance:
  - Logic: **500MHz**
  - DSP: 800MHz
  - Diff I/O: 1Gbps
  - SerDes: 12.5Gbs
  - ARM R52: **600MHz**
- ECSS Class-1 qualification
- Hardening performance
  - Fully hardened by design
  - Fully SEU immune up to 60 MeV-cm2 / mg
  - Total dose > 50 Krads TID
  - No single event latch up (LET>60 MeV-cm2 / mg)



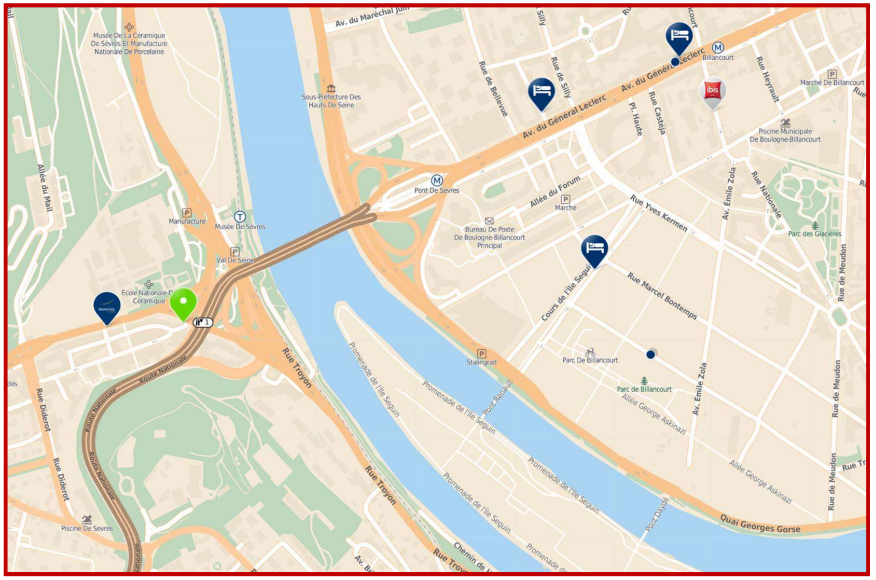
NX FPGA Schedule

One Qualified Radiation Hardened FPGA device every year from 2018



Conclusion

Thank you



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