From eFPGA cores
to
RHBD System-On-Chip FPGA

4th SEFUW – ESA/ESTEC Noordwijk (NL) – 9/11apr18
NanoXplore Overview

- **Created in 2010** by three veterans of semiconductor industry with long experience in the design, test and debugging of FPGA cores.
- **Fabless** semiconductor company headquarter in France
- R&D engineers in two offices in France:
  - Sèvres: Hardware developments
  - Montpellier: Software developments
- NanoXplore is a leader in the design of large scale programmable logic arrays for state of the art FPGA cores
- The company is focusing on 2 main activities:
  - Offer hard block embedded FPGA core IP (NX-eFPGA)
  - Developing rad-hard FPGA qualified for space applications (from BRAVE contract)
NanoXplore - FPGA architecture

- 1st of all, hereafter a basic FPGA architecture

- 2nd, there are 4 different ways to do interconnection:
  - Antifuse
  - Flash-based
  - Std 6T-cell SRAM
  - RHBD 12T/16T-cell SRAM
FPGA market and Main Vendors

FPGA TAM
~$6.50B
Xilinx, Intel PSG, Microsemi, Lattice

Aerospace & Defense FPGA TAM
~$1.00B
Xilinx, Intel PSG, Microsemi

Space FPGA TAM
~$0.23B
Xilinx, Microsemi
(source ESA)

Source: Grand View Research Dec 2016
FPGA market and Main Vendors

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~$6,50B
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Space FPGA TAM
~$0,23B
Xilinx, Microsemi + (source ESA)

Source: Grand View Research Dec 2016
NanoXplore – From eFPGA to RH FPGA

- NX has a **strong experience** in developing eFPGA cores on the most advanced technology nodes.
- **Hi-rel** markets (like space) require specific features (hardening, reliability, security etc) which are **not well addressed by market leaders** due to limited market opportunity: **Not true for NX**.
- European funding to support that initiative: **CNES, ESA, EC, DGA, DGE, BPI** ...
- **Space market** has many synergies with additional market such as Avionic, Military, Railway and Medical, even Automotive
  - Limited competition and clear technology advantages.

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Export Regulation

- NX RH FPGA devices are **ITAR & EAR-free** ➞ No Dependance to USA.
- Classified 3A001.a.2.c according (EC)2015/2420 rules.

<table>
<thead>
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<th>US Dep’t. of Commerce</th>
<th>US Department of State</th>
<th>US Department of Treasury</th>
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<td>Office of Foreign Assets Controls</td>
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<td>International Traffic in Arms Regulations</td>
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<td>Commerce Control List</td>
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</table>
Process Technology
High Performance vs Low Power

- Chip designers are challenged to choose between
  - Standard processes to meet performance goals or
  - Low Power processes to meet power goals.

- Parts designed for a fixed supply voltage and manufactured in the FF corner will have
  the highest frequency, have the most leakage and provide the best performance.

- Parts manufactured in the SS corner will have the slowest performance and have the
  least leakage and consume the least power.
Process Technology

STM C65 SPACE Low Power

Features

Process
- ST/Microelectronics C65SPACE (65nm CMOS)
- 3.3V IO gate oxide GO2 (5nm)
- 1.2V core gate oxide GO1 (1.9nm), triple VT transistors
- 7 copper metallization, 5 thin and 2 thick
- Low-K inter-metallic dielectrics for thin metal layers
- High density SRAMs
- Compatible with flip-chip and wire bonding packaging

Radiations
- SEL-free up to LET = 60MeVcm^2/mg at 125°C Tj and Vdd max
- SEE hardened library
- Tested up to a total dose of 300 krad (Si)

Reliability
- Library cells models with 20 years aging
- Transistor models including aging alteration
- ESD better than:
  - 2kV in HBM (Class 2 / MIL-STD-883H)
  - 150V in MM
  - 250V in CDM

Design flow
- An ST customized design flow (RTL to GDS) involving commercial solutions (Synopsys, Cadence, Mentor...) is available for partners and certified design houses:
  - Front-End kit from RTL to gates based
  - SiPkit for IO ring generation
  - FTK8 for place and route
  - SignOffKit for final verification before tape-out
- For customer owned tools (COT) flow, ST provides the C65SPACE design platform along with the DRM and sign-off kit.

Description
The C65SPACE is fabricated on a proprietary 65nm, 7 metal layers CMOS process intended for use with a core voltage of 1.2V ±0.10V.

The ST standard-cells, memories and PLL have been designed and characterized to be compatible with each other.

Library offer
- Comprehensive library of standard logic with P/V and aging corners models
- IO pad libraries provide interfaces at 3.3V +/-0.30V / 2.5V +/-0.25V and 1.8V +/-0.15V
- High speed IO Pad LVDS supplied at 2.5V +/-0.25V up to 650Mbps
- Cold spare ICs with single/double row support
- Memories generation: single port SRAM, ROM, Dual port SRAMs, BIST library, EDAC library
- Wide-range PLLs (1.2GHz with multi-phase outputs)
- 6.25Gbit/s high speed serial links (HSSL)
Process Technology

*STM C28 SPACE FD-SOI*

- FD-SOI substrates enable ultra-low-power features, unique cost/performance tradeoff, high-reliability and high-performance-mixed signal integration for a wide range of applications.

**Power and energy efficiency**
- Ultra low leakage, wide Body-Bias & operating voltage range

**Analog performance**
- for mixed signal & RF design

**Robustness**
- for mission critical applications

**Cost effective platform**

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Source: http://www.st.com/content/st_com/en/about/innovation---technology/FD-SOI/efficiency-at-all-levels.html

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NX FPGAs are Rad Hardened

All logic of NX FPGAs is hardened by design (RHBD) and simulated with TFIT software.

On top of it, Embedded Configuration Memory Integrity Check (“CMIC”)

- EDAC
  - Register File
  - DPRAM

- DICE
  - Cfg Memory
  - User Register
  - DFF

- TMR
  - Other Logic Cells (SKYROB)

- DMR
  - Clock Tree
    - Clock buffer
    - Matrix system
CMIC Overview

CMIC = Configuration Memory Integrity (= Scrubber Ctrl)

- The CMIC is an embedded engine performing automatic verification and repair of the configuration memory.

- The CMIC period can be set by the user.
- At 50MHz, the minimum period is 5.3 ms and the maximum 65 days.
- The configuration memory scan takes 4ms (+1.3ms delay).
- The CMIC reference memory is protected by ECC.
- The CMIC does not need to access the external NVRAM when performing checks and repairs at run time.
NanoXplore Rad-Hard FPGA Roadmap

2017

Low-End FPGA
(Just Logic, RAM & DSP)
- 35kLUTs / 3Mb RAM
- 112 DSP
- No HSSL
- No Hard IP Processor

NG-MEDIUM
(NX1H550FSP)

Mid-End FPGA
(+ SERDES & Processor)
- 140kLUTs / 10Mb RAM
- 384 DSP
- HSSL 6G
- Single-core ARM-R5
  (No Peripherals)

NG-LARGE
(NX1H100FSP)

High-End FPGA
(+ SoC architecture)
- 550kLUTs / 40Mb RAM
- 1760 DSP
- HSSL 12G
- Quad-core ARM-R52
  (Full SoC architecture)

NG-ULTRA
(NX4S50TSP)

2018

2019

2017                  2018                      2019

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NX RH FPGA products positioning

- **Performance FPGA x2**
- **Power Consumption / 4**
- **Lower SER**

**CURRENT MARKET**

- 65nm RH NG-MEDIUM
  - NX1H3SS (FR)
- 65nm RH NG-LARGE
  - NX1H40TSP (FR)
- 28nm RH NG-ULTRA
  - NX2H550TSP (FR)

- Performance FPGA x2
- Power Consumption / 4
- Lower SER
Programming Software: NanoXmap Overview

Diagram:

- Test bench
  - Simulation
  - FPGA library (.vhdl)
  - Simulation

- User HDL files
  - Creating project
    - Native.nxm
  - NanoXmap
    - Synthesize
      - Synthesized.nxm
    - Place
      - Placed.nxm
    - Route
      - Routed.nxm
    - Final design netlist (.vhd or .v) + Standard delay format (.sdf)
    - Bitstream
      - .nxm
    - Timing analysis

Legend:
- NanoXplore resources
- Third party tools
- User resources
- FPGA

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NanoXmap Programming Software

NanoXmap-v2 targets to reach Best Performances/Features by End-2018

- **H1-19:** NanoXmap v3, IP Library
- **H2-18:**
  - NG-Large process on-going
  - Embedded Logic Analyser
- **Q2-18:** NG-Medium process stabilized

- **Q3-17 to Q1-18:**
  - NanoXmap optimization process against
    - Logic density
    - Operation frequency (*)
- **2014 to Q3-17:**
  - NanoXmap development: database, algorithms, debug and flow set up from synthesis to bistream
  - Implementation of all FPGA blocks

(*) Acc. LP process

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Next planned NanoXmap features

**IP Library**

- **Planned in coming weeks**
  - *SpaceWire IP core*
  - *DDR Interface (DFI2.1)*

- **In the pipe**
  - *Parallel FIR filters generator,*
  - *FIFO generator (Synchronous & Asynchronous),*
  - *SIN/COS lookup table,*
    - even Direct Digital Synthetizer (DDS) or Numerically Controlled Oscillator (NCO),
  - *Complex Multiplier, Multiplier 24*30bits, Clock generator, etc.*

- **From NX Eco-system**
  - **3D-PLUS:** *DDR Controller,*
  - **Adentis/Maya Technology:** *Mil-Std-1553B BC/RT,*
  - **Skylabks:** *PicoSkyFT-L, and PicoLIB (UART, Timer, I2C, GPIO, ...)*
  - **STAR Dundee:** *SpaceWire, SpW CODEC, RMAP, Routing Switch,*
    - even High Perf. FFTs, Image Processing, Camera Interface, CAN...

And you, what do you need?
**NanoXmap**  Embedded Logic Analyser

- Embedded Logic Analyser IP core (currently in VHDL)
- Expected Q3-18

---

### Menu bar

Configuration parameters bar:
- Capture_width, capture_depth
- Trigger mode (basic or basic_and_edges)
- Capture_mode (pre_trigger_enable & value or multiple_windows)
- Adv_trigger_enable (single_level or two-level_trigger)
- User’s defined additional buffering: 0, 1 or 2

### Status bar:
- Waiting for command
- Waiting for Adv_trigger
- Waiting for trigger
- Current capture window (for multiple_windows capture)
- Loading captured data

---

#### DATA_IN(15:0)
- **251**
- **3BAC**

#### ADDR_W(7:0)
- **1’**
- **0’**

#### CS

#### WR

#### DATA_OUT(15:0)
- **x”3BAC”**
- **x”4E”**

#### ADDR_R(7:0)

#### STATUS(3:0)
- **b”0110”**
- **x”1’**

#### ENA
- **55**

#### CNT(5:0)

---

- **Active Cursor**
  - C1: 604
  - C2: 1095
  - C3: 1917
  - C4: 491
  - C5: 713
  - C6: 222

---

- **Main trigger conditions**
  - Data_in = "0ADC"
  - Addr_W = "x73"
  - CS = "1’"
  - WR = x’(rising)
  - DATA_OUT = 0’xxxxxxxxxxxxxxxxxxxxx
  - ADDR_R = 0’xxxxxxxxxxxx
  - STATUS = 0’xxxx
  - ENA = x’x
  - CNT = 0’xxxxx

- **Adv trigger conditions**
  - DATA_IN = "0ADC"
  - ADDR_W = "x73"
  - CS = "1’"
  - WR = x’(rising)
  - DATA_OUT = 0’xxxxxxxxxxxxxxxxxxxxx
  - ADDR_R = 0’xxxxxxxxxxxx
  - STATUS = 0’xxxx
  - ENA = x’x
  - CNT = 0’xxxxx
1st NX Rad-Hard SRAM-based FPGA
NanoXplore Rad-Hard FPGA Roadmap

*Step1 – NG-Medium*

- **Frequency**: 200 MHz
- **Logic Density**: 35kLUT
- **Complexity**: Low-End FPGA (Just FPGA fabric)
- **Unit Price**: 4th SEFUW – ESA/ESTEC Noordwijk (NL) – 9/11apr18
NG-MEDIUM is ideally a Companion Chip

- FPGA companion chips expand the capabilities of embedded host processors by adding missing host features and by offloading high-speed processing tasks.
- FPGA provides the ideal platform to add custom features tailored to specific project needs and much of the design can be re-used to support multiple processors.
## Overview

### Device Details

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Details</th>
<th>NX1H35S</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic Modules</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register</td>
<td>3840FF<em>28</em>3rows</td>
<td>32,256</td>
</tr>
<tr>
<td>LUT-4</td>
<td>408LUT<em>28</em>3rows</td>
<td>34,272</td>
</tr>
<tr>
<td>Carry</td>
<td>96CY<em>28</em>3rows</td>
<td>8,064</td>
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<tr>
<td><strong>Embedded RAM</strong></td>
<td></td>
<td>2,856Mb</td>
</tr>
<tr>
<td>DPRAM</td>
<td>28RAM<em>2rows</em>48Kb</td>
<td>2.688K</td>
</tr>
<tr>
<td>Core Register File</td>
<td>28<em>2RF</em>3rows</td>
<td>168</td>
</tr>
<tr>
<td>Core Register File Bits</td>
<td>168<em>64</em>(16+6)bits</td>
<td>168K with ECC</td>
</tr>
<tr>
<td><strong>Additional Features</strong></td>
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<tr>
<td>DSP Blocks</td>
<td>56*2rows</td>
<td>112</td>
</tr>
<tr>
<td>SpaceWire link I/F 400Mbps</td>
<td>CODEC</td>
<td>1</td>
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<tr>
<td>High-Speed Serial Link 6,25Gbps</td>
<td>SERDES Tx/Rx</td>
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<tr>
<td>Hard IP Processor core</td>
<td>ARM Cortex R5</td>
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### Clocks

<table>
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<th>Clocks</th>
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<th>NX1H35S</th>
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<tbody>
<tr>
<td>4 CKG * 6 CCK</td>
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<td>24</td>
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</table>

### Inputs / Outputs

<table>
<thead>
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<th>Inputs / Outputs</th>
<th>Details</th>
<th>NX1H35S</th>
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<tbody>
<tr>
<td>I/O banks</td>
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<tr>
<td>DDR PHY (1I0Bs)</td>
<td>2 Complex + 5 Simple</td>
<td>13</td>
</tr>
<tr>
<td>SpaceWire PHY (8I0Bs)</td>
<td>2x / Bank Complex</td>
<td>16</td>
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</table>

### Packages – User I/Os

<table>
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<th>Packages – User I/Os</th>
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<tbody>
<tr>
<td>LG625 &amp; CG625</td>
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<td>374</td>
</tr>
<tr>
<td>CQ352</td>
<td></td>
<td>192</td>
</tr>
<tr>
<td>FG625 (Jun18)</td>
<td></td>
<td>374</td>
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### Vcore

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<th>Vcore: 1,2V</th>
<th>VDD: 1,5 or 1,8 or 2,5 or 3,3V</th>
<th>VAuxAnalog: 2,5V</th>
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</thead>
<tbody>
<tr>
<td>(I/Os, Comp, Thermal Sensors, …)</td>
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</table>

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- Power consumption

- Static Power consumption depends of I/O configuration
- Dynamic Power consumption depends of the design
  - % of FPGA resources usage
  - Operating frequency
    - Finally the power consumption is 0,50 µW/MHz/LUT+DFF

- What about medium?

  - Quiescent VDDcore supply current is
    - 2 versus Antifuse FPGA
    - 2 versus Flash-based FPGA
    - 30+ versus biggest RHBD Sram-based FPGA

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>IDD1V2</td>
<td>Quiescent* Core supply current</td>
<td>TBD</td>
<td>170</td>
<td>295</td>
<td>mA</td>
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<tr>
<td>IDD2V5A</td>
<td>Quiescent* VDD2V5A supply current</td>
<td>-</td>
<td>251</td>
<td>-</td>
<td>mA</td>
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<tr>
<td>IDD_SER</td>
<td>Quiescent* VDD_SERVICE supply current</td>
<td>TBD</td>
<td>20</td>
<td>TBD</td>
<td>mA</td>
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</tbody>
</table>

Quiescent current is measured when the chip is turned on in safe-config mode without any design.

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NG-MEDIUM includes 1x Space Wire CODEC

- Two mode of operation:
  - bitstream download
  - User application

- Full hardware implementation

- Up to 430Mbps

- Standard common mode LVDS buffers
Packet Level transmits address, cargo and end_of_packet

The soft IP implemented in the fabric can handle addressing and different protocols

Time code and control signals are accessed through a serial interface
The NG-MEDIUM includes **16 SW-PHY**

- Clock recovery and data sampling up to 430Mbps
- 10 bits parallel to serial interface
- The soft IP shall implement the exchange and packet level
- Can be used to implement various protocol (RMAP, switch)
NG-MEDIUM includes 16 DDR/DDR2 PHY (physical interfaces)

- The PHY includes the hardware to implement DDR transmission and reception up to 800Mbps
  - SSTL15/18/25 buffers
  - Differential DQS
  - Mixed analog / digital delay lines
  - Dynamic Phase Alignment sensor
  - DDR clock recovery
  - Delay Calibration
  - 4-bits serial / parallel interfaces

- The DDR IP includes
  - a DFI compliance block
  - a state machines for eye centering and initialization
  - a DDR controller
**medium Packaging**

**LGA625**
29*29mm body, 1.00mm pitch

**MQFP352**
48*48mm body, 0.50mm pitch
This NX1H35S bitstream size depends on the application size (configuration) and the number of user Core RAM and Core Register Files to be initialized.

- Maximum configuration (100%): 6.46Mb

The maximum bitstream size is 6460 + 56 \times 96.06 + 168 \times 3.03 = 12210Kb

- So, it would require 3x NVRAM 4Mb or 1x NVRAM 16Mb.

Configuration download would me 240ms maximum with Flash SPI @ 50MHz.

Most applications do not require to initialize all memories. A typical bitstream is less than 8Mb.

- These figures are just estimations. The actual size can be determined only by running the mapping software.
Bitstream Download: Cfg Memory

- Recommended Space FPGA Configuration Memory
  - 3D-PLUS Serial NOR Flash TMR’ed 128Mb / 3DFS128M01VS2728
    - 128Mbit SPI FLASH Nor
    - Single Power Supply operation:
      - Triple 128M-bit/16M-byte
      - Triple Modular Redundancy (TMR) integrated
      - Enhanced TID implementation
      - Supports standard SPI
      - 50MHz Normal
      - More than 100,000 erase/program cycles
      - More than 20-year data retention
      - Program 1 to 256 bytes per page
      - Program/Erase Suspend & Resume
      - Low Instruction Overhead Operations
      - Continuous Read 8/16/32/64-Byte burst
      - Selectable burst length
      - Available Temperature Range:
        - 0°C to 70°C
        - -40°C to +85°C
        - -55°C to +125°C
  - Programmable Clock 50MHz ÷ n
The DevKit is an evaluation board to be used interactively through
- **JTAG**, or
- standalone from a **EEPROM board**.

The board configuration mode is thus selected by on-board jumpers.

A 10-pin HE10 connector is provided to receive an EEPROM memory board (Atmel Dump Mode **EEPROM** or standard **SPI EEPROM**).

An optional SpaceWire connector allows **SpaceWire** configuration.
RADIATIONS

SEE campaigns

- 4 SEE campaigns done in Q4CY16 and Q4CY17
  - **OCT & NOV16:**
    - 2 UCL/HIF campaigns,
    - 1st silicon, packaged in LGA625,
    - Static & Dynamic SEU/SET/SEFI testing.
  - **NOV17:**
    - PSI/PIF campaign
    - Latest silicon, packaged in LGA625.
  - **DEC17**
    - UCL/HIF campaign,
    - Latest silicon, packaged in LGA625,
    - Full SEE testing (SEL/SEU/SET/SEFI)
Radiations

SEL testing

- Temperature 100° C, regulated by PID controller,
- Supply at their max value (+10%),
  - VDD1V2: 1.32V
  - VDD3V3: 3.63V
  - VDD2V5: 2.75V
  - VDD1V8: 1.98V
- Fluence over $10^7$ p/cm$^{-2}$ with the highest LET $^{124}$Xe$^{35+}$
- NO LATCH-UP event was detected during the test period.
Heavy-Ions
Cfg Memory Xsection

SEU Cross-section (cm²/bit) vs. LET Eff (MeV/(mg/cm²))

- NG_medium Measure DUT6+7
- NG_medium Measure DUT6+7 tilted phi=0
- NG_medium Measure DUT6+7 tilted phi=90
- NG_medium Measure Weibull

Weibull parameter DUT6+7:
- SIGsat (cm²/bit): 5.1852 E-09
- Onset / L0 (MeV/(mg/cm²)): 0.11214
- Width (MeV): 36.4286
- s: 4.44737
Protons

Cfg Memory Xsection

- Xsection confidence intervals of 95% (alpha = 5%) are calculated for:
  - Relative fluence uncertainty of PSI is $\delta F/F = 5\%$.

![Graph showing cross section vs. energy with Weibull parameters]

<table>
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<tr>
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<th>Value</th>
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<tr>
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<td>4.84232E-16</td>
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<tr>
<td>Onset / L0</td>
<td>29.99900</td>
</tr>
<tr>
<td>MeV/(mg/cm$^2$)</td>
<td></td>
</tr>
<tr>
<td>Width (MeV)</td>
<td>28.16281</td>
</tr>
<tr>
<td>$s$</td>
<td>0.47816</td>
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</table>
Orbital Upset Rate

HEAVY IONS Weibull

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<th>SIGsat (cm²/bit)</th>
<th>5.1852 E-09</th>
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<tr>
<td>Onset / L0 (MeV/(mg/cm²))</td>
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PROTONS Weibull

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<td>28.16281</td>
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<tr>
<td>s</td>
<td>0.47816</td>
</tr>
</tbody>
</table>

- Orbital Upset Rate calculation (CREME 96 model, OMERE software):
  - Solar min, AE8 electron model, AP8 proton model,
  - shielding = 100mils
  - sensitive volume thickness = 2µm

Mission profile

<table>
<thead>
<tr>
<th>SER (bit/day)</th>
<th>2,05E-10</th>
<th>1,26E-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SER (chip/day)</td>
<td>1,30E-09</td>
<td>7,98E-3</td>
</tr>
<tr>
<td>LEO1 Pol (800km, 800km, 98°)</td>
<td>2,57E-09</td>
<td>1,58E-2</td>
</tr>
<tr>
<td>LEO2 ISS (400km, 400km, 51,5°)</td>
<td>3,06E-10</td>
<td>1,88E-3</td>
</tr>
</tbody>
</table>

- Outside of CMIC
  - Which will correct 98% of Single Errors.

- Only a small fraction of NX FPGA memory cells are used

*Less than 10% of configuration bits used in typical design*
Next SEE Campaigns

- Neutrons SEE testing of PicoSkyFT design at ISIS / ChipIR by Skylabs and University of Maribor (Si),
- Heavy ions campaigns to be performed by UFRGS (Br),
- 4th UCL/HIF campaign to be performed ourselves,
- New Radiation campaign, expected from CERN at PSI & CHARM,
- New Radiation campaign, expected from CTI (Br)
  - TID ($^{60}$CO & X-Ray)
  - Heavy Ions
  - Protons
  - Neutrons
• Space Qualification is running at STM on both CQFP-352 & LGA-625,
• ESCC9000 qualification completion expected SEP18,
• and QML-V qualification completion DEC18,
• QML-V certification from DLA expected FEB19
NanoXplore Rad-Hard FPGA Roadmap

Step 2 – NG-Large

- **200 MHz**
- **35kLUT**
- **140kLUT**

- **Low-End FPGA (Just FPGA fabric)**
- **Mid-End FPGA with SERDES & Single-core ARM-R5**

**Complexity**

**Unit Price**

**Logic Density**
NG-Large replaces both MPU + Companion Chip

- 4x density vs NG-Medium
- Thanks to World-Wide recognized ARM Cortex-R5, optimized for High-Performance, Hard Real-Time applications.
### Device Details

<table>
<thead>
<tr>
<th>Device</th>
<th>Details</th>
<th>NX1H140</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Capacity</strong></td>
<td>Equivalent System Gates</td>
<td>15 000 000</td>
</tr>
<tr>
<td></td>
<td>ASIC Gates</td>
<td>1 900 000</td>
</tr>
<tr>
<td><strong>Logic Modules</strong></td>
<td>Register</td>
<td>7x Tile + 4CGBs</td>
</tr>
<tr>
<td></td>
<td>LUT-4</td>
<td>384DFF<em>48</em>7rows</td>
</tr>
<tr>
<td></td>
<td>Carry</td>
<td>408LUT<em>48</em>7rows</td>
</tr>
<tr>
<td></td>
<td></td>
<td>96CY<em>48</em>7rows</td>
</tr>
<tr>
<td><strong>Embedded RAM</strong></td>
<td>DPRAM</td>
<td>9,888Mb</td>
</tr>
<tr>
<td></td>
<td>Core Register File</td>
<td>48RAM<em>4</em>48Kb</td>
</tr>
<tr>
<td></td>
<td>Core Register File Bits</td>
<td>48RF<em>2</em>7rows</td>
</tr>
<tr>
<td></td>
<td></td>
<td>672<em>64</em>(16+6)bits</td>
</tr>
<tr>
<td><strong>Additional Features</strong></td>
<td>DSP Blocks</td>
<td>672 with ECC</td>
</tr>
<tr>
<td></td>
<td>SpaceWire link I/F 430Mbps</td>
<td>96DSP*4rows</td>
</tr>
<tr>
<td></td>
<td>SERDES Tx/Rx 6,25Gbps</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Hard IP Processor core</td>
<td>4 Hex x 6 SERDES</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ARM Cortex-R5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td><strong>Clocks</strong></td>
<td>4 CLK * 8 CKC</td>
<td>32</td>
</tr>
<tr>
<td><strong>Inputs / Outputs</strong></td>
<td>I/O banks</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>DDR PHY (11 IOBs)</td>
<td>10 Complex</td>
</tr>
<tr>
<td></td>
<td>SpaceWire PHY (8 IOBs)</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2x / Bank Complex</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
</tr>
<tr>
<td><strong>Packages - User I/Os</strong></td>
<td>LG1752 &amp; CG1752</td>
<td>42,5*42.5mm / 1mm</td>
</tr>
<tr>
<td></td>
<td>FF1752</td>
<td>42,5*42.5mm / 1mm</td>
</tr>
<tr>
<td></td>
<td>FF1152 (TBC)</td>
<td>35*35mm / 1mm</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td>$V_{core}$: 1.2V</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td>$V_{IO}$: 1.5 or 1.8 or 2.5 or 3.3V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{Aux Analog}$: 2.5V</td>
<td></td>
</tr>
</tbody>
</table>

*Note: ECC stands for Error Correcting Code.*
- **SERDES developed in C65 Space, acc. Veloce contract,**
- **Take into account Space requirements, (esp JESD204B, SpF, ...),**
- **0.70 – 6.25 Gbps data rate,**
- **NG-Large will embed 4 Hex SERDES= 24 HSSLs.**

**Hex architecture:**
- HSSL blocks provide multi-protocol high-speed serial link capability with multi-rate support.
- Hex HSSLs are composed of 6 RX/TX lanes, a PLL, and a calibration circuit.
- Each transceiver lane includes the PMA and PCS hard macros.
- The SERDES block has configurable features such as data width (up to 80 bits in parallel), equalization and protocol dependent properties.

**HSSL supported protocols:**

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Type</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESIstream</td>
<td>3,125 – 6.25Gbps</td>
<td>14B/16B</td>
</tr>
<tr>
<td>Serial RapidIO</td>
<td>3,125 – 6.25Gbps</td>
<td>8B/10B</td>
</tr>
<tr>
<td>JESD204B</td>
<td>3,125 – 6.25Gbps</td>
<td>8B/10B</td>
</tr>
<tr>
<td>SpaceFibre</td>
<td>3,125 – 6.25Gbps</td>
<td>8B/10B</td>
</tr>
</tbody>
</table>
This NX1H140TSP bitstream size depends on the application size (configuration) and the number of user Core RAM and Core Register Files to be initialized.
- Maximum configuration (100%): 26.46Mb

The maximum bitstream size is 26458 + (192 x 96.06) + (672 x 3.03) = 46938Kb
- So, it would require 3x NVRAM 16Mb or 1x NVRAM 64Mb.

Configuration download would me 118ms maximum with Flash QSPI @ 100MHz.

Most applications do not require to initialize all memories. A typical bitstream is less than 32Mb.
- These figures are just estimations. The actual size can be determined only by running the mapping software.
NG-Large forecast of Config SEU cross-section (LET)

Configuration Memory SEU
@ 25°C, VDDmin

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIGsat (cm²/bit)</td>
<td>2.32E-09</td>
</tr>
<tr>
<td>L0 (MeV/(mg/cm²))</td>
<td>0.42243</td>
</tr>
<tr>
<td>W (MeV)</td>
<td>49.42755</td>
</tr>
<tr>
<td>s</td>
<td>4.91666</td>
</tr>
</tbody>
</table>

SER:
- SEU/config/day: 8.26E-13 SEU/config/day
- SEU/chip/day: 2.03E-05 SEU/chip/day
- SEU/chip/year: 7.4E-03 SEU/chip/year → SER > 100 years
NanoXplore Rad-Hard FPGA Roadmap

**Step3 – NG-Ultra**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Complexity</th>
<th>Unit Price</th>
<th>Logic Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 MHz</td>
<td></td>
<td></td>
<td>35kLUT</td>
</tr>
<tr>
<td>500 MHz</td>
<td>Low-End FPGA (Just FPGA fabric)</td>
<td></td>
<td>140kLUT</td>
</tr>
<tr>
<td></td>
<td>Mid-End FPGA with SERDES &amp; Single-core ARM-R5</td>
<td></td>
<td>550kLUT</td>
</tr>
</tbody>
</table>

**High-End SoC FPGA**
Based on Quad-cores ARM-R52
NG-Ultra becomes a System-On-Chip
- **4x FPGA density vs NG-Large**
- Full SoC architecture based on Quad-core ARM Cortex-R52, again optimized for High-Performance, Hard Real-Time applications.

SoC definition: It includes an Embedded Processor + Logics & RAM blocks, even analog circuitry.

Benefits: Reducing form factor, power consumption, heat dissipation, analog mixed signal integration
1st Rad Hardened SoC
High-End FPGA

- Performance:
  - Logic: 500MHz
  - DSP: 800MHz
  - Diff I/O: 1Gbps
  - SerDes: 12.5Gbs
  - ARM R52: 600MHz

- ECSS Class-1 qualification

- Hardening performance
  - Fully hardened by design
  - Fully SEU immune up to 60 MeV-cm² / mg
  - Total dose > 50 Krad TID
  - No single event latch up (LET > 60 MeV-cm² / mg)
NX FPGA Schedule

One Qualified Radiation Hardened FPGA device every year from 2018

2018

Q2CY18

NX1H35 TapeOut

Q4CY18

NX1H35 Proto

Q4CY18

NX1H35 QML-V

2019

Q2CY19

NX2H600 TapeOut

Q4CY19

NX2H600 Proto

Q4CY20

NX1H600 QML-V

2020

Q2CY19

NX1H140 TapeOut

Q4CY19

NX1H140 Proto

Q4CY19

NX1H140 QML-V

2016

Q3CY16

NX1H35 TapeOut

Q2CY17

NX1H35 Proto

Q4CY18

NX1H35 QML-V

2017

Q2CY18

NX1H140 TapeOut

Q4CY18

NX1H140 Proto

Q4CY19

NX1H140 QML-V

2018

Q4CY19

NX2H600 Proto

Q4CY20

NX1H600 QML-V

2019

Q4CY19

NX1H140 QML-V

2020

Q4CY20

NX1H600 QML-V

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Conclusion
Thank you

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