

# FUSIO RT

## A New Space Modular Computer Core based on NG-Medium FPGA

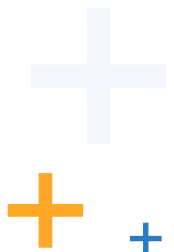
SEFUW 2018



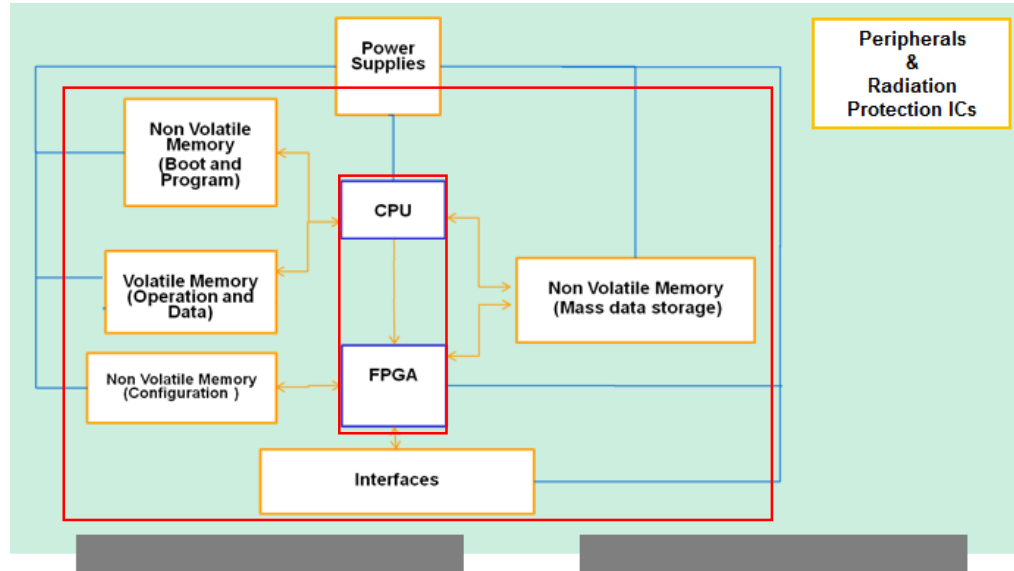
| Pierre-Xiao WANG  
| April 9th, 2018  
| ESTEC



- What is FUSIO RT / Modular Computer Core
- The motivation
- The architecture
- The key feature & benefits
- Conclusion

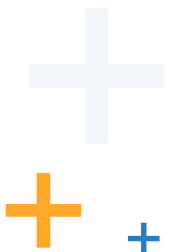


# What is this modular computer core



FPGA based computer unite is quite common in space design thanks to FPGA's high flexibility, high performance and its short time to market and unit low cost.

A **Modular Computer Core**(MCC) is this kind of **complete computer built in a single module** with modular design, with microprocessor(inside of FPGA), memories, input/output (I/O) and other features required of a functional computer.

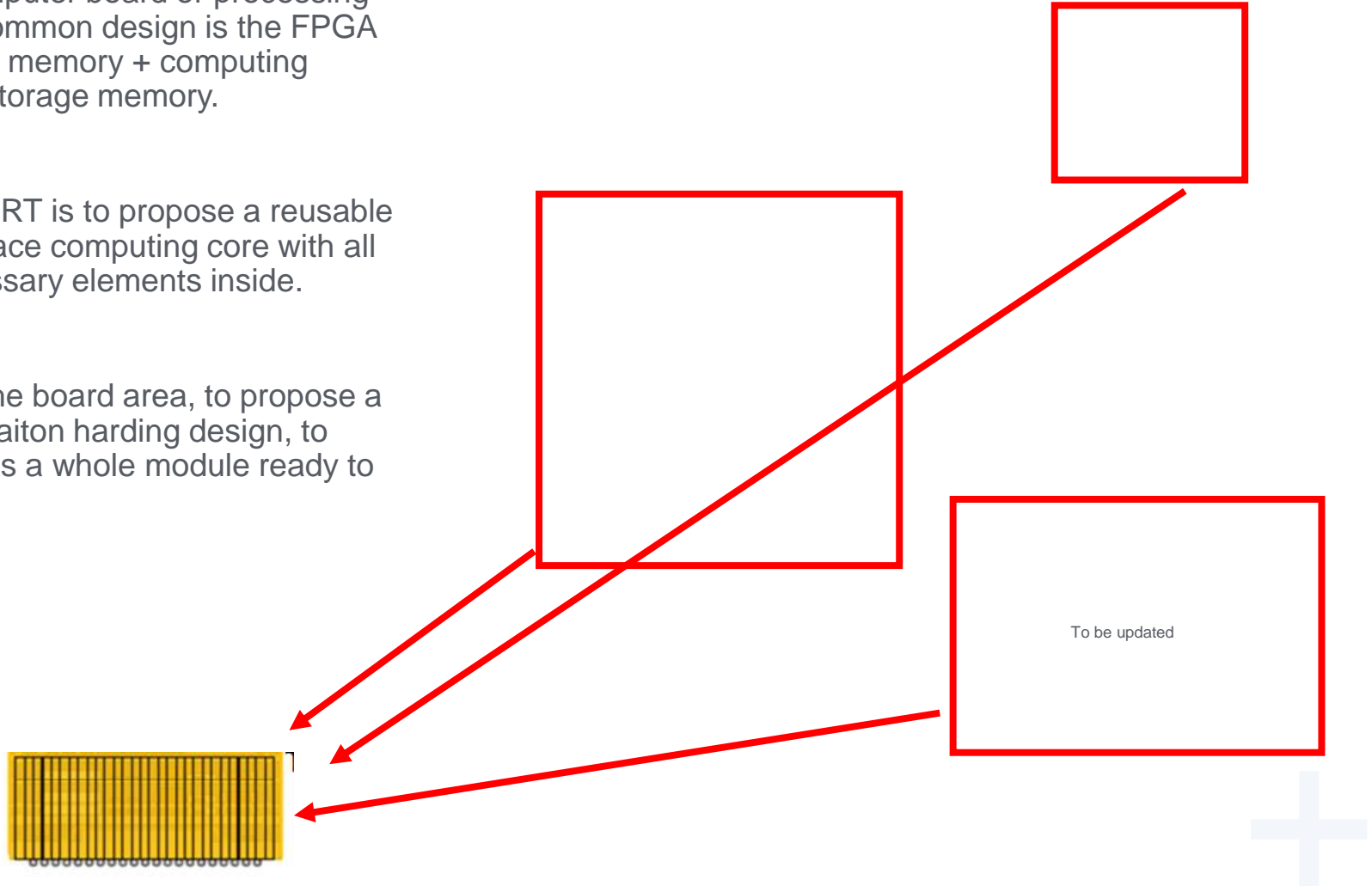


# The motivation to develop this module

In most computer board or processing unite, the common design is the FPGA with its boot memory + computing memory + storage memory.

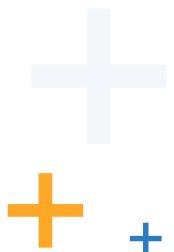
The FUSIO RT is to propose a reusable matured space computing core with all these necessary elements inside.

To reduce the board area, to propose a verified radiaiton harding design, to qualified it as a whole module ready to use.



# Under CNES R&T

3D PLUS develop this module under CNES R&T activity

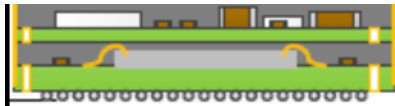


# Modular computer core architecture

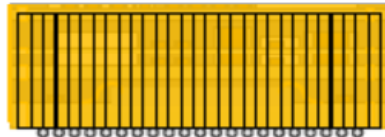
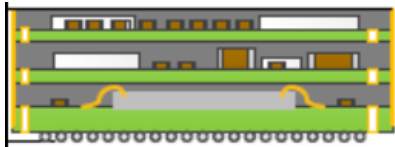
Modular design with same footprint



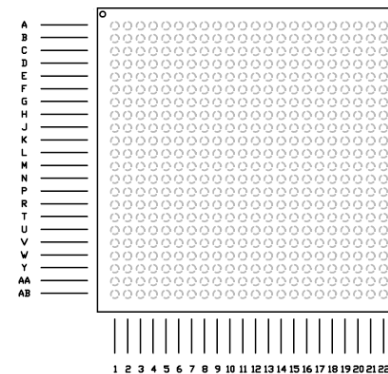
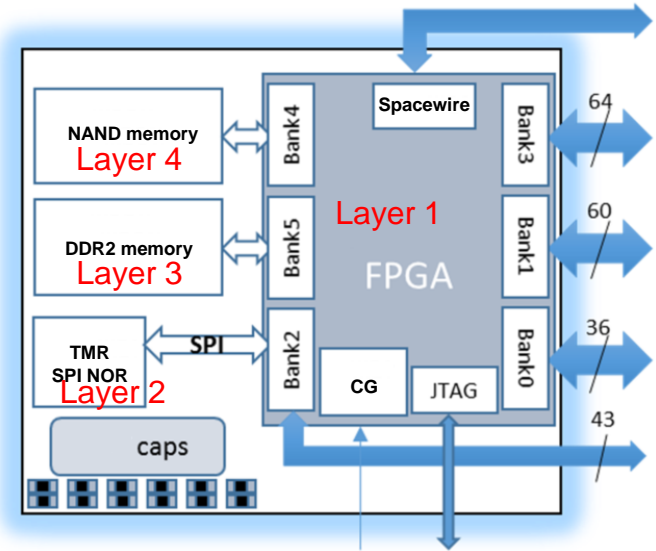
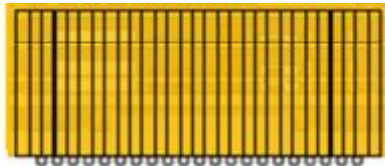
L1+L2



L1+L2+L3

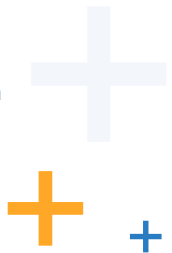


L1+L2+L3+L4



The module will keep all configurations at the **same footprint** with NG-Medium

BGA484 1.27pitch, LxWxH: 32x32x12mm

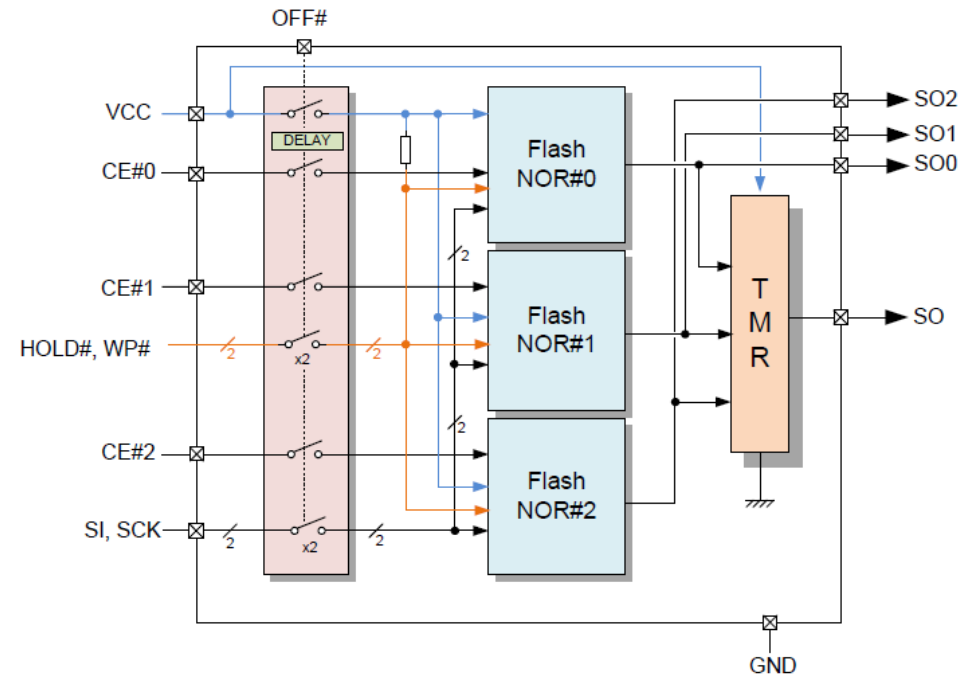
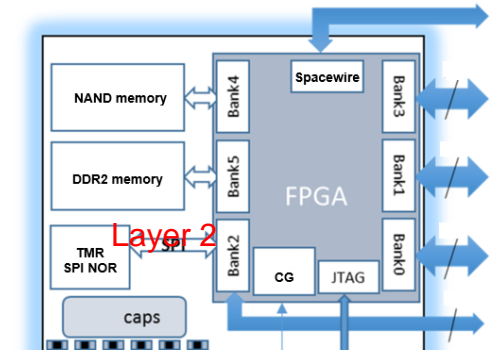


# Memories Features

**Configuration** + Computing + Mass memories are inside of the module

## Configuration Memory:

- **Standard SPI NOR – triple dice, each 128Mb**
- **TMR** - Triple vote to mitigate SEU
- 100K erase/program cycles
- 20 Years data retention
- Single Power Supply operation: 3.3V read, erase and program operations.
- Enhanced TID implementation (Switch integrated)
- 50MHz Normal
- Program 1 to 256 bytes per page
- Program/Erase Suspend & Resume
- Low Instruction Overhead Operations



\*Please note: this TMR SPI Nor can be ordered as a single module under 3D PLUS P/N: 3DFS128M01VS2728





# Memories Features

Configuration + **Computing + Mass memories** are inside of the module

## Computing Memory (Optional):

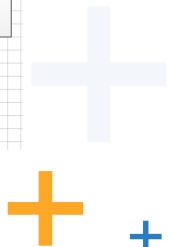
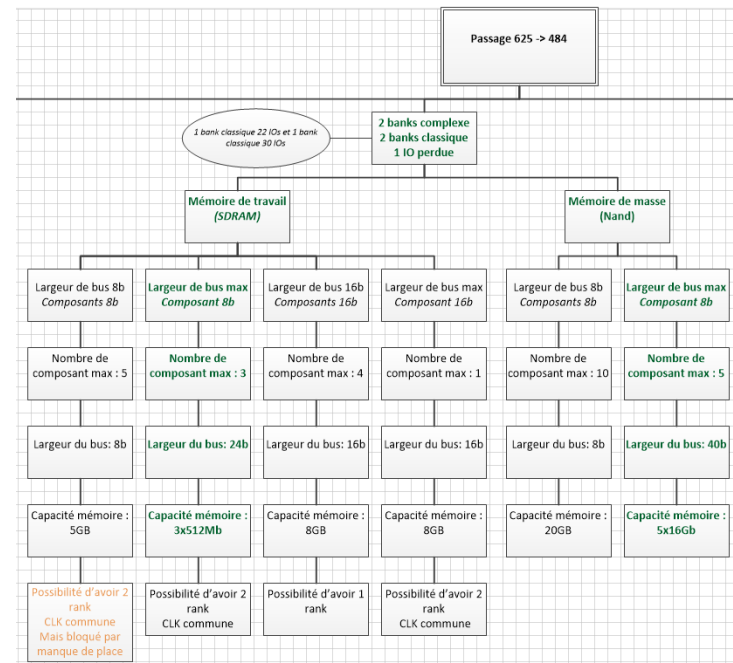
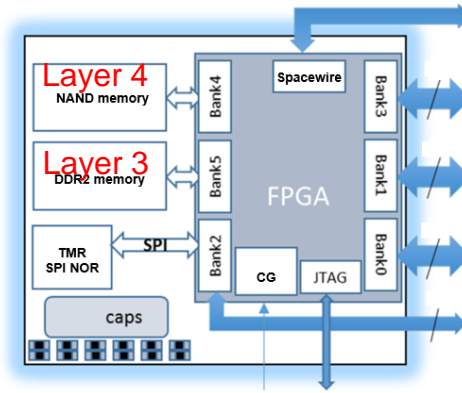
- **SDRAM – from x8 to x24b bus** to adapt to different speed & ECC
- From 512Mb to 1.5Gb configurations
- 3D PLUS SDRAM memory listed at EPPL

## Mass Memory (Optional):

- **Nand Flash – from 16Gb to 64Gb configurations**
- From x8b to x32b bus to adapt to different speed
- 100K erase/program cycle
- 10 years data retention
- 3D PLUS NAND memory listed in EPPL

## Radiation Hardening IP Core (Optional):

- SDRAM Controller IP core to manage the SDRAM radiation issue
- Nand Flash Controller IP core to manage the Nand Flash radiation issue





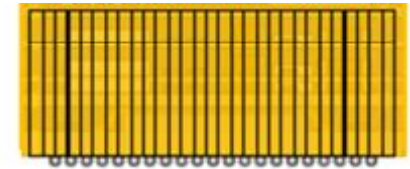
# FUSIO RT module

a trade off among performance/power/size/easy to use



- **BGA484 1.27mm pitch**, LxWxH: 32x32x12.5mm (all memories)

- 1.27mm BGA is under 3D PLUS PID.
- BGA 484 with 32X32mm saving PCB area
- Easy to assembly
- All memory I/Os has been integrated inside of the module
- 262 user I/Os (3.3V, 1.8V & 1.5V ) available

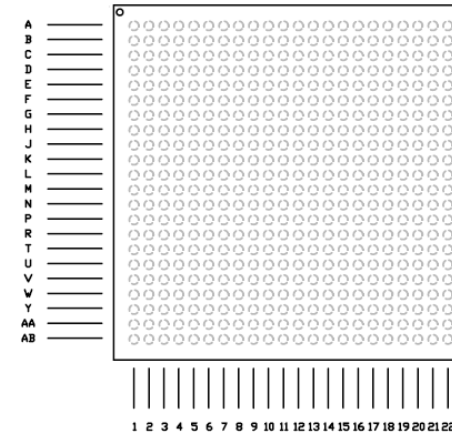


- **SDRAM/Nand had been selected**

- sufficient performance
- No further termination regulator needed for SDRAM
- Good power consumption/ 3.3V I/Os

- **Radiation tolerance**

- Total ionizing dose > 50Krad
- SEL immune up to LET > 60MeV.cm2/mg.
- SPI Nor switch off during non-use
- memory controller IP core ready to use to manage radiation issue



no board design for the memories

no memory controller design

Radiation Hardening design

all in one Space Qualified Package



# FUSIO RT module summary

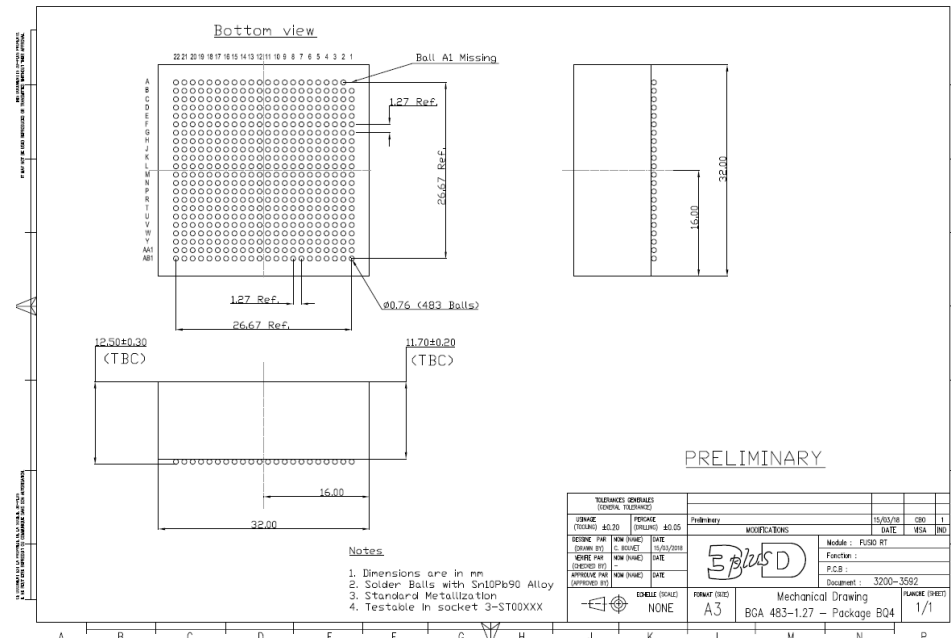
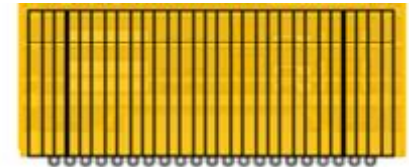


## Key Features & Benefits

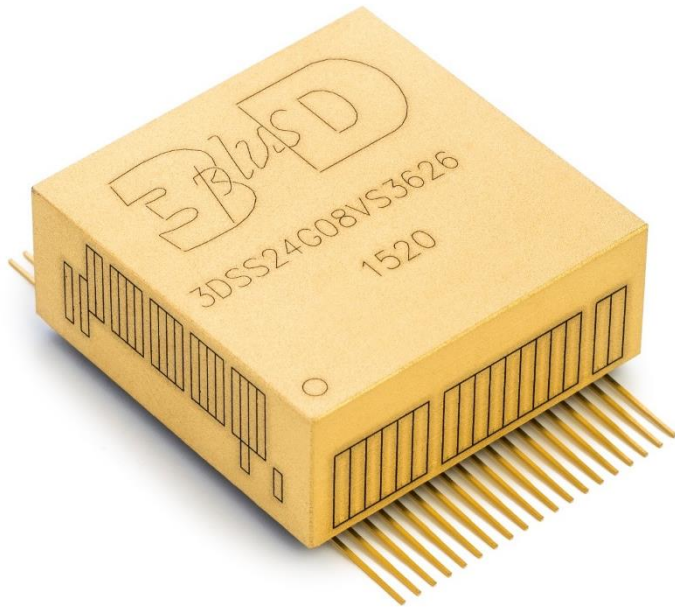
### FUSIO RT : FPGA integrated with Radiation tolerant Memory

#### Module Key Benefits:

- **Space technology FPGA**
- **Triple vote SPI NOR** – bitstream memory integrated
- **Optional DRAM** – max x24b wide computing memory integrated
  - ❖ DRAM Controller IP core available
- **Optional Nand** – max x32b wide mass memory integrated
  - ❖ Nand Flash Controller IP core available
- Embedded bitstream integrity check – low error rate
- **262 user I/Os** (3.3V, 1.8V & 1.5V ) available
- Temperature range: -55 to +105°C
- **BGA484 1.27mm pitch**, LxWxH: 32x32x12.5mm (all memories)
- Radiation Tolerance:
  - Total ionizing dose > 50Krads
  - SEL immune up to LET > 60MeV.cm2/mg.
- The EM will be available the end of 2018, and FM will be available at middle of 2019



# Thanks For Your Attention



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