Experience Summary on Microsemi RTG4 designs

SEFUW: SpacE FPGA Users Workshop, 4th Edition

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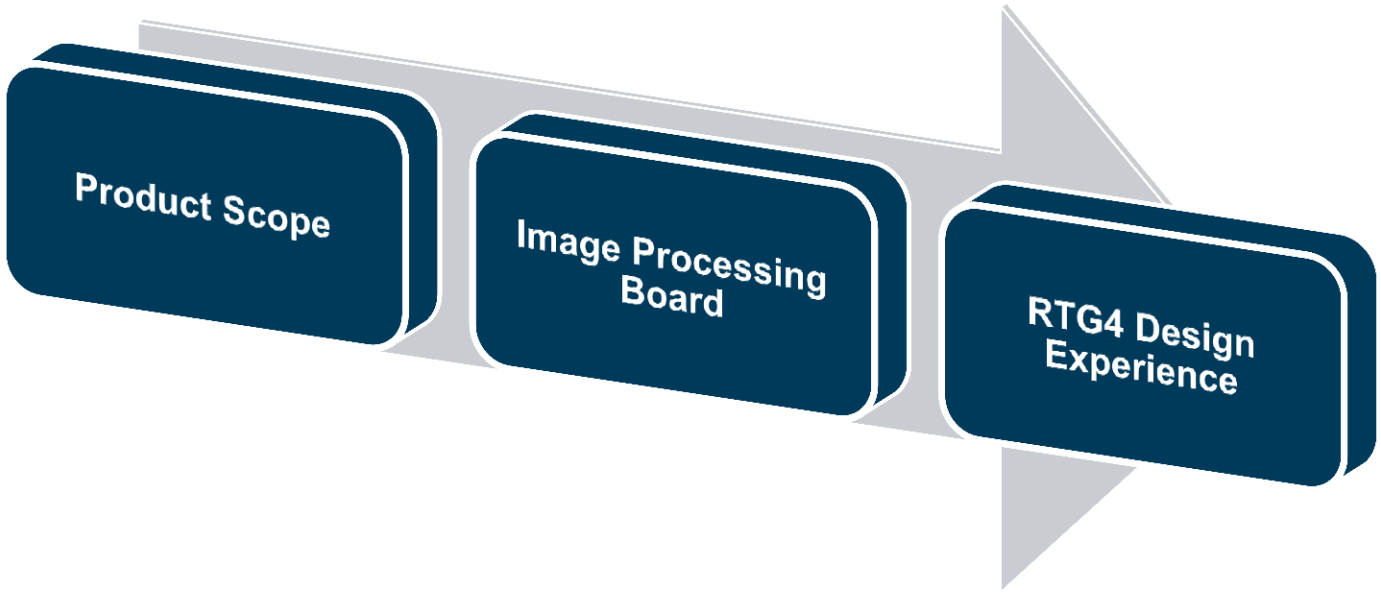
OVERVIEW

Overview


Product Scope
Image Processing Board
RTG4 Design Experience

PRODUCT SCOPE

Jena-Optronik GmbH

Jena-Optronik LIDAR Sensors

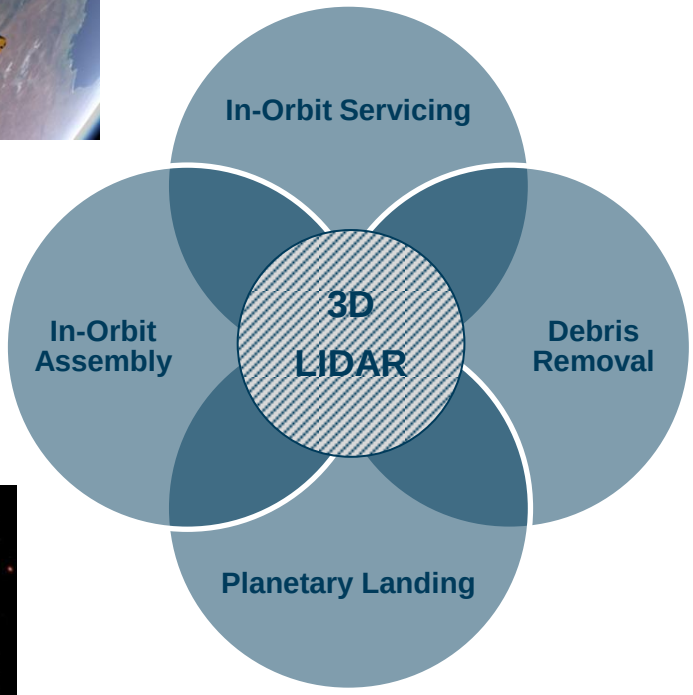


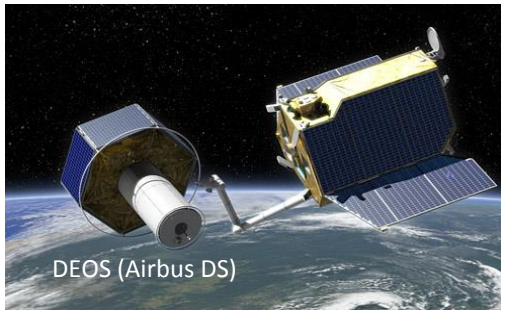

RVS-ARP

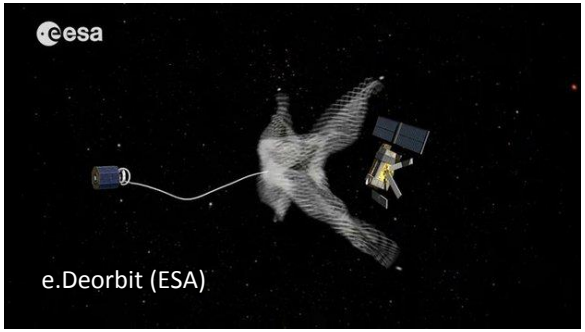
RVS for ATV / HTV / Cygnus

42 Flight Models delivered, 48 under contract, flawless flight heritage


Market Opportunities



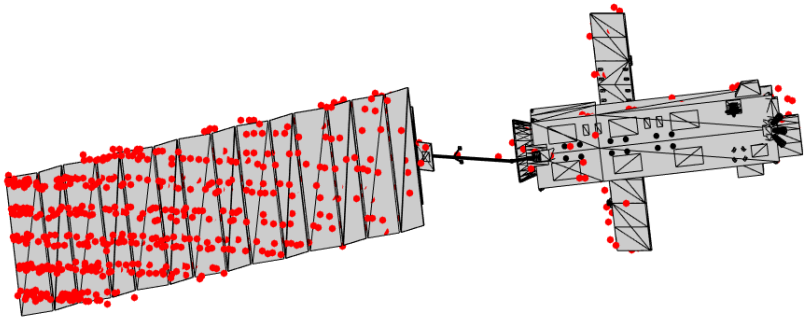




RVS3000-3D Pose Estimation

- LIDAR + Image processing = “One Box Solution”
- Real-time calculation of 6DOF information
- Application of Iterative Closest Point Algorithm
- Matching between LIDAR scans and target CAD model

Debris Removal Scenario

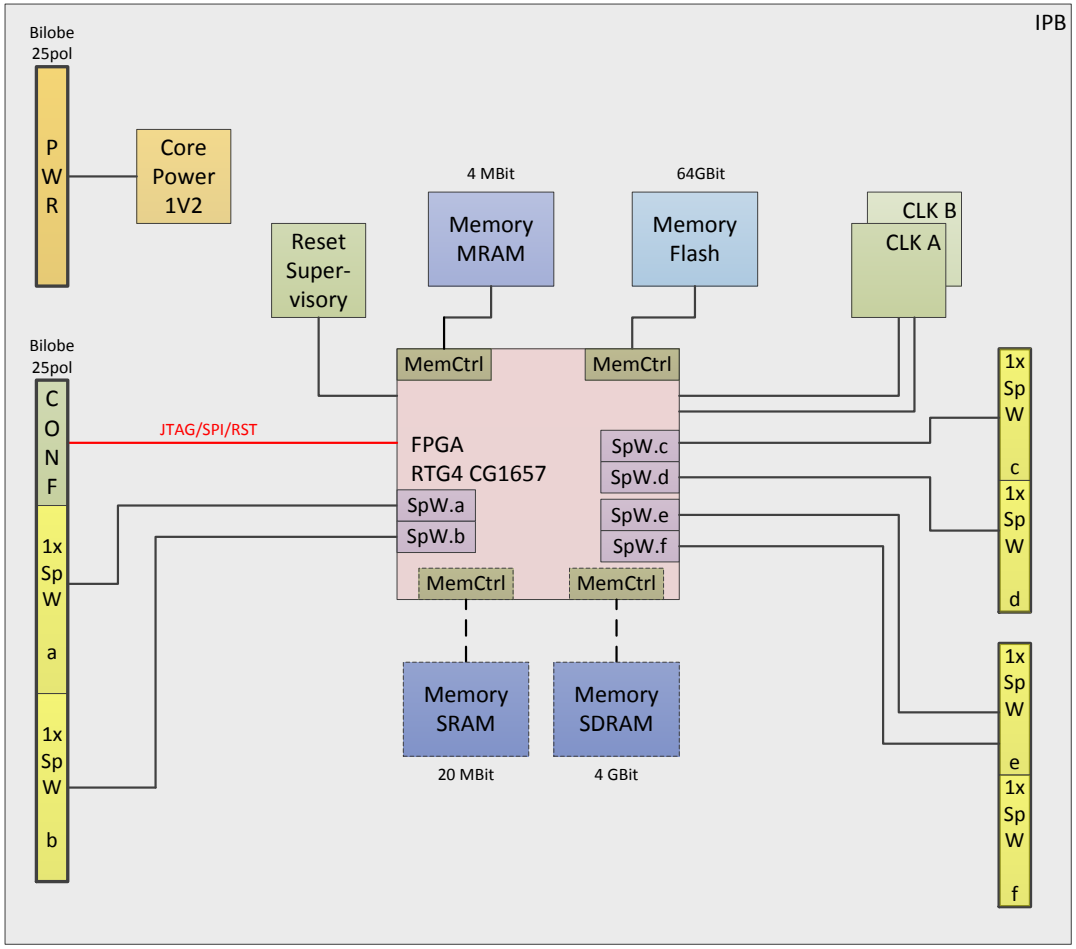


Match Scan Data with CAD Model

IMAGE PROCESSING BOARD

High Performace In-Orbit Computing Plattform

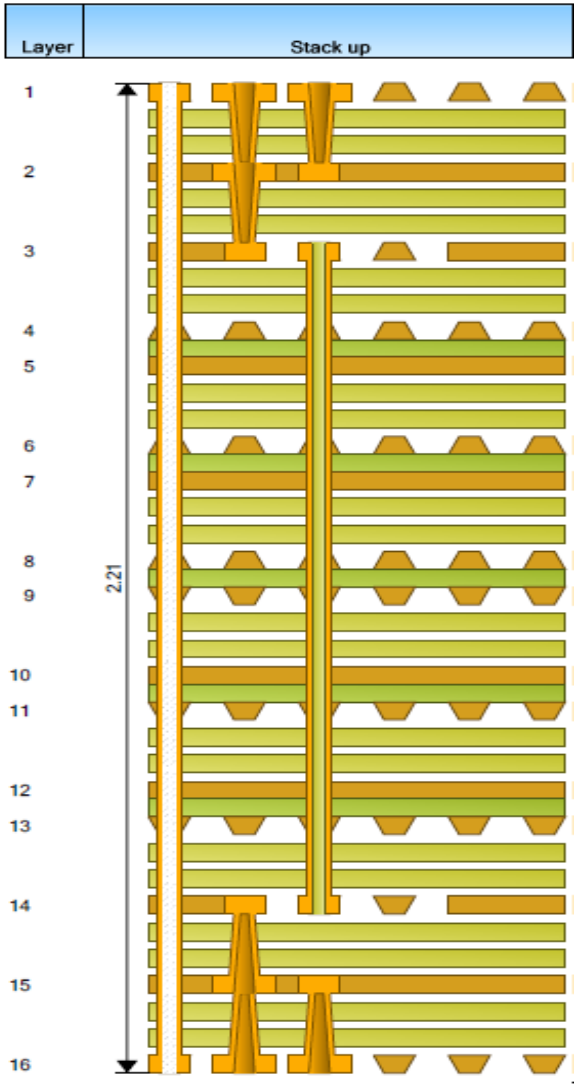
Block Diagram



Main Challenges

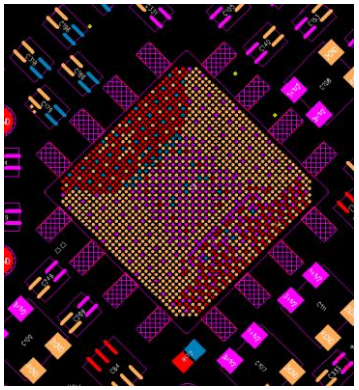
- Stable Core Supply for rapid changing loads
- IP Core support for memories
- Limitation of IO types
- Decoupling condensators (more than 300 for fully populated RTG4)
- Mounting of CCGA 1657 RTG4 package

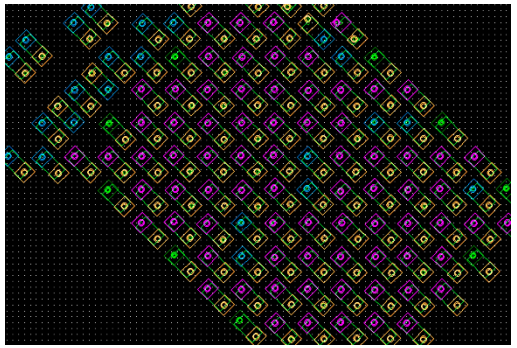
PCB Stackup

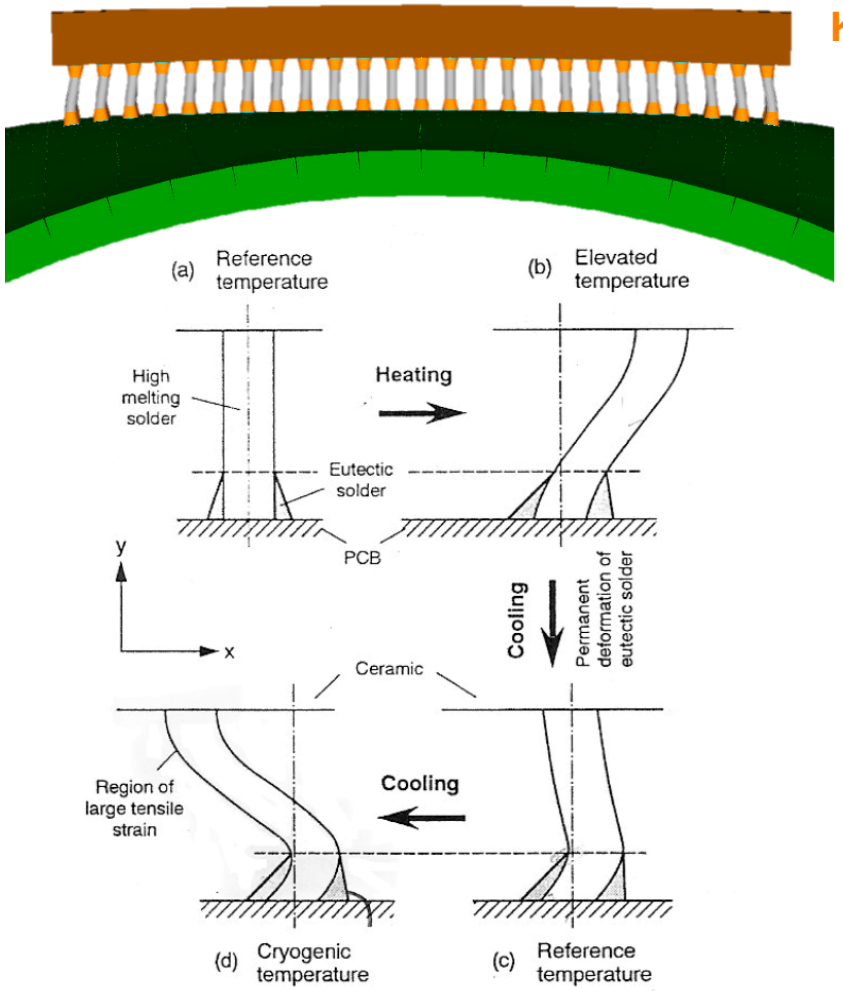


Key Aspects

- 16 layer Stackup
- 8 signal layers capable of routing out up to 80 % of the RTG4 IO pins
- blind and buried via technology
- 2 supply voltage layers
- Via-In-Pad Technology
- No SERDES support!







Key Aspects

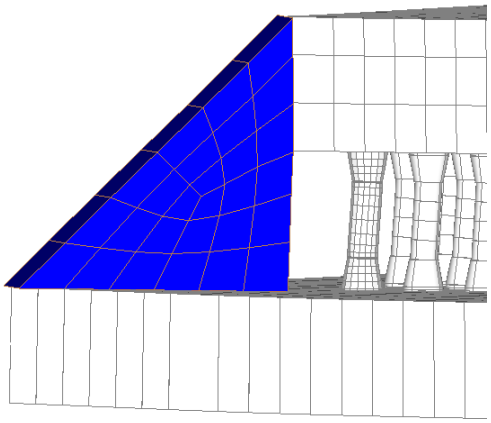
- Mechanical stress due to vibration and temperature changes

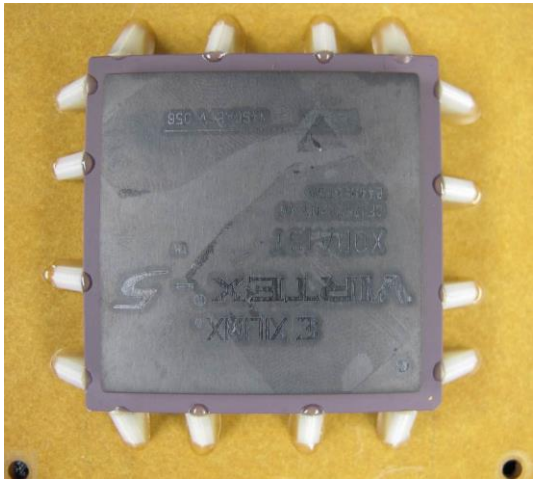
CTE for	Unit	FR4	Hitachi 705G
X-Axis	µm	14	5-7
Y-Axis	µm	12	5-7
Z-Axis	µm	70	10-15

Key Aspects

- Mechanical stress due to vibration and temperature changes
- Low CTE Material to minimize the thermal stress between PCB and CCGA package

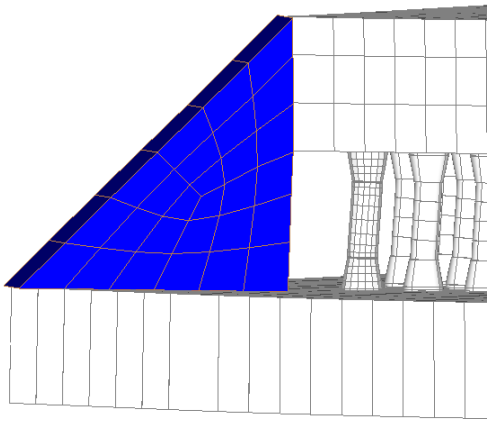
PCB Mounting

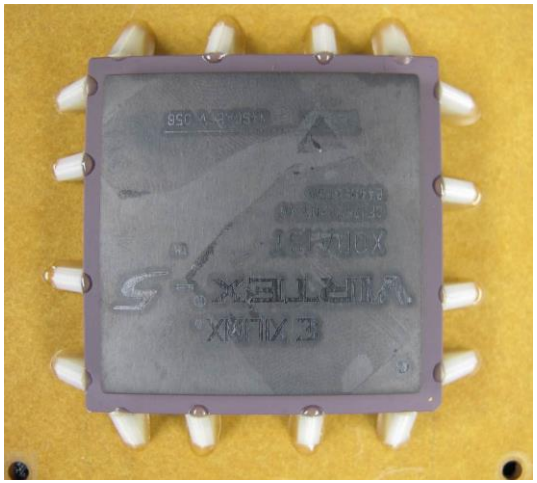




Key Aspects

- Mechanical stress due to vibration and temperature changes
- Low CTE Material to minimize the thermal stress between PCB and CCGA package
- Corner Pins to stabilize outer columns





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Qualification has been passed for CCGA1752 packages in 2015

Delta qualification for CCGA1657 with 1 mm pitch is expected to be finished in Q2/2018

RTG4 DESIGN EXPERIENCE

Main Challenges

- Accuracy of Power Estimator
  - First estimation of ~ 5 W for our design
  - 1.5 W for the whole board during Lab Tests!
  - Rerun of power estimation with the latest spread sheet -> 12 mW less
  - Iterating the spread sheet values parameters by using the final synthesis values for register count, clock tree etc.
    - ➔ Still 3.6 W
    - ➔ overdesigned power supply

Main Challenges

- Accuracy of Power Estimator
- asynchronous reset net limitations

  Why asynchronous resets?

  - Heritage designs use asynchronous resets
  - Defined state of flip flops and IOs during power up
  - Change FF state if clock is not present anymore -> SpW RX part

  Conclusion: one asynchronous reset net is not enough!

  Microsemi approach of net segmentation result often in unroutable designs

Main Challenges

- Accuracy of Power Estimator
- asynchronous reset net limitations
- Libero Design Suite
  - use of Libero is mandatory for RTG4
  - TCL interface is available but not all functions are supported yet (IP cores)
  - Integrated make mechanism is annoying
  - Better error massages are appreciated

Main Challenges

- Accuracy of Power Estimator
- asynchronous reset net limitations
- Libero Design Suite
- Microsemi Support
  - Slow flow of information (TNs, CNs, document updates)
  - FAE support is overloaded -> only 1 FAE is not enough
  - Customer support via online platform
    - Long response time of a week or more
    - different customer service members every time
    - Quality of replies differs a lot
    - 1 issue was closed without any comment

TANK YOU FOR
YOUR ATTENTION

QUESTIONS?