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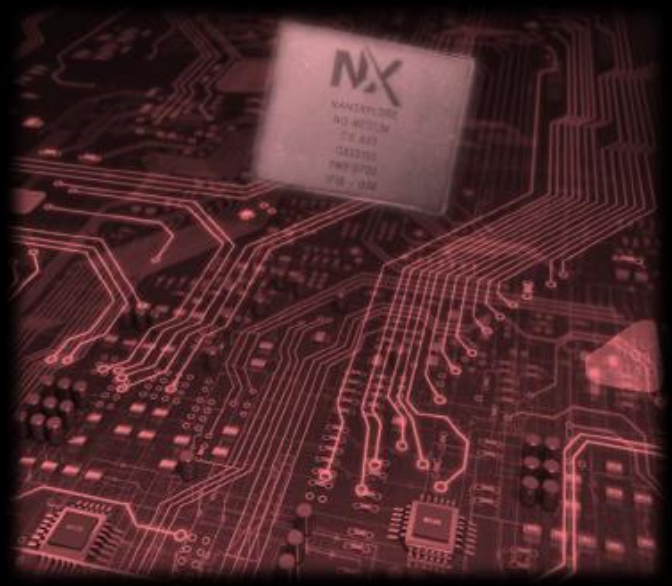
QUEENS-FPGA:
Quality Evaluation of European New SW for BRAVE FPGA

SEFUW 2018
ESTEC 11th April 2018



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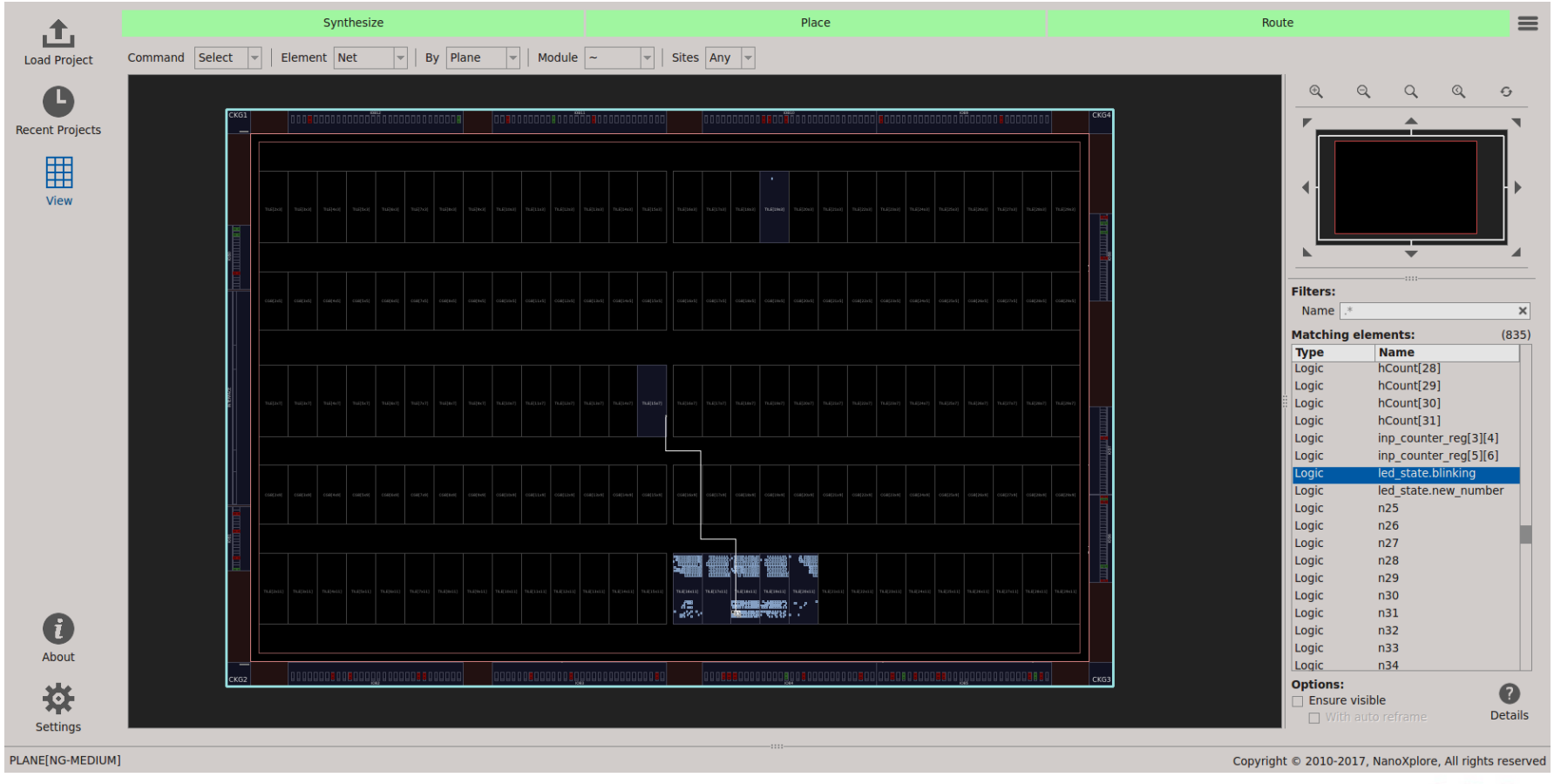
gmv BLOG

NanoXmap SW Tools

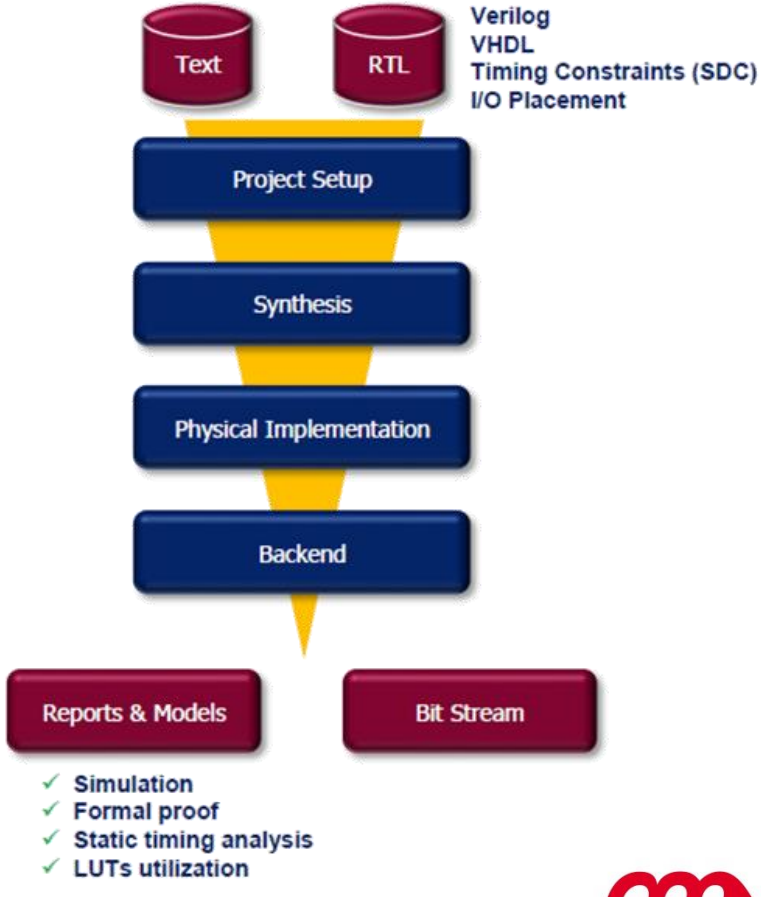


Código Doc.

QUEENS-FPGA OBJECTIVES

QUality assessment Evaluation of European NanoXplore SW for brave FPGA

- ❑ BRAVE project provided very promising European SRAM-based FPGAs for Space
- ❑ FPGA Development SW is really important to take full advantage of the technology
- Quality systematic Assessment Plan based on measurable FPGA SW Tools Metrics identification
- HW benchmarking identification based on consortium background knowledge (GMV, NTUA, NanoXplore)
- Performance and Reliability Evaluation
- FPGA and HDL-languages expertise on Space projects under ESA contracts
- Migration or Porting to BRAVE of in-house developed IP-core for space project



EVALUATION RESULTS BASES

DOES IT MAKE THE JOB?

Can you use it for your mission?

SW tools comparison

Usability, Flexibility, Reporting, Inference, Libraries

HW devices comparison

Power, Performances, Area

QUEENS-FPGA METRICS

ABILITY TO:
- synthesize a RTL code
- ability to route a design
- Inferred VHDL coding and mapping

SW TOOL PC CONSTRAINTS:
- Memory resources
- Execution time
- CPU usage

QUALITY OF REPORTS
- Organization
- Synthesis estimations
- Timing reports

USER EXPERIENCE
- Ease of use
- Customization of the tools
- Scripting capabilities

DESIGN REUSE
- IP cores provided
- generating new IP cores
- Support of reuse standards

HARDWARE INTERACTION
- Programming time
- verification of bitstream
- hardware debugging

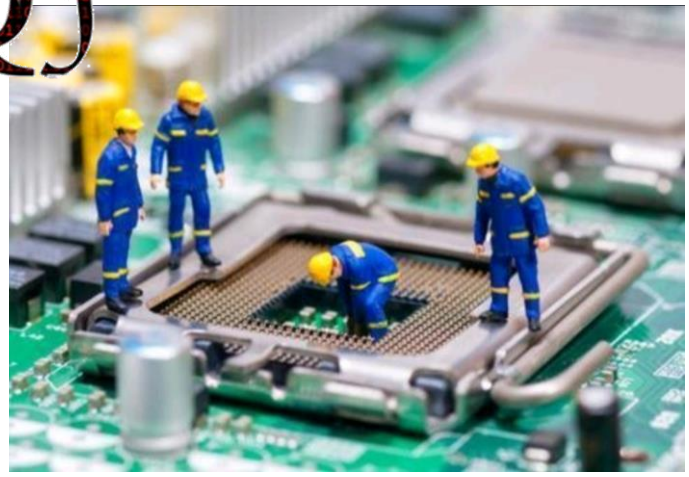
ADVANCED DESIGN FLOWS
- Floorplanning
- Incremental design
- Third-Party Integration (Simulation)

MAIN DEV. PRODUCT METRICS
- RTL Optimization
- Area vs Timing vs Power
- Constraints

QUEENS-FPGA METHODOLOGY

- Follow a systematic & unified approach throughout the tool assessment project
  1. metrics & methodology (Task1) ☑
  2. benchmark selection (Task1) ☑
  3. synthesis (Task2) ☑
  4. Place & Route (Task3) ☑
  5. 3rd party tools (Task4) ⟸
  6. HW testing (Task5) ⟸
- Different complexity level circuits
- Fair selection of comparable devices
  - Technology
  - Resources
  - Hardened
- Methodology serves a twofold purpose
  1. explore/examine multiple tool issues
     - parameters, load, trade-offs, etc.
     - compare to 3rd tools, show quality
  2. avoid dead ends & erroneous reports
     - use feedback paths, simulations

QUEENS-FPGA



QUEENS-FPGA SYNTHESIS

- Built in same technology node 65 nm, SRAM-based
- Similar in architecture/technology
  - 4 input LUTs
  - DSPs (18*18 bits)
  - Registers
  - DFFs
- Similar available resources
  - Embedded RAM blocks
  - Number of LUTs, DSPs, DFF
- Space-grade devices
  - Rad-hard High-performance devices (not so many)
- Each devices are supported by its vendor SW tool
- NanoXmap 2.6.3 -> NanoXmap 2.8.4
  (Not yet tested 2.8.5)
- Trade-off

BENCHMARK CIRCUITS

SIMPLE CIRCUITS (DC1):

- Light in terms of area utilization
- Light in effort requirement for the SW tolos
- The basics
- Simplicity

MID-COMPLEX CIRCUITS (DC2):

- Heavier in terms of area utilization
- More exigent for the SW tools
- Less complex than DC3

COMPLEX CIRCUITS (DC3):

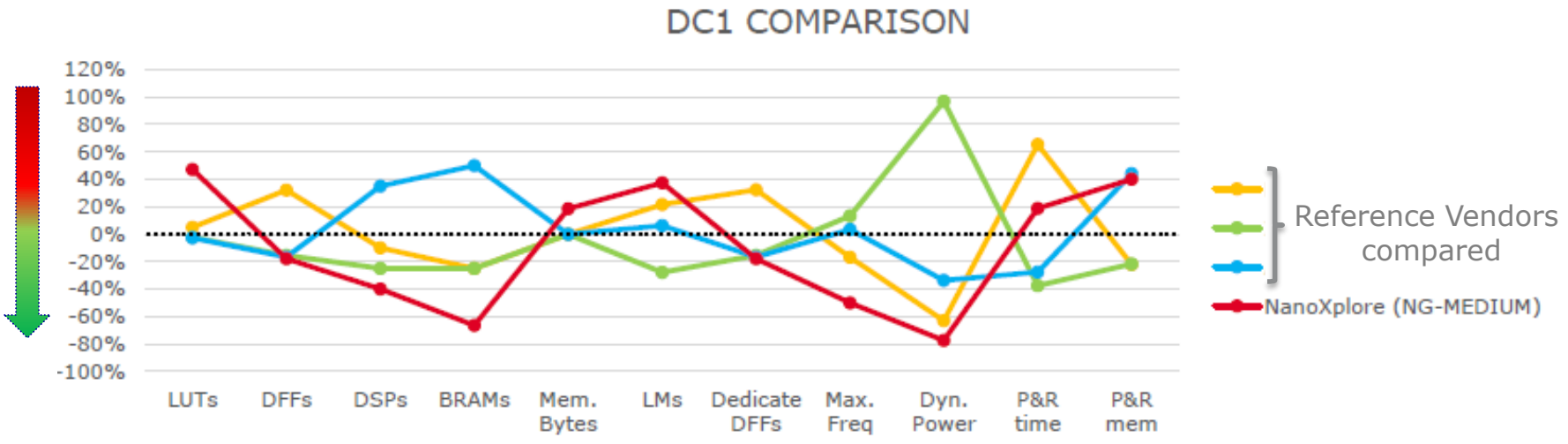
- Most complex of the designs
- Worth to elaborate a specific section for the selection
- Stress the FPGA synthesis challenges

PORTING:

- Image feature detection & tracking
  Re-design to fit in NG-MEDIUM
  up to the limits of resources

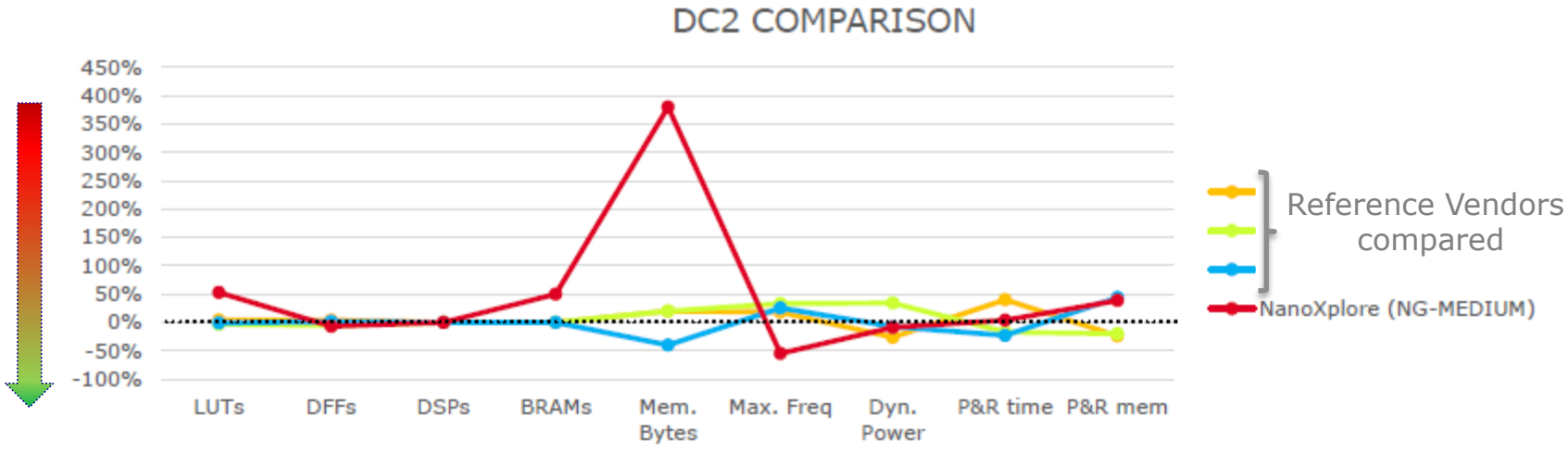
Bench-mark	Id	Configuration	Bench-mark	Id	Configuration
Multiplexor	DC1-01-C1	Case sentence	VGA controller	DC1-07-C1	Default
Multiplexor	DC1-01-C2	If-else sentence	LED controller	DC1-08-C1	Default
Multiplexor	DC1-01-C3	Concurrent sentence	32-bits FPM	DC1-09-C1	Without DSP
4 bit counter	DC1-02-C1	Asynchronous reset	32-bits FPM	DC1-09-C2	With DSP
4 bit counter	DC1-02-C2	Synchronous reset with priority enable	FIFO buffer	DC1-10-C1	18Kx18
4 bit counter	DC1-02-C3	Synchronous priority reset with enable	CAN controller	DC2-01-C1	Default
BCD counter	DC1-03-C1	Standard VHDL design method	LEON 3	DC2-02-C1	Basic
BCD counter	DC1-03-C2	2 process VHDL design method	Guess game	DC2-03-C1	Default
Register bank	DC1-04-C1	Case sentence	SDRAM controller	DC2-04-C1	Default
Register bank	DC1-04-C2	Indexed array	SpaceWire	DC2-05-C1	Default
Finite state machine	DC1-05-C1	If-else sentence	FIR	DC3-01-C1	Configuration 2
Finite state machine	DC1-05-C2	One-Hot encoding	Harrys	DC3-02-C1	Configuration 3
PWM	DC1-06-C1	Without DSP	Disparity	DC3-03-C1	Configuration 1
PWM	DC1-06-C2	With DSP	VBN	Porting	Ad-hoc

FIRST RESULTS DC1



- Overall increased number of LUTs used in low complexity designs
  - Mainly, due to use of these as pass-thru logic and suboptimal performance of arithmetic operations.
- Less maximum frequency achieved
- Efficient use of DFFs, DSPs and RAMBs in low complexity circuits
- Very low dynamic power consumption reported
- Place and route time over reference value, but still acceptable taking into account that '*Timing driven*' option has been enabled in all DC1 circuits

FIRST RESULTS DC2

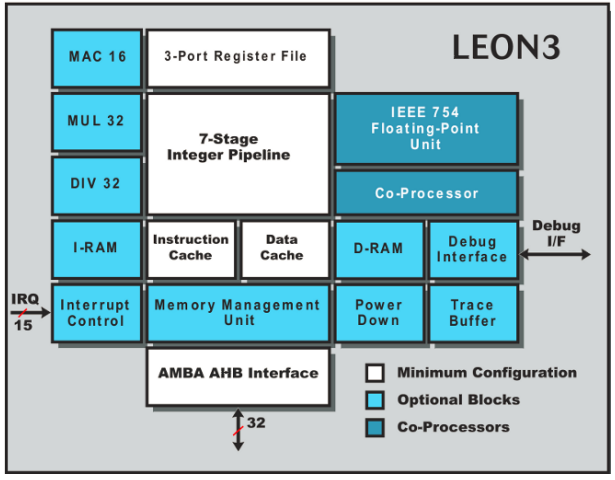


- Overall increased number of LUTs used in medium complexity designs
  - Mainly, because of the use of these as pass-thru logic and routed elements.
- Less maximum frequency achieved ~[+30% to +50%]
- Efficient use of DFFs
- Very low dynamic power consumption reported

- Better maximum frequencies are not always achieved with *'Timing driven'* option than without it
- *Timing driven'* option increases place and route time around 45%

PORTING LEON3

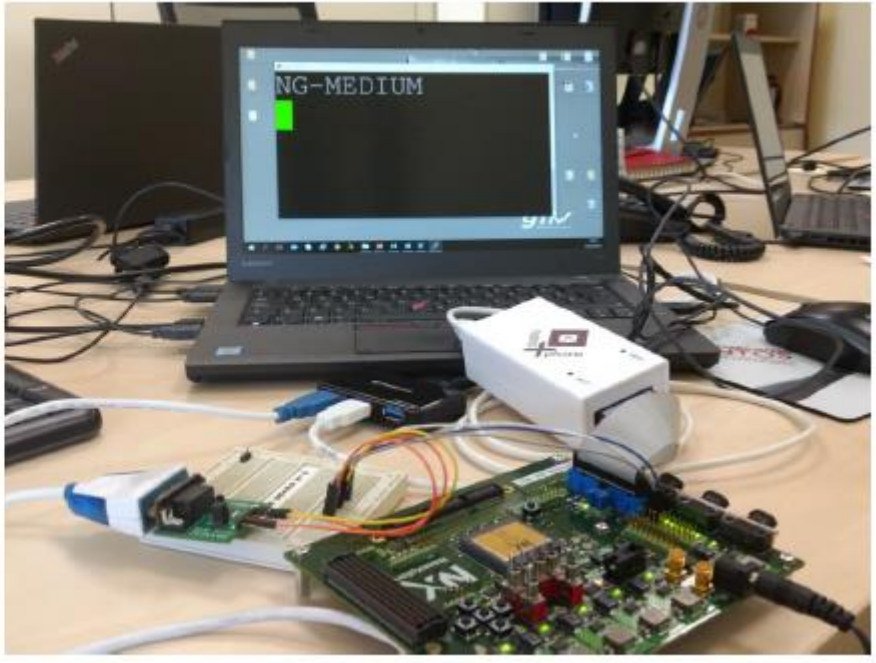
NG-MEDIUM máx freq. <= 20 MHz



1. NG-MEDIUM technology and specific hardware resources
2. NG-MEDIUM technology added to gencomp pkg with following features:
   - FPGA device
   - SRAM resources (Embedded block RAMs and Register file blocks)
   - Unavailable simultaneous read & write operations to same address in BRAMs
   - 2 ports BRAMs
   - True dual port BRAMs
   - Pads
   - Inverted output enable pad polarity
   - Embedded *clock and* resources (Clock switch component – CKS)
   - Embedded *clock generator* resources (phase-locked loop component – PLL)
3. clock generator of LEON 3 with NG-MEDIUM clock resources (PLLs and WFGs-Wave form generators). C*lock and* functionality with NG-MEDIUM resources (CKS).
4. different configurations of BRAMs are instantiated related with the size of data and address bus. In the case of memories up to 64 words the design instantiates register file blocks (RFBs) instead of BRAMs.
5. IO pads of LEON3 with the IO resources of NG-MEDIUM.
6. New technology is integrated in the GRLIB. Modify all files using the adapted components. Add IF_GENERATE
7. Different hardware in the board like DDR memories or PHY interfaces may need independent IPs to control the hardware

PORTING VISION-BASED NAVIGATION IP

- NG-MEDIUM device has limited resources
- Starting point: (1) synthesize the design as it is
- Check the result
  - If it fits, go ahead
  - If it does not fit, (2) make it fit:
    - Modify configurations of the design
    - HW/SW redesign part of the project
- Once it fits, (3) modify the design to optimise it
- Consider different communication protocols and interfaces to transfer data between board and host
- Implement the chosen interface (UART) and check it
- Add and manage communication interface to RelNav IP core
- Implement full design and take metrics



RESULTS OF VISION-BASED NAVIGATION

Reporting instances

4-LUT	DFF	XLUT	4-bits carry	Register file block	Cross domain clock	Clock switch	Digital signal processor	Memory block	WFG	PLL
19402/32256 (61%)	7397/32256 (23%)	860/2016 (43%)	779/2016 (39%)	0/168 (0%)	0/168 (0%)	0/336 (0%)	21/112 (19%)	37/56 (67%)	1/32 (4%)	0/4 (0%)

Reporting Detail of 4-LUTs use

Synthesized From HDL	Used by DFF	CY	RF	CDC	CKS	Internal	Total	Total 4-LUT Count
11720	3864	2687	0	0	0	1131	7682	19402/32256 (61%)

Reporting Detail of Register use

SFE	Carry	Dff sub-total	CDC	CKS	RF	DSP	RAM	Pads	Total
6989	408	7397/32256 (23%)	0	0	0	980	0	0/1122 (0%)	8377

Options:

UseNxLibrary: Yes
DefaultFSMEncoding: Binary
DefaultRAMMapping: RAM
DefaultROMMapping: LUT
MaxRegisterCount: 10100
ManageUnconnectedOutputs: Error
ManageUnconnectedSignals: Error

MappingEffort: High
MergeRegisterToPad: Never
AdderToDSPMapThreshold: 0
LessThanToDSPMapThreshold: 0
MultiplierToDSPMapThreshold: 1

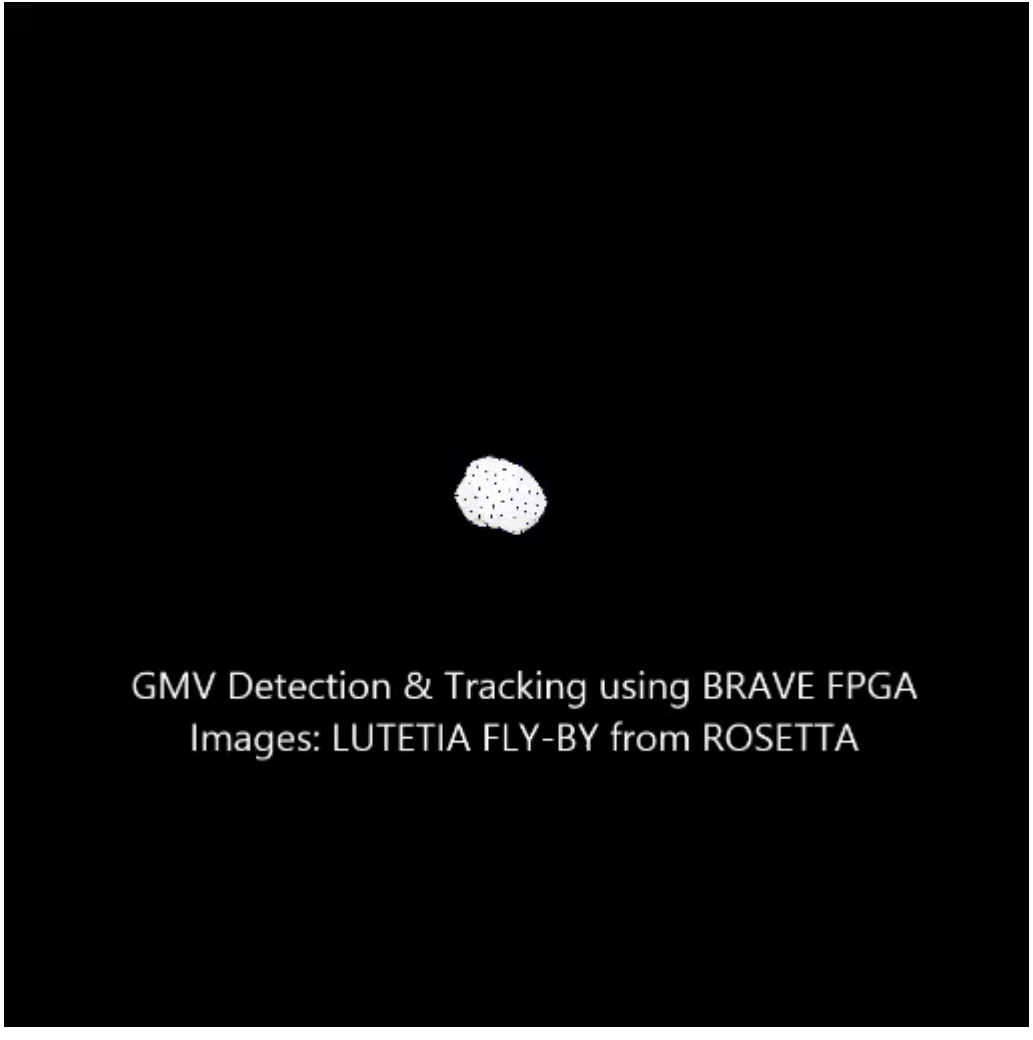
TimingDriven: No

Last Version of NanoXmap v2.8.5

Metric	NanoXmap	Vendor 1
LUTs	19402	7386 (6-in)
DFFs	7397	3526
DSPs	21	16
BRAMs	37	58
Total Memory (Kbits)	1776	1044
Max. Freq (MHz)	39	145
Dynamic Power Consumption	0,37W	1,33W
Static Power Consumption	0,73W	3,5W

RESULTS

- Very preliminary Demo, cheating just a bit:
  - Not in real-time
  - Not in closed loop
  - HW/SW split



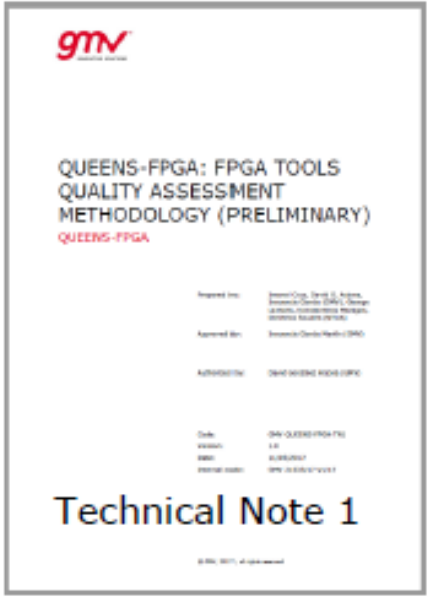
PRELIMINARY CONCLUSIONS

- Architecture Matters: Learn how to optimize design for the new board architecture
- Porting → wrappers over specific HW resources (DSPs, BRAMs)
- Very responsive Vendor support team.
- Improvements version by version
  - Corner cases or different improvement targets make some parameter worse
- NG-MEDIUM is in the market → NanoXplore is an actual competitor → Portfolio increasing → Good for Industry

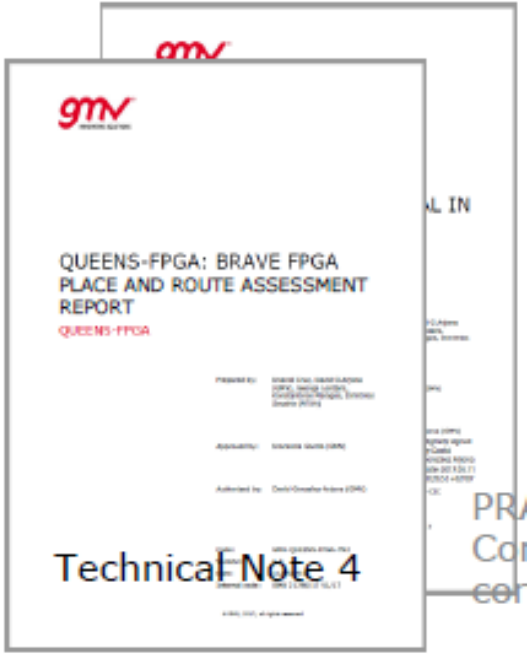
- Great improvement of generated reports in 2.8.3 version
- Efficient use of DFFs in low and medium complexity designs
- Reduced use of LUTs and DFFs when RAMB or DSP are used in low and medium complexity designs.
- Very low dynamic power consumption reported
- Competitive implementation times

- Increased use of LUTs compared to 3rd party tools ~[+10% to +60%] → Depends on reporting (LUTs for HDL, LUTs pass-through) [architecture matters].
- Lower maximum frequencies achieved ~[+30% to +50%]
- Less flexibility to tailor elements in designs

MORE FROM QUEENS-FPGA



Application to NanoXplore FPGA SW tools



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BACKGROUND
EXPERIENCE

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Questions? Suggestions?

EXOMARS
- EDM-ExoMars 2016
- GNC Exomars 2020
- SVF+OBC Simulator

Phobos

Mars

Phobos Sample Return
- GNC-PHOOT
- NEOGNC2-IP-NPAL
- CAMPHORVNAV
- MREP Camera

HW Reconfiguration
- ENABLE-S3
- CORA-MBAD
- PEPS

Asteroid Sample Return
- NEOGNC-2 (Marco Polo-R)

Itokawa

VEGA, ARION1, GETDEN TSN, TME Launchers

NEO Impact Prevention
- NEOShield-2

1996FG3

Earth

Moon

Active Debris Removal
- ***e.Deorbit***
- HIPNOS/ORCO

Didymos

Asteroid Deflection Mision
- AIM (AIDA)

HW-in-the-loop test
- ***platform–art®***
- Optical Nav Lab
- ATB Avionics Testbed

Re-entrant Vehicle
- IXV
- Space Rider

Moon Exploration
- Lunar Lander
- LL-VNHDA
- Pilot B+

Rovers Exploration
- Opportunistic Science, Spartan/Sextant/Compass
- LUCID/RAT

Jupiter

Ganimedes

JUICE
- Proposals for: JUICE Navcam, SW StarTracker

Callisto

Europa

ROSETTA

Operations support, mission studies, IP

Comet 67P/Churyumov-Gerasimenko

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THANK YOU

David Gonzalez-Arjona

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