Xilinx—Re-configurable FPGAs for Space

➢ Dynamically re-configurable digital logic FPGA for space borne processing needs
➢ Hardware built and integrated into Spacecraft pending launch for many programs
  ★ Many active V5QV designs in Commercial, Civil, and Military applications
➢ Silicon functionality, IPs, radiation, reliability, tool chains all validated through extensive qualification tests and user testing
  ★ All functional blocks validated with radiation, upset rate published
  ★ Thermo-mechanical manufacturing process implementations well established and qualified at leading Space contractors and agencies
  ★ XRTC Radiation Reports available in Xilinx Space Lounge
➢ Major flight heritage accumulated since 2014
➢ QML-Y certification in process
➢ V5QV mature product in stable production accumulating heritage
  ★ Life cycle extended to late 2020s
  ★ Screened devices with 30% lower static power now available
Power Screened V5QV Devices via SCD4591

Streamlined Specification:
XQR5VFX130-1CN1752B4591,
XQR5VFX130-1CN1752V4591

Description
The device(s) listed in Table 1 conforms to the production device data sheet with the known deviations listed below.

Table 1

<table>
<thead>
<tr>
<th>Applicable Ordering Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>XQR5VFX130-1CN1752B4591</td>
</tr>
<tr>
<td>XQR5VFX130-1CN1752V4591</td>
</tr>
</tbody>
</table>

Custom Specification
The deviations from the production data sheet are:
This SCD changes the test sample for total device static ICCRQ current from a standard limit of 8A at 125C to 3.6A at 125C as specified in the "Radiation-Hardened, Space-Grade Virtex-5QV FPGA Data Sheet: DC and AC Switching Characteristics", DS692 (v1.3.1) January 16, 2015 Product Specification Table 4, note 4.

Radiation-Hardened, Space-Grade Virtex-5QV FPGA Data Sheet DS692

Important Note
Typical values for quiescent supply current are now specified at nominal voltage, 125°C junction temperatures (Tj). Xilinx recommends analyzing static power consumption at Tj = 125°C because the majority of designs operate near the high end of the temperature range. Data sheets for order products (e.g., Virtex-4QV devices) still specify typical quiescent supply current at Tj = 25°C. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: Typical Quiescent Supply Current

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Device</th>
<th>Typical ICCRQ</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICRQ</td>
<td>Quiescent ICCRQ supply current</td>
<td>XQR5VFX130</td>
<td>6344mA</td>
<td>mA</td>
</tr>
<tr>
<td>ICCQ</td>
<td>Quiescent ICCQ supply current</td>
<td>XQR5VFX130</td>
<td>12</td>
<td>mA</td>
</tr>
<tr>
<td>ICCQ</td>
<td>Quiescent ICCQ supply current</td>
<td>XQR5VFX130</td>
<td>304</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
1. Typical values are specified at nominal voltage, 125°C junction temperatures (Tj).
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, and IO pins are 3-state and floating.
3. If DC or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Xilinx Power tool.
4. Maximum ICCRQ is 8A, specified at maximum VCCINT and 125°C junction temperature (Tj).

XPE for SCD4591 screened parts available on Space Lounge for SCD4591:
- https://www.xilinx.com/member/space/Virtex5_Virtex6_XPE_14_3_rev2.zip

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Xilinx Class “Y” Update

Xilinx chip capacitor vendor received conditional DLA slash sheet approval
- Conditional screening defined for increased voltage stress
- Vendor able to deliver chip capacitors meeting defined conditional screening in June, 2019
  • Delays V5QV Class “Y” shipments to Q4’2019
  • No impact to plans for XQRKU060 Class “Y”
Missions with Virtex-5QV – More in Pipeline

M-Cubed/COVE-2 Mission (2013)
A CubeSat design to validate the Virtex-5 FPGA for spaceborne image processing
- Dmitriy L. Bekker; Thomas A. Werne; Thor O. Wilson; Paula J. Plangger; Kilil Donchev; Michael Heywood; Rafael Ramos; Brad Freyberg; Fernando Saca; Brian Gilchrist; Alec Gallimore; James Culler

Glonass-K (2014)

Formosat-5 (Launched August 24th 2017)
FORMOSAT-5 Development & Metrology Application
- Ho-Pen Chang; Way-Jin Chen

Iridium Next (66+6+9)
See Xilinx Press Release (First 50 Satellites deployed)
“High performance, high volume reconfigurable processor architecture”
Paul Murray; Tres Randolph; Damon Van Buren; David Anderson; Ian Troxel
2012 IEEE Aerospace Conference

NovaSAR (2018 Launch)
“NovaSAR-S low cost spaceborne SAR payload design, development and deployment of a new benchmark in spaceborne radar”
- Martin Cohen; Andy Larkins; Pedro Lau Semedo; Geoff Burbidge

Cosmo Skymed NextGen (2018 Launch)

SARah (2019 Launch)

DLR H2 Comm. Sat. (2020 Launch)
“An FPGA based on-board processor platform for space application”
- Alexander Hofmann; Rainer Wansch; Robért Glein; Bernd Kollmannthaler
2012 NASA/ESA Conference on Adaptive Hardware and Systems (AHS)

Multiple U.S. Classified Programs

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Paradigm Shift in Satellite Design

Marco Caceres, senior analyst and director of space studies for Virginia-based Teal Group consulting firm

“We expect that the next 10 years will see an increase of about 25 percent in the number of new spacecraft of 50Kg mass or larger. These new spacecraft will have more sophisticated payload electronics than their predecessors, doing more on-board data processing to maximize data acquisition while dealing with limited downlink bandwidth.”

Marco Caceres, senior analyst and director of space studies for Virginia-based Teal Group consulting firm

Paradigm shift to Satellite on-board, autonomous processing drives need for very high performance reconfigurable electronics in space

“Bent Pipe”

Telemetry control: 10s of MOPS

Signal processing & data switching: 100s of GOPS

“On-board Processing”

Telemetry control: 10s of MOPS

Signal processing & data switching: 100s of GOPS

Paradigm shift to Satellite on-board, autonomous processing drives need for very high performance reconfigurable electronics in space
Key Xilinx Space Product Applications– On-Board Processing (OBP)

➢ Communication Digital Payloads:
  – Channelizer – RX/TX module, DSP Switches
  – High frequency down converter, Modulation, De-Modulation
  – Beamforming Modems & Crypto Unit, Ethernet Routers/Switches
  – Payload frequencies reconfiguration - defeating jamming threats

➢ Imaging (remote sensing, space telescopes):
  – ADC data conversion, Imaging data processing & compression

➢ Synthetic Aperture Radar (SAR)
  – High Speed Digitizer, Timing Generator Module, Baseband data processing, data compression, mass memory storage

➢ GPS – Digital Waveform Generators

➢ Manned Crew Capsules
  – Video processor and Displays for Crew Capsules
  – C&DH (Command and Data Handling)
XQR Kintex UltraScale KU060 for Space Applications
Radiation Feasibility test data for XQRKU060

➢ Existing Kintex UltraScale Radiation Feasibility Test Data indicate XQRKU060 will meet Space customer needs – no need for RHBD re-design

− NASA Testing showed no SEL up to 40 MeV-cm²/mg on Kintex UltraScale parts

− Sandia National Laboratories testing showed no Single Event Latch-up (SEL) up to 79.2 MeV-cm²/mg

★ “Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation”

★ “An Analysis of High-Current Events Observed on Xilinx 7-Series and Ultrascale Field-Programmable Gate Arrays”

• Xilinx testing on Kintex UltraScale

★ No SEL susceptibility seen in testing up to 58 MeV-cm²/mg

★ X-Ray Total Ionizing Dose (TID) test results good in testing up to 100 Krad
Space (XQR) Kintex UltraScale Product

Kintex UltraScale Advantage for Space Applications
- Deploys same commercial silicon mask set and 20nm wafer processing
- Vivado Ultrafast Development Advantage
  - High Level Synthesis (HLS)
  - Block-based IP Integration with Vivado IP Integrator
  - Accelerated design implementation achieved through analytical place and route technology

Packaged in 40mm x 40mm Ceramic Column Grid Array (CCGA)
- XQRKU060-CNA1509 will be footprint compatible with commercial A1517 pin out
- Ceramic package loses 2 additional solder columns in each corner
  - 1 XCVR
  - 4 HP-IO

Product Space Test Flows
- B-Flow = QML-Q Equivalent
- Y-Flow = QML-Y Compliant
  - MIL-PRF-38535 Revision K defines requirements for ceramic non-hermetic packages in space applications, designated as Class Y

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XC Commercial Package Transceiver Locations

The ceramic package (CNA1509) pinout for Space Product compatible with A1517 configuration

- Difference being additional two pins in each corner removed from Ceramic Column Grid Array package for shock, vibe, and handling considerations
- Ceramic package loses 2 additional solder columns in each corner
  - 1 XCVR
  - 4 HP/IO

- In the case of the A1517 => A1509 I/O pins to avoid or not use:

<table>
<thead>
<tr>
<th>Bank/Quad</th>
<th>Pin</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quad 224</td>
<td>AV1</td>
<td>MGTHRXN1, thus also AV2 (MGTHRXP1) – Relocated to T1/T2</td>
</tr>
<tr>
<td>Bank 25</td>
<td>AV39</td>
<td>IO_L8N, thus AV38 (IO_L8P) unusable as differential pair</td>
</tr>
<tr>
<td>Bank 25</td>
<td>AV38</td>
<td>Single-ended IO</td>
</tr>
<tr>
<td>Bank 46</td>
<td>A38</td>
<td>(IO_L17N), thus also A37(IO_L17P) unusable as differential pair</td>
</tr>
<tr>
<td>Bank 46</td>
<td>B39</td>
<td>(IO_L16N), thus also C38(IO_L16P) unusable as differential pair</td>
</tr>
</tbody>
</table>

UG575 UltraScale and UltraScale+ FPGAs Packaging and Pinouts
# XQRKU060 Select-IO Data Rate Targets

**I/O Performance targets consistent with Kintex UltraScale -1 (.95V) performance targets:**

- **DDR IO rates**
  - DDR4 (HP I/O) 2133 Mb/s
  - DDR3 (HP I/O) 1866 Mb/s
  - DDR3L (HP I/O) 1600 Mb/s
  - DDR3L (HP I/O) 1600 Mb/s

- **QDR IO Rates**
  - QDR II+ (HP I/O) 550 MHz
  - QDRIV (HP I/O) 667 MHz
  - RLDRAM 3 (HP I/O) 933 MHz

- **LVDS Component mode (Legacy using HDL)**

<table>
<thead>
<tr>
<th>LVDS IO Rates</th>
<th>HP</th>
<th>HR</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX DDR (OSERDES 4:1, 8:1)</td>
<td>1250</td>
<td>1000</td>
</tr>
<tr>
<td>TX SDR (OSERDES 2:1, 4:1)</td>
<td>625</td>
<td>500</td>
</tr>
<tr>
<td>RX DDR (ISERDES 1:4, 1:8)(1)</td>
<td>1250</td>
<td>1000</td>
</tr>
<tr>
<td>RX SDR (ISERDES 1:2, 1:4)(1)</td>
<td>625</td>
<td>500</td>
</tr>
</tbody>
</table>

Notes:

1. LVDS receivers typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms used to achieve maximum performance

- **LVDS Native mode (Using Wizard)**

<table>
<thead>
<tr>
<th>LVDS IO Rates</th>
<th>HP-min</th>
<th>HP-max</th>
<th>HR-min</th>
<th>HR-max</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX DDR (TX_BITSLICE 4:1, 8:1)</td>
<td>300</td>
<td>1400</td>
<td>300</td>
<td>1250</td>
</tr>
<tr>
<td>TX SDR (TX_BITSLICE 2:1, 4:1)</td>
<td>150</td>
<td>700</td>
<td>150</td>
<td>625</td>
</tr>
<tr>
<td>RX DDR (RX_BITSLICE 1:4, 1:8)(2)</td>
<td>300</td>
<td>1400</td>
<td>300</td>
<td>1400</td>
</tr>
<tr>
<td>RX SDR (RX_BITSLICE 1:2, 1:4)(2)</td>
<td>150</td>
<td>700</td>
<td>150</td>
<td>625</td>
</tr>
</tbody>
</table>

Notes:

1. Native mode supported through High-Speed SelectIO Interface Wizard available with Vivado Design Suite.
2. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

LVDS Information above per DS892 Tables 24 and 25

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UltraScale Documentation

- **DS890** Architecture and Product Overview
- **DS892** Kintex UltraScale FPGAs Data Sheet

### White Papers
- **WP434** Xilinx UltraScale Architecture for High-Performance, Smarter Systems
- **WP446** Comprehensive JESD204B Solution Accelerates and Simplifies Development
- **WP451** UltraScale Architecture Low Power Technology Overview
- **WP454** High-Performance, Lower-Power Memory Interfaces with the UltraScale Architecture
- **WP458** Leveraging UltraScale Architecture Transceivers for High-Speed Serial I/O Connectivity

### User Guides
- **UG570** UltraScale Architecture Configuration
- **UG571** UltraScale Architecture SelectIO
- **UG572** UltraScale Architecture Clocking Resources
- **UG573** UltraScale Architecture Memory Resources
- **UG574** UltraScale Architecture CLB
- **UG575** UltraScale and UltraScale+ FPGAs Packaging and Pinouts
- **UG576** UltraScale Architecture GTH Transceivers
- **UG579** UltraScale Architecture DSP Slice
- **UG580** UltraScale Architecture System Monitor
- **UG583** UltraScale Architecture PCB Design

### Product Guides
- **PG150** UltraScale Architecture-Based FPGAs Memory Interface Solutions
- **PG156** UltraScale Devices Gen3 Integrated Block for PCI Express
- **PG182** UltraScale FPGAs Transceivers Wizard

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Alpha Data Space Development Kit

**ADA-SDEV-KIT**

**Development Kit for XQRKU060**

Modular design with:
- Commercial XCKU060 in -1 speed grade
- XRTC compatible Configuration Module
- Two FMC Sites
- DDR3 DRAM
- System Monitoring
- Space-Grade Compatible Power Regulators

**Product Details**
www.alpha-data.com/sdev

**Datasheet**  **Manual**  **Ref Designs**
## For retro-perspective: V4QV & V5QV Resource Table

<table>
<thead>
<tr>
<th></th>
<th>XQR4V (Radiation Tolerant, 1.2V)</th>
<th>XQR5V (RH-BD, 1.0V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SX55</td>
<td>55,296</td>
<td>131,072</td>
</tr>
<tr>
<td>FX60</td>
<td>56,880</td>
<td></td>
</tr>
<tr>
<td>FX140</td>
<td>142,128</td>
<td></td>
</tr>
<tr>
<td>LX200</td>
<td>200,448</td>
<td></td>
</tr>
<tr>
<td>Logic Cells</td>
<td>55,296</td>
<td>131,072</td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>49,152</td>
<td>81,920</td>
</tr>
<tr>
<td>Distributed RAM (Kbits)</td>
<td>384</td>
<td>1,580</td>
</tr>
<tr>
<td>Total Block RAM (Kbits)</td>
<td>5,760</td>
<td>10,728</td>
</tr>
<tr>
<td>Digital Clock Manager (DCM)</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>Phase Lock Loop (PLL)</td>
<td>---</td>
<td>6</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>512</td>
<td>320</td>
</tr>
<tr>
<td>350 MHz PPC405 Cores</td>
<td>512</td>
<td>---</td>
</tr>
<tr>
<td>10/100/1000 EMACs</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>Multi-Gigabit Transceivers (MGT)</td>
<td>---</td>
<td>18</td>
</tr>
<tr>
<td>TID (krad)</td>
<td>300</td>
<td>1,000</td>
</tr>
<tr>
<td>SEL Immunity (LETs)</td>
<td>&gt;125</td>
<td>&gt;125</td>
</tr>
<tr>
<td>Package Size (mm)</td>
<td>35 x 35 mm</td>
<td>45 x 45 mm</td>
</tr>
<tr>
<td>Pin Counts</td>
<td>1140</td>
<td>1752</td>
</tr>
<tr>
<td>Max. IO Count</td>
<td>640</td>
<td>840</td>
</tr>
<tr>
<td>Daisy Chain</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Next Generation Xilinx Space Product XQRKU060-CNA1509

**Space Product (XQR) Plan of Record** Kintex® UltraScale™ FPGA

<table>
<thead>
<tr>
<th>Device Name</th>
<th>XQRKU060</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Logic Cells (K)</td>
<td>726</td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>663,360</td>
</tr>
<tr>
<td>CLB LUTs</td>
<td>331,680</td>
</tr>
<tr>
<td>Maximum Distributed RAM (Kb)</td>
<td>9,180</td>
</tr>
<tr>
<td>Block RAM/FIFO w/ECC (36Kb each)</td>
<td>1,080</td>
</tr>
<tr>
<td>Block RAM/FIFO (18Kb each)</td>
<td>2,160</td>
</tr>
<tr>
<td>Total Block RAM (Mb)</td>
<td>38</td>
</tr>
<tr>
<td>CMT (1 MMCM, 2 PLLs)</td>
<td>12</td>
</tr>
<tr>
<td>I/O DLL</td>
<td>48</td>
</tr>
<tr>
<td>Maximum Single-Ended HP I/Os</td>
<td>520</td>
</tr>
<tr>
<td>Maximum Differential HP I/O Pairs</td>
<td>240</td>
</tr>
<tr>
<td>Maximum Single-Ended HR I/Os</td>
<td>104</td>
</tr>
<tr>
<td>Maximum Differential HR I/O Pairs</td>
<td>48</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>2,760</td>
</tr>
<tr>
<td>System Monitor</td>
<td>1</td>
</tr>
<tr>
<td>PCIe® Gen1/2/3</td>
<td>3</td>
</tr>
<tr>
<td>Interlaken</td>
<td>0</td>
</tr>
<tr>
<td>100G Ethernet</td>
<td>0</td>
</tr>
<tr>
<td>12.5Gb/s Transceivers (GTH)</td>
<td>32</td>
</tr>
<tr>
<td>Military (-55°C to +125°C)</td>
<td>-1</td>
</tr>
</tbody>
</table>

### Package Footprint

<table>
<thead>
<tr>
<th>Package</th>
<th>Package Dimensions (mm)</th>
<th>HR I/O, HP I/O, GTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1517</td>
<td>40x40</td>
<td>104, 520, 32</td>
</tr>
<tr>
<td>CNA1509</td>
<td>40x40</td>
<td>104, 516, 31</td>
</tr>
</tbody>
</table>
Preliminary XQRKU060-CNA1509 Schedule

➢ Early programs proceeding directly to development
  - Pin compatible commercial XCKU060/A1517 device available now!
  - Target XCKU060-1FFVA1517I (-1 Speed Grade) in Vivado software
  - Alpha Data Space Development Kit (ADA-SDEV-KIT)

➢ Flight Part Schedule
  - April 2018 – Package Design Release
  - October 2018 – All piece parts available to begin assembly and test of qualification units
  - December 2018 – Pre-qualification Ready (Operations Space Test Flow hardware and procedures)
  - June 2019 – Complete pre-qualification validation with full qualification unit quantities
  - December 2019 – “B” Availability XQRKU060-CNA1509B
  - December 2020 – “Y” Availability XQRKU060-CNA1509Y
Kintex UltraScale (KU060) Architecture for Space Applications
Vivado Design Suite Enables the UltraScale Advantage

Next Generation Implementation

ISE Design Suite (simulated annealing)

Vivado Design Suite (Analytical Placer)

Timing Cost \( f(x) \)

Placement Solution \( x \) (found by random moves and seeds)

initial random seed

Local moves

not routable

best solution found

optimal solution (not found)

Next Generation Implementation
UltraScale Re-Architects the Core

Highest Utilization at Maximum Performance

Next Generation Routing

- Re-designed routing architecture
- 2X routing, agile switching
- Co-Optimized with Vivado

ASIC-Like Clocking

- Regional, segmented structure
- Flexible clock placement
- Scales w/density to balance skew

System Logic Cells

- Higher utilization enabled by routing
- Shorter net delays for performance
- Less wire switching for lower power

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## Enhanced DSP Sub-Systems for Performance and Efficiency

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| 27x18 multiplier in a DSP slice; 35x28 support in a DSP tile (2 slices) | • Optimal performance per block  
• Implement double-precision floating point in two-thirds the fabric |
| Pre-adder squaring                           | • More efficient motion estimation in video applications  
• Perform “sum-of-square-difference” calculations in 50% fewer resources |
| Extra accumulator feedback path              | Implement complex multiply-accumulate in half the resources             |
| Wide XOR                                     | Implement EFEC, CRC, ECC functionality                                 |
| White box modeling                           | Full visibility with accurate simulation and debug                       |

**Figure:** Enhanced DSP Sub-Systems with 5 high speed interconnects.
Xilinx DSP Design Flow

- Floating-point and Fixed-point Hardware Generation
- World class C/C++ design flow
- Real time analog data acquisition
Vivado High-Level Synthesis:
Accelerated IP Development and Design Space Exploration

- **Comprehensive coverage**
  - C, C++, SystemC
  - Arbitrary precision
  - Floating-point

- **Accelerated verification**
  - Magnitudes of order (2-3) faster than RTL for large blocks

- **Fast compilation and design exploration**
  - Algorithm feasibility
  - Architecture Iteration

- **Customer proven results**
## Optimized Block RAM Alleviate Bottlenecks for Many Applications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Built in high speed memory cascading</td>
<td>Eliminates CLB usage, reduces routing congestion &amp; dynamic power consumption</td>
</tr>
<tr>
<td>Enhanced FIFO</td>
<td>• Lower power, greater performance than soft FIFO</td>
</tr>
<tr>
<td></td>
<td>• Easy migration to soft core implementation for additional functionality</td>
</tr>
<tr>
<td></td>
<td>• Asymmetric read and write port widths for clock domain crossings</td>
</tr>
<tr>
<td>User-accessible power gating of active BRAM</td>
<td>Reduces dynamic power when access to BRAM contents is temporarily not needed</td>
</tr>
</tbody>
</table>

### 7 Series (2k x 36 RAM)

- Decoder (logic fabric)
- DIN
- Addr
- BRAM 512 x 36
- 512x36
- BRAM 512 x 36
- 512x36
- BRAM 512 x 36
- 512x36
- DOUT

### UltraScale (2k x 36 RAM)

- Decoder (logic fabric)
- DIN
- Addr
- EN
- DOUT
- BRAM 512 x 36
- EN
- BRAM 512 x 36
- EN
- BRAM 512 x 36
- EN
- BRAM 512 x 36
- EN
- DOUT (hardened multiplexers)
## Delivering Massive I/O Serial Bandwidth

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| GTH                           | • 12.5Gb/s performance in -1 Speed and Military Temperature Grade  
                                • Enabled Standards:  
                                • PCIe Gen3  
                                • JESD204B  
                                • Xilinx Aurora  
                                • Serial RapidIO (SRIO) – [Space VPX (VITA 78)](https://www.vita.org/) / Next Generation Space Interconnect Standard (NGSIS)  
                                • NGSIS IP Core from Alliance Program Partner, Praesum Communications, developed on UltraScale Architecture |
| Major power reduction         | ~40% lower power over 7-Series for 10G backplanes                                                                                                                                                       |
| Continuous auto-adaptive equalization | Continuously optimizes link margin over PVT in increasingly challenging channel conditions                                                                                                           |

![Graph showing 2x Aggregate Bandwidth (Gb/s)](image)

- **Kintex UltraScale**: GTH  
- **Virtex UltraScale**: GTH  
- **GTH**: 30.5 Gb/s  
- **GTY**: 16+ Gb/s  
- **2x Aggregate Bandwidth (Gb/s)**:  
  - Kintex UltraScale (GTH): 2,784  
  - Virtex UltraScale (GTH): 5,616  
  - Virtex UltraScale (GTY): 1,536  

![Graph showing Half the Power](image)

- **10G Backplanes**:  
  - 7 Series: ~40% Lower  
  - UltraScale:  

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Auto-Adaptive Receiver Equalization in Action

Transceiver Architecture

- Hard PCS Logic
- PSD
- PLL
- RX CDR
- RX DFE
- RX CTLE
- RX AGC
- TX Driver
- Pre-emphasis
- TX PKG
- RX PKG

2-D Eye Scan

- Open Eye at Transmitter
- Closed Eye at Receiver
- Open Eye Post-Equalization

Lossy Channel

VIVADO Serial I/O Analyzer

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UltraScale Device Configuration Options for PCIe

120ms Guarantee

None

Tandem

Initial Configuration
• Tandem PROM
• Tandem PCIe

Updates after Initial Configuration
• Not Available

Tandem with Field Updates

Initial Configuration
• Tandem PROM
• Tandem PCIe

Updates after Initial Configuration
• Via PCIe

Partial Reconfiguration Over PCIe

Vivado Flow
• Project
• Non-project

Vivado Flow
• Project
• Non-project

Vivado Flow
• Project
• Non-project

Notes:
1: See Vivado Design Suite User Guide Partial Reconfiguration (UG909) for Project mode details
2: See PG156 UltraScale Devices Gen3 Integrated Block for PCI Express "Tandem Configuration"

First stage bitstreams are not compatible
MicroBlaze Triple Modular Redundancy (TMR) Subsystem

Micro-controller systems

 Derived from MicroBlaze TMR designed for Zynq Ultrascale+ MPSoC PMU & CSU
  – Add redundancy to detect failures and recover from faults without disrupting application
  – Use Vivado IP Integrator to automate creation of a TMR system using handful of new IPs
  – Partitioning into IP building blocks with automated triplication in Vivado

 MicroBlaze TMR Fundamentals
  – Triplication (TMR) for Fail Tolerant–Fail Safe (FT-FS)
    • First failure; continue nominal operation without degradation
    • Second failure; detect failure and halt operation
  – Duplication (Lockstep) for Fail-Safe (FS)
    • First failure; detect failure and halt operation

 Triplicate MicroBlaze sub-system
  – Voting at boundary
  – Recovery of failing CPU under SW control (seen by application as servicing interrupt)

 MicroBlaze Triple Modular Redundancy (TMR) Subsystem v1.0 Product Guide
Space Policy for non-XQR Parts

It is the stated policy of Xilinx to only provide radiation performance data, guidance or support for the use of Xilinx products in Space Radiation Environment applications for products designated as Xilinx Space (XQR) products. As such, Xilinx will not provide this type of data, guidance or support for non-XQR products. The Space Radiation Environment is a branch of astronautics, aerospace engineering and space physics that seeks to understand and address conditions existing in space that affect the design and operation of spacecraft, launch vehicles and associated electronic systems. Only Xilinx Space (XQR) products are specified and endorsed for use in the space environment. The Xilinx standard terms and conditions1 state that the Xilinx Limited Warranty does not apply to and excludes to the maximum extent permitted by applicable law “Products used in an application or environment that is not within the Specifications”. Customers choosing to use Xilinx products in space environments that are not specified for use in space do so entirely at their own risk.

• Xilinx continues to support Xilinx Radiation Test Consortium (XRTC) weekly conference calls and annual meeting
• Xilinx does post XRTC proceedings from annual meeting in the Xilinx Space Lounge under agreement with XRTC
• Do note that the XRTC is a distinct and separate organization from Xilinx
• Current chairperson for the XRTC is Gary Swift, who can be contacted via the information below:

Swift Engineering and Radiation Services, LLC
408-628-4803 (landline) or 408-679-3785 (cell)
email: gary.m.swift@ieee.org
http://xrtc.groups.et.byu.net/wiki/doku.php

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Space 2.0 Approach

- Lowest risk choices are V4QV and V5QV space products, then schedule permitting XQRKU060
  - Space products available in Ceramic Column Grid Array package with Space Test flows (“B”, “V”, “Y”)
- With Space Policy clearly in mind, for select programs with approved business case discussions for non-XQR product following conditions apply
  - Customer must be capable and willing to use a Defense Grade (XQ) product
    - Defense Grade (XQ) value attributes appeal to their needs, such as:
      - Full range extended temperature testing at Military temperature extremes
      - Full compliance with MIL-PRF-38535 Pb content standards
      - Ruggedized packaging- MIL-STD-883 group D Qualification tested for Defense Grade products prior to product release
  - Single Lot Date Code (SLDC) orders possible for customer to perform their own additional qualification
    - Orders must be NCNR- Customer takes on the Lot Jeopardy, not Xilinx
    - SLDC option incurs increased pricing (contact factory)
  - Total Ionizing Dose (TID) testing requires significant NRE for initial setup and characterization
  - High Temperature Operating Life testing requires an even larger NRE and is strongly discouraged
  - No Single Event Effect performance test requests:
    - Customer must either work with the XRTC or make determination from their own independent testing results