Single Event Characterization of a Xilinx UltraScale+ MP-SoC FPGA

Thomas LANGE, Maximilien GLORIEUX, Adrian EVANS, A-Duong IN, Thierry BONNOIT, Dan ALEXANDRESCU
  iRoC Technologies – France

Cesar BOATELLA POLO, Carlos URBINA ORTEGA, Veronique FERLET-CAVROIS
  ESA/ESTEC – Netherlands

Maris TALI, Ruben GARCIA ALIA
  CERN – Switzerland/France

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  Tuesday, April 10th 2018

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Outline

- Motivation
- Test Setup
- Facilities
- Test Results
- Conclusion and Future Work
ESA project to study radiation sensitivity of components operating in JUICE environment

- 3 classes of devices tested
  - Commercial SRAMs
  - SRAM-Based FPGA
  - CPU/SoC

- All devices tested under
  - ✓ Heavy Ions (UCL, CERN H8)
  - ✓ High Energy Electrons (VESPER)
  - ✗ High Energy Protons (PSI in May 2018)
  - ✓ Low Energy Protons (RADEF)
Motivation – XCZU3EG Overview (1)

- Latest generation Xilinx MP-SoC
  - Ultrascale architecture FPGA
  - ARM based processing system (4x A53 + 2x R5)
  - Manufactured in TSMC FinFET 16nm Technology
### Characteristics of Zynq Ultrascale+ EG devices

<table>
<thead>
<tr>
<th>Device Name</th>
<th>ZU2EG</th>
<th>ZU3EG</th>
<th>ZU4EG</th>
<th>ZU5EG</th>
<th>ZU6EG</th>
<th>ZU7EG</th>
<th>ZU9EG</th>
<th>ZU11EG</th>
<th>ZU15EG</th>
<th>ZU17EG</th>
<th>ZU19EG</th>
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<tbody>
<tr>
<td><strong>Application</strong></td>
<td>Processor Core</td>
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<tr>
<td><strong>Processor Unit</strong></td>
<td>Memory w/ECC</td>
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<td><strong>Real-Time</strong></td>
<td>Processor Core</td>
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<td><strong>Graphic &amp; Video</strong></td>
<td>Graphics Processing Unit</td>
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<td><strong>External Memory</strong></td>
<td>Dynamic Memory Interface</td>
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<td>Static Memory Interfaces</td>
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<td><strong>PS to PL Interface</strong></td>
<td>12 x 32/64/128b AXI Ports</td>
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<td>System Logic Cells (K)</td>
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<td>504</td>
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<td>CLB Flip-Flops (K)</td>
<td>94</td>
<td>141</td>
<td>176</td>
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<td>CLB LUTs (K)</td>
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<td>DSP Slices</td>
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<td>1,248</td>
<td>1,973</td>
<td>1,728</td>
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<td>Transceivers</td>
<td>GTH 16.3Gb/s Transceivers</td>
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<td>GTY 32.75Gb/s Transceivers</td>
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</table>
Test Setup – Requirements

- SEL monitoring on all 19 power domains

- SEU characterisation of
  - FPGA
    - Configuration RAM (CRAM)
    - Block RAM (BRAM) & Distributed RAM (DistRAM)
    - Flip-flops (FFs)

  - Processing system
    - Single thread benchmark execution on R5 processor core
      - Coremark and PI FFT benchmark
    - ECC enabled on all internal memories
Test Setup – Test Board Overview

- FPGA SW&LED
- USB UART
- DDR3 SODIM module
- SD Memory Card
- JTAG interface
- QSPI flash
- Boot mode selection SW
- Processor SW&LED
- Shunt resistors (current monitoring)
- Power supplies
- Tester interface
Test Setup – General Test Setup
Test Setup – Package Preparation

- **Flip-chip die**
  - Die directly interfaced on the PCB package
  - Radiation from the backside
  - Die thinned to 73 µm
  - *Xenon* penetration range 73.1 µm

### Available particles and penetration range at UCL HIF

<table>
<thead>
<tr>
<th>Ion, Mass</th>
<th>DUT energy [MeV]</th>
<th>Range [µm Si]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{13}$C $^{4+}$</td>
<td>131</td>
<td>269.3</td>
</tr>
<tr>
<td>$^{22}$Ne $^{7+}$</td>
<td>238</td>
<td>202.0</td>
</tr>
<tr>
<td>$^{27}$Al $^{8+}$</td>
<td>250</td>
<td>131.2</td>
</tr>
<tr>
<td>$^{40}$Ar $^{12+}$</td>
<td>379</td>
<td>120.5</td>
</tr>
<tr>
<td>$^{53}$Cr $^{16+}$</td>
<td>513</td>
<td>107.6</td>
</tr>
<tr>
<td>$^{58}$Ni $^{18+}$</td>
<td>582</td>
<td>100.5</td>
</tr>
<tr>
<td>$^{84}$Kr $^{25+}$</td>
<td>769</td>
<td>94.2</td>
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<tr>
<td>$^{124}$Xe $^{35+}$</td>
<td>995</td>
<td>73.1</td>
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</table>
Test Setup – FPGA Test Methodologies

- **CRAM** scrubbing with SEM-IP
  - Reflects real usage of FPGA in space application
  - Avoid accumulation of CRAM upsets
  - Live CRAM error reporting during the test (UART output of SEM-IP sent via tester)

- **BRAM** and **DistRAM**
  - Build as two memory arrays
  - Accessible via external pins (address + data)
  - Tester generates WRITE/READ patterns (similar to a SRAM component test)

- Two **flip-flop chain** configurations
  - Standard FF chain
  - XTMR chain

<table>
<thead>
<tr>
<th>Instance</th>
<th>Standard FF Chain</th>
<th>+ TMR Chain</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRAM</td>
<td>28 Mb</td>
<td>28 Mb</td>
</tr>
<tr>
<td>BRAM</td>
<td>7.8 Mb</td>
<td>7.8 Mb</td>
</tr>
<tr>
<td>DistRAM</td>
<td>0.88 Mb</td>
<td>0.88 Mb</td>
</tr>
<tr>
<td>FF</td>
<td>96 000</td>
<td>48 000</td>
</tr>
<tr>
<td>TMR</td>
<td>0</td>
<td>16 000</td>
</tr>
</tbody>
</table>

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<td>48 000</td>
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<tr>
<td>TMR</td>
<td>0</td>
<td>16 000</td>
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</tbody>
</table>
Heavy Ions – Facilities

- **UCL HIF**
  - Typical fluence per condition:
    - Carbon (LET = 1.3 MeV/mg/cm²): 5e6 hi/cm²
    - Xenon (LET = 62.5 MeV/mg/cm²): 1.5e5 hi/cm²

- **CERN H8 ultra-high energy Xe beam**
  - Energy = 30 GeV/amu ➔ Ion range ≈ 6 cm
  - LET = 3.7 MeV/mg/cm²
  - Typical fluence per condition: 1e5 hi/cm²

- **Facility comparison CERN H8 vs UCL HIF**

<table>
<thead>
<tr>
<th></th>
<th>CERN H8</th>
<th>UCL HIF</th>
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<tbody>
<tr>
<td><strong>Pros</strong></td>
<td>• Test in air</td>
<td>• Relatively constant flux</td>
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<tr>
<td></td>
<td>• No need to de-lid / thin devices</td>
<td>• Moving stage in the vacuum chamber</td>
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<td></td>
<td>• Up to 90° tilt angles</td>
<td>• Accurate alignment (LASER)</td>
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<tr>
<td><strong>Cons</strong></td>
<td>• Beam delivered as spills</td>
<td>• Vacuum test complexities</td>
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<tr>
<td></td>
<td>- Deadtime computation complexities</td>
<td>• Device preparation difficulties</td>
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<tr>
<td></td>
<td>- Less test efficiency</td>
<td>• Effective LET depends on device thickness</td>
</tr>
<tr>
<td></td>
<td>• Lack of information about flux vs time</td>
<td>• Limited cable to control room</td>
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<tr>
<td></td>
<td>• DUT alignment accuracy</td>
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</tr>
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<td></td>
<td>• Limited cable to control room</td>
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</tbody>
</table>
Heavy Ions – SEL Test Results

- **VCC_AUX / VCC_PSAUX**

  - [Graph for VCC_AUX / VCC_PSAUX]

- **VCC_AUXIO**

  - [Graph for VCC_AUXIO]
Heavy Ions – SEU Test Results (1)

- Configuration RAM

- Xilinx scaling family trends

Based on [7]
Heavy Ions – SEU Test Results (2)

- BRAM and Distributed RAM

- User Flip-Flops
Heavy Ions – HD IO Hard Failure

- Observed permanent stuck at failure of HD IOs (operation at 3.3V) input
  - Output driver is still operating correctly
  - Input is stuck at 1 or 0
  - Occurred during high LET tests (Xe and Ni)
  - Does not seem to be contention with tester
    - 100 Ohm resistor connected between
High-Energy Electron – Facility

- **VESPER**
  - Energy Range: 60 – 200 MeV
  - Flux: $7 \times 10^6 – 1 \times 10^8$ e-/cm$^2$/s
  - Beam delivered as pulses, with 0.8-10 Hz frequency
  - Beam size: 2 cm x 2 cm

- **SEE mechanisms**
  - Indirect ionization
  - Direct ionization is negligible
    $(LET \approx 1 \times 10^{-3}$ MeV/cm$^2$/mg)
HE Electron – SEL Test Results

- No SEL events observed on any power domain

![Graph showing SEL XS UL (cm²) vs. Electron Energy (MeV)]
HE Electron – SEU Test Results

- Configuration RAM

- BRAM and Distributed RAM
Radiation test results for the Xilinx Ultrascale+ ZU3EG MP-SoC FPGA

- Implemented test setup
- Overview of used test facilities
- SEE sensitivity
  - Standard and ultra-high energy heavy-ion
  - High-energy electron

Further tests and analysis

- Low Energy Protons (RADEF)
- High Energy Protons (PSI)

Deeper analysis of the Processing System
Thank You!

Questions?

Thomas Lange thomas.lange@iroctech.com
Maximilien Glorieux maximilien.glorieux@iroctech.com
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[6] Xilinx TMRTool Industry’s First Triple Modular Redundancy Development Tool for Re-Configurable FPGAs