Single Event Characterization of a Xilinx UltraScale+ MP-SoC FPGA

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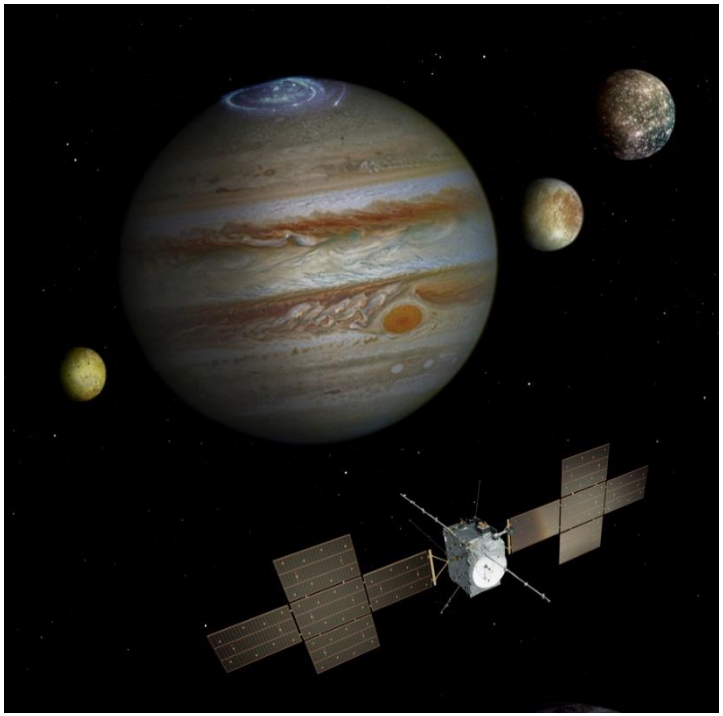
Outline

- ❑ Motivation
- ❑ Test Setup
- ❑ Facilities
- ❑ Test Results
- ❑ Conclusion and Future Work

Motivation

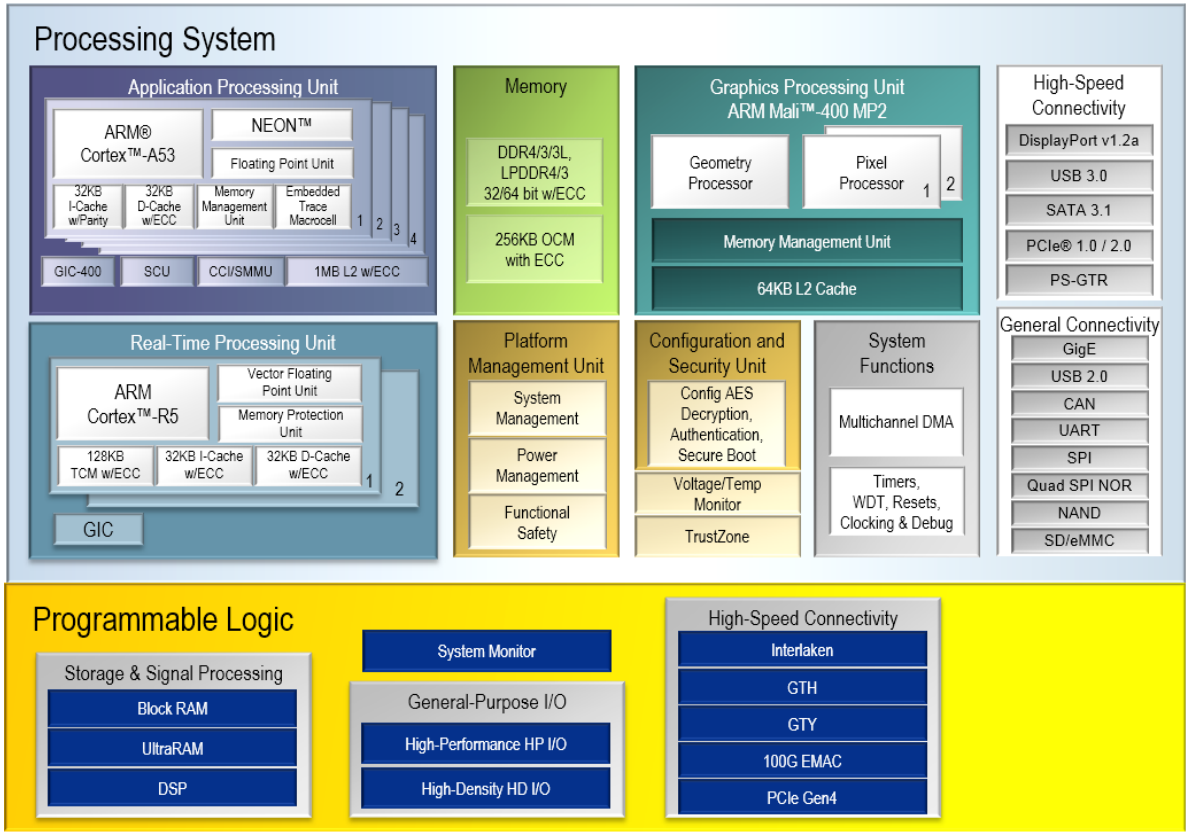
- ESA project to study radiation sensitivity of components operating in JUICE environment
  - 3 classes of devices tested
    - Commercial SRAMs
    - **SRAM-Based FPGA**
    - CPU/SoC
  - All devices tested under
    - ✓ Heavy Ions (UCL, CERN H8)
    - ✓ High Energy Electrons (VESPER)
    - ✗ High Energy Protons (PSI in May 2018)
    - ✓ Low Energy Protons (RADEF)



[1]

Motivation – XCZU3EG Overview (1)

- Latest generation Xilinx MP-SoC
  - Ultrascale architecture FPGA
  - ARM based processing system (4x A53 + 2x R5)
  - Manufactured in TSMC FinFET 16nm Technology



[2]

Motivation – XCZU3EG Overview (2)

❑ Characteristics of Zynq Ultrascale+ EG devices

		Device Name[1]	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB										
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core										
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz										
		Memory	L2 Cache 64KB										
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC										
		Static Memory Interfaces	NAND, 2x Quad-SPI										
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet										
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO										
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains										
		Security	RSA, AES, and SHA										
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor										
PS to PL Interface			12 x 32/64/128b AXI Ports										
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	47	71	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express® Gen 3x16 / Gen4x8	-	-	2	2	-	2	-	4	-	4	5
		150G Interlaken	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[2]	-1 -2 -2L		-1 -2 -2L -3					-1 -2 -2L -3			
		Industrial	-1 -1L -2										

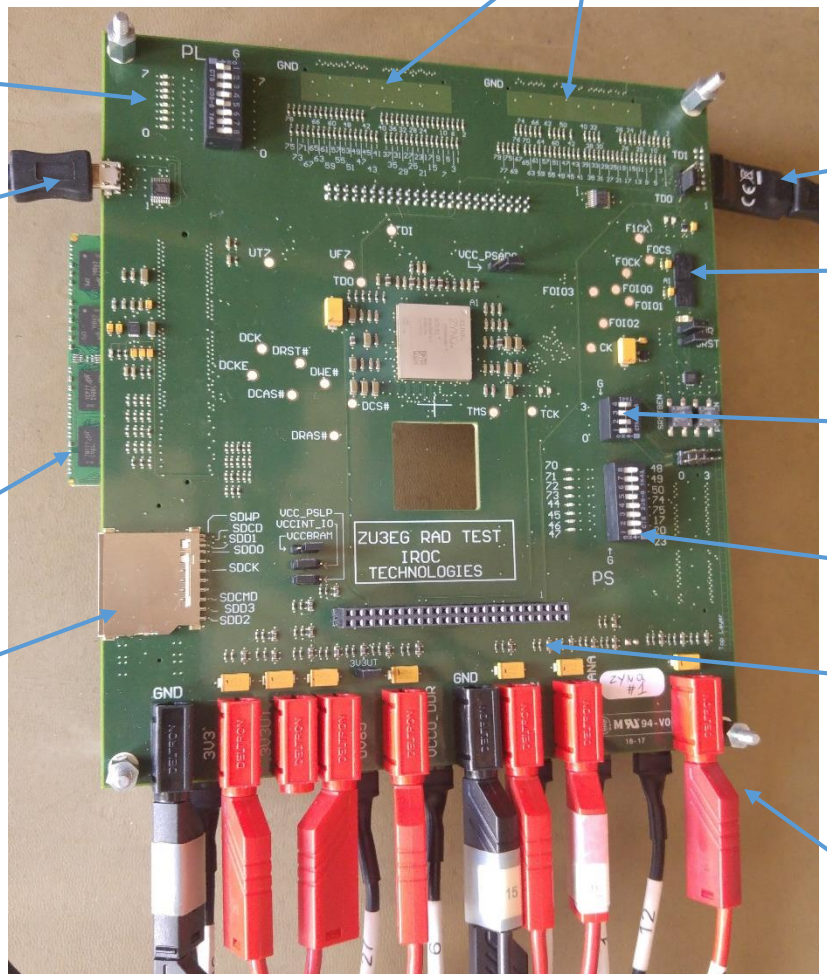
[3]

Test Setup – Requirements

- SEL monitoring on all 19 power domains

- SEU characterisation of
  - FPGA
    - Configuration RAM (CRAM)
    - Block RAM (BRAM) & Distributed RAM (DistRAM)
    - Flip-flops (FFs)
  - Processing system
    - Single thread benchmark execution on R5 processor core
      - Coremark and PI FFT benchmark
    - ECC enabled on all internal memories

Test Setup – Test Board Overview



Tester interface

FPGA SW&LED

USB UART

DDR3 SODIM module

SD Memory Card

JTAG interface

QSPI flash

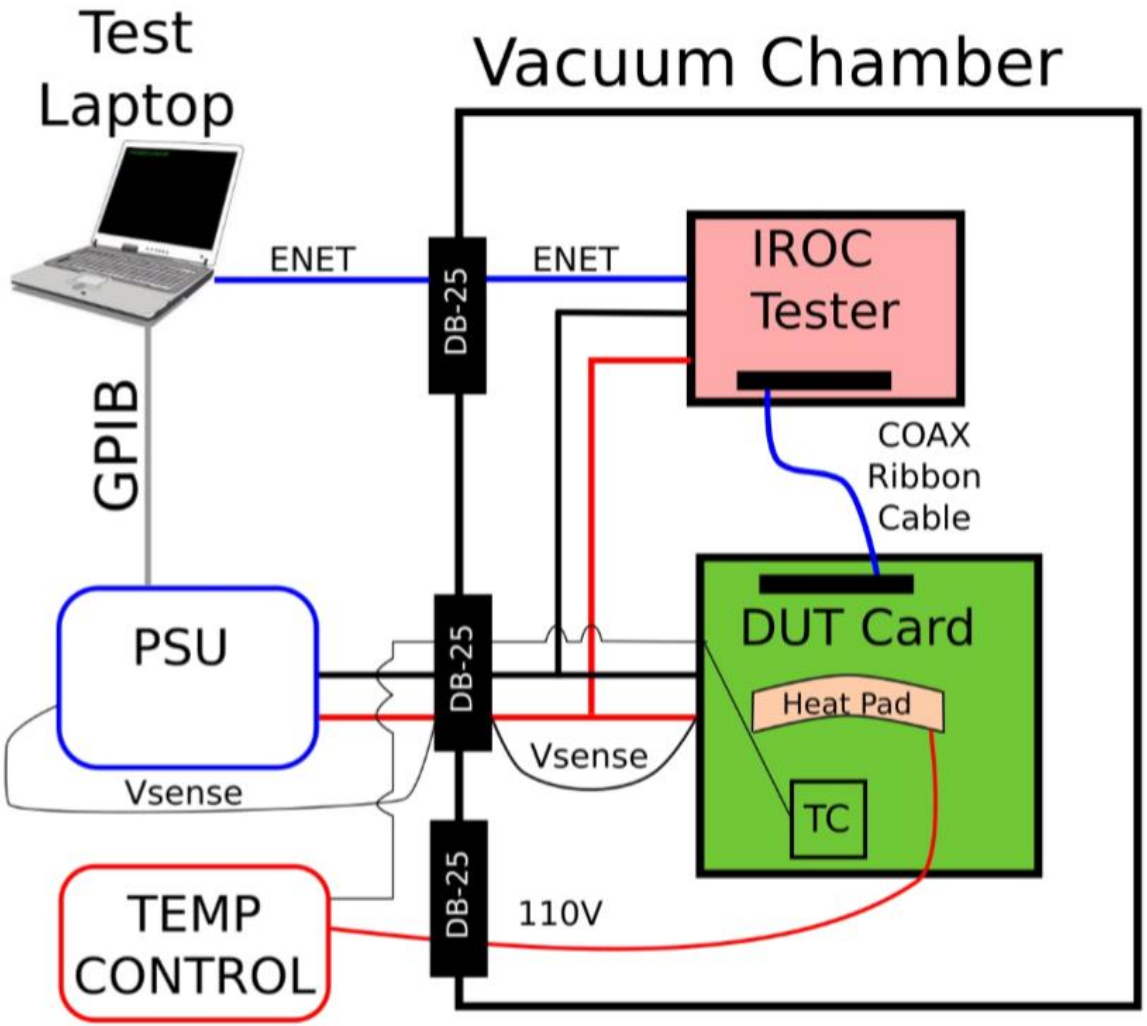
Boot mode selection SW

Processor SW&LED

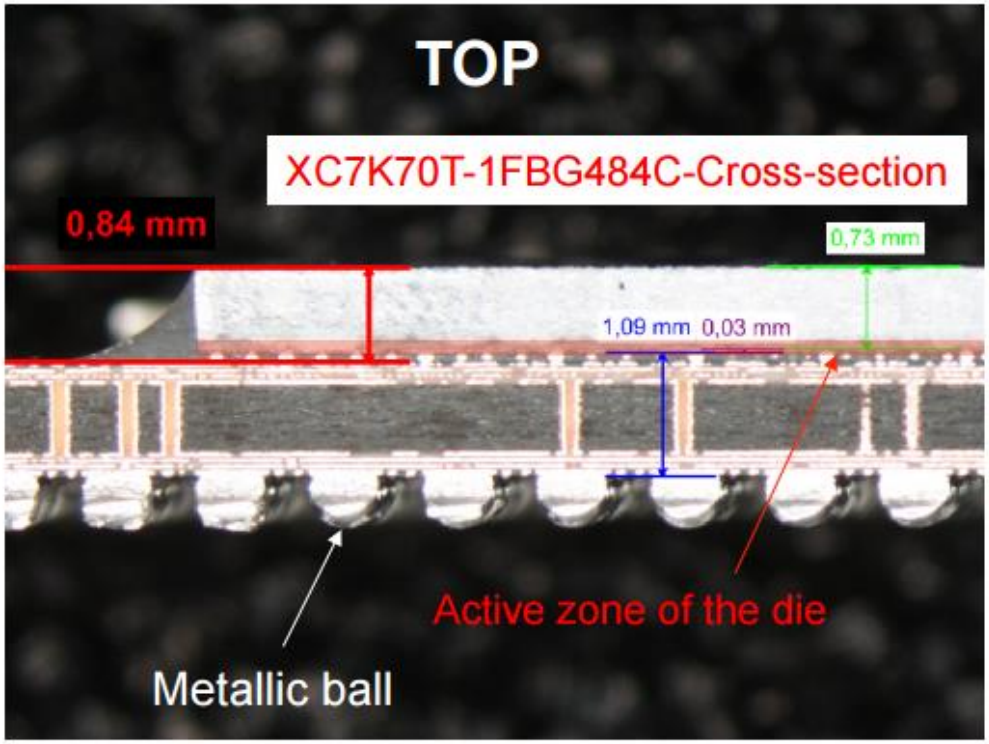
Shunt resistors (current monitoring)

Power supplies

Test Setup – General Test Setup



Test Setup – Package Preparation



[4]

Available particles and penetration range at UCL HIF

Ion	DUT energy [MeV]	Range [µm Si]
$^{13}C^{4+}$	131	269.3
$^{22}Ne^{7+}$	238	202.0
$^{27}Al^{8+}$	250	131.2
$^{40}Ar^{12+}$	379	120.5
$^{53}Cr^{16+}$	513	107.6
$^{58}Ni^{18+}$	582	100.5
$^{84}Kr^{25+}$	769	94.2
$^{124}Xe^{35+}$	995	73.1

[5]

- Flip-chip die
  - Die directly interfaced on the PCB package
  - Radiation from the backside
  - Die thinned to 73 µm
    - Xenon penetration range 73.1 µm

Test Setup – FPGA Test Methodologies

- CRAM scrubbing with SEM-IP
  - Reflects real usage of FPGA in space application
  - Avoid accumulation of CRAM upsets
  - Live CRAM error reporting during the test (UART output of SEM-IP sent via tester)

- BRAM and DistRAM
  - Build as two memory arrays
  - Accessible via external pins (address + data)
  - Tester generates WRITE/READ patterns (similar to a SRAM component test)

- Two flip-flop chain configurations
  - Standard FF chain
  - XTMR chain

Instance	Standard FF Chain	+ TMR Chain
CRAM	28 Mb	28 Mb
BRAM	7.8 Mb	7.8 Mb
DistRAM	0.88 Mb	0.88 Mb
FF	96 000	48 000
TMR	0	16 000

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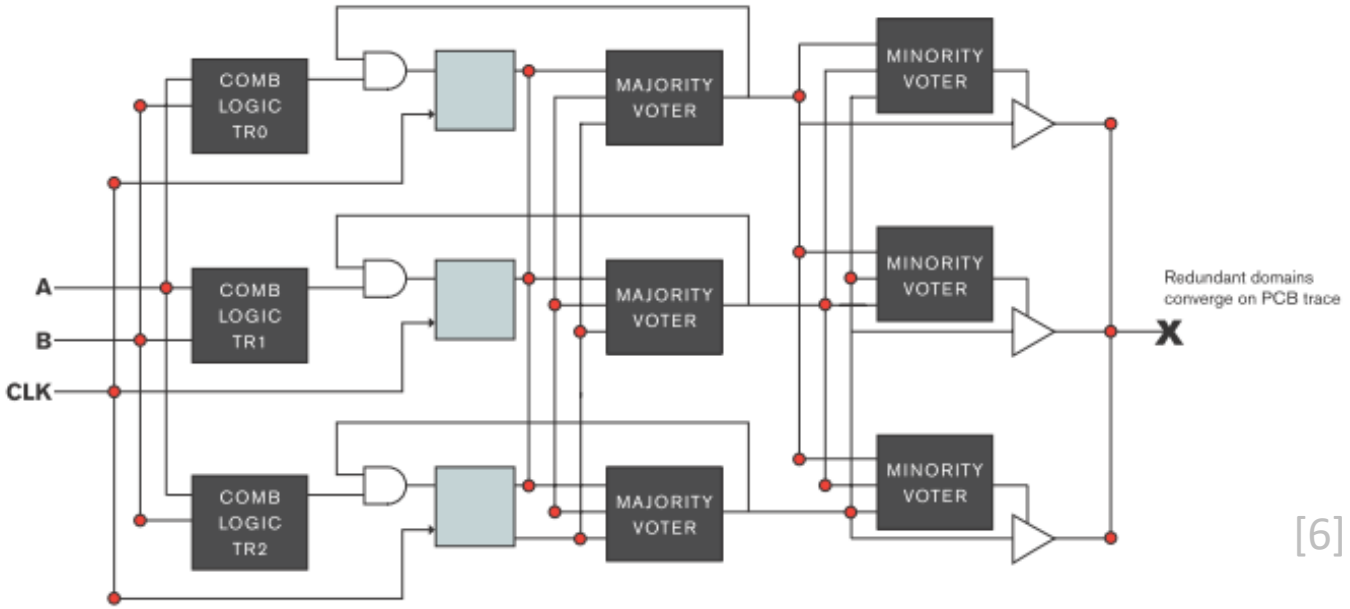

[6]

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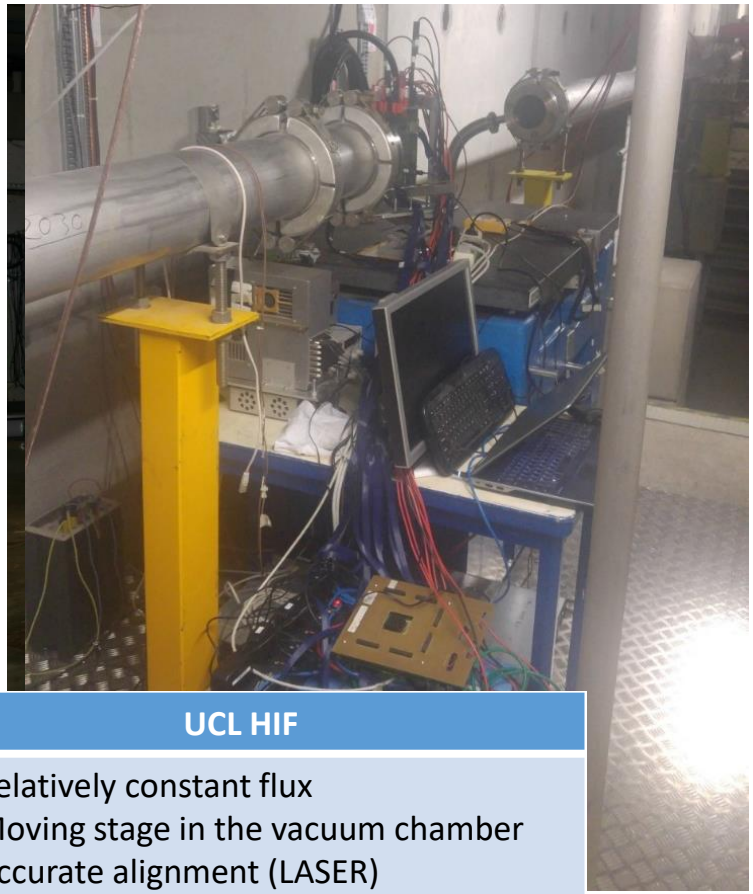
TMR	0	16 000

Heavy Ions – Facilities

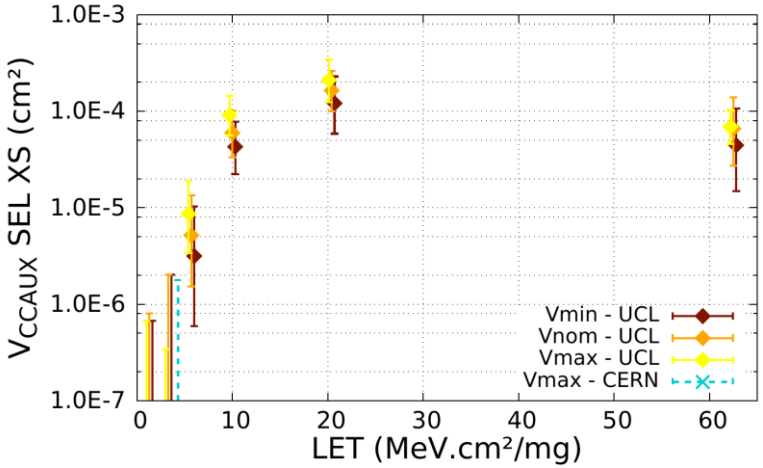
- UCL HIF
  - typical fluence per condition:
    - Carbon (LET = 1.3 MeV/mg/cm²): 5e6 hi/cm²
    - Xenon (LET = 62.5 MeV/mg/cm²): 1.5e5 hi/cm²
- CERN H8 ultra-high energy Xe beam
  - Energy = 30 GeV/amu ➥ Ion range ≈ 6 cm
  - LET = 3.7 MeV/mg/cm²
  - typical fluence per condition: 1e5 hi/cm²
- Facility comparison CERN H8 vs UCL HIF

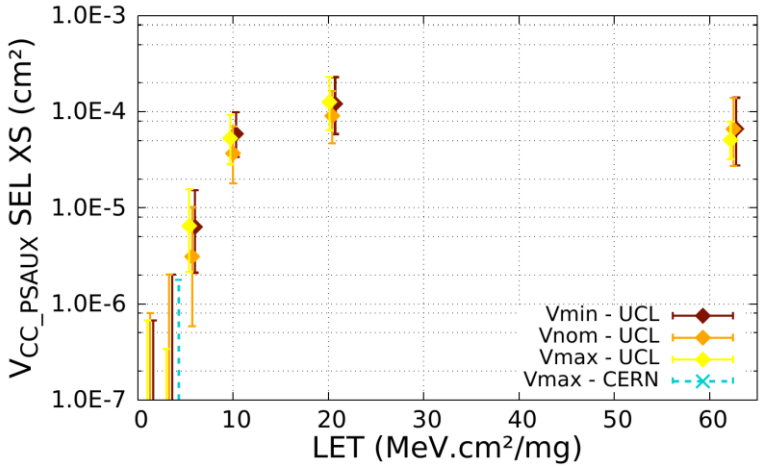


	CERN H8	UCL HIF
Pros	• Test in air • No need to de-lid / thin devices • Up to 90° tilt angles	• Relatively constant flux • Moving stage in the vacuum chamber • Accurate alignment (LASER)
Cons	• Beam delivered as spills - Deadtime computation complexities - Less test efficiency • Lack of information about flux vs time • DUT alignment accuracy • Limited cable to control room	• Vacuum test complexities • Device preparation difficulties • Effective LET depends on device thickness

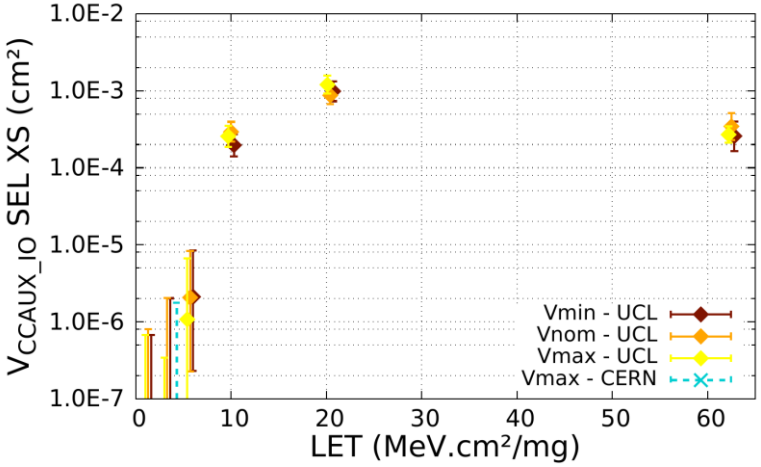
Heavy Ions – SEL Test Results

- VCC_AUX / VCC_PSAUX



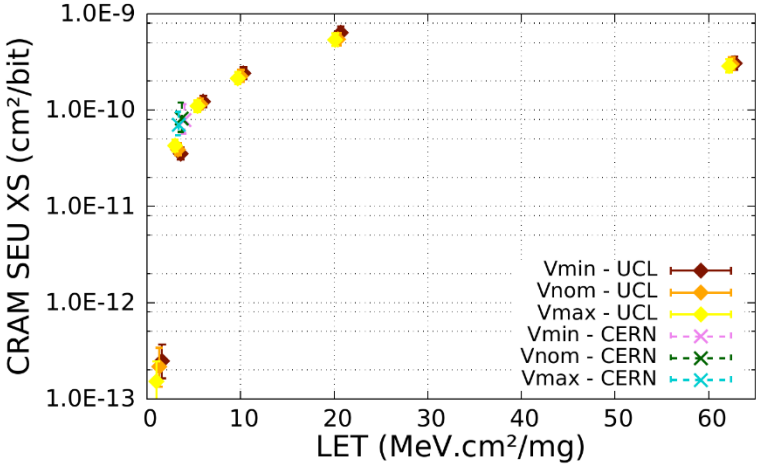


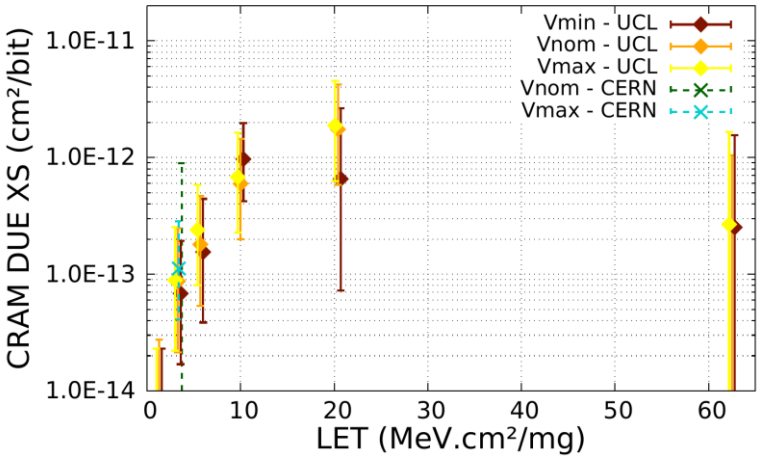
- VCC_AUXIO



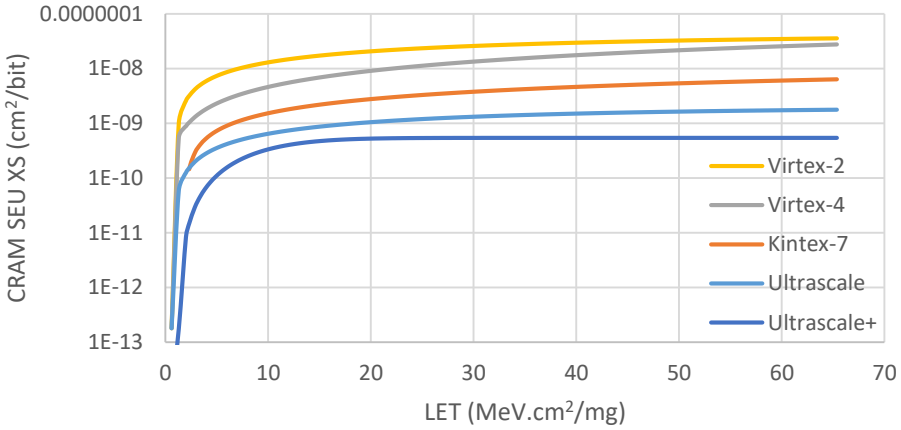
Heavy Ions – SEU Test Results (1)

❑ Configuration RAM





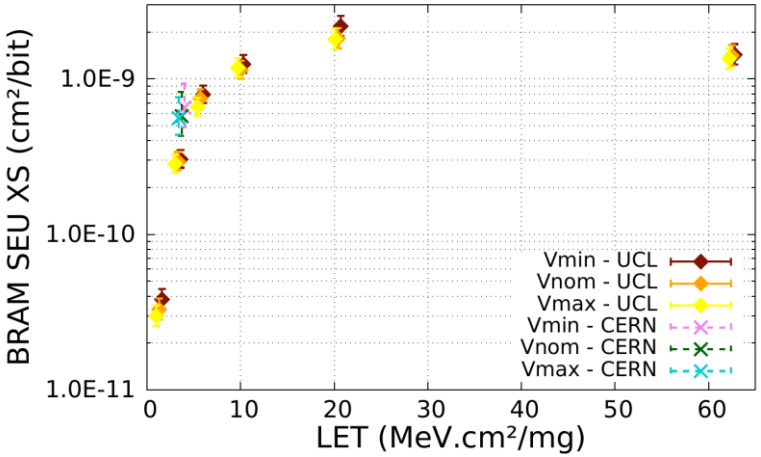
❑ Xilinx scaling family trends

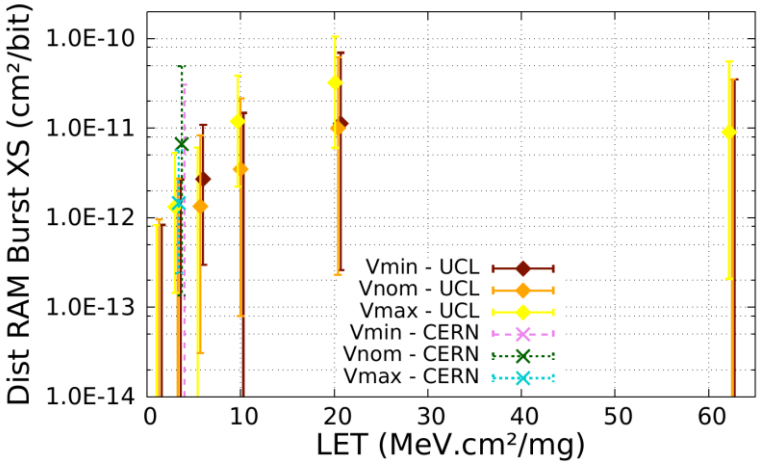


based on [7]

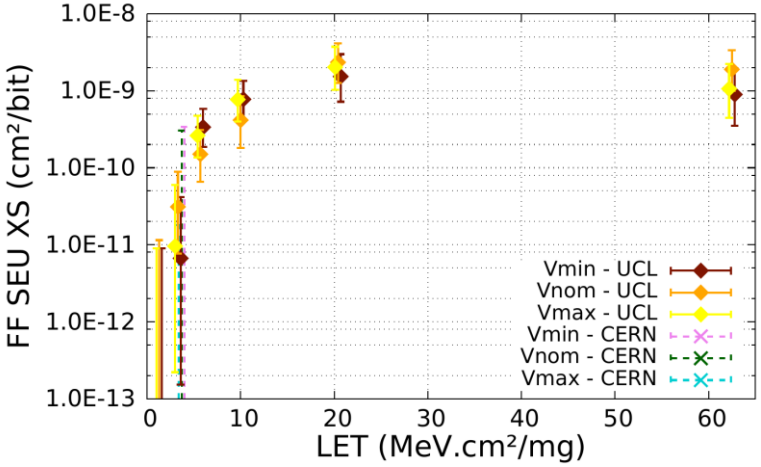
Heavy Ions – SEU Test Results (2)

❑ BRAM and Distributed RAM





❑ User Flip-Flops



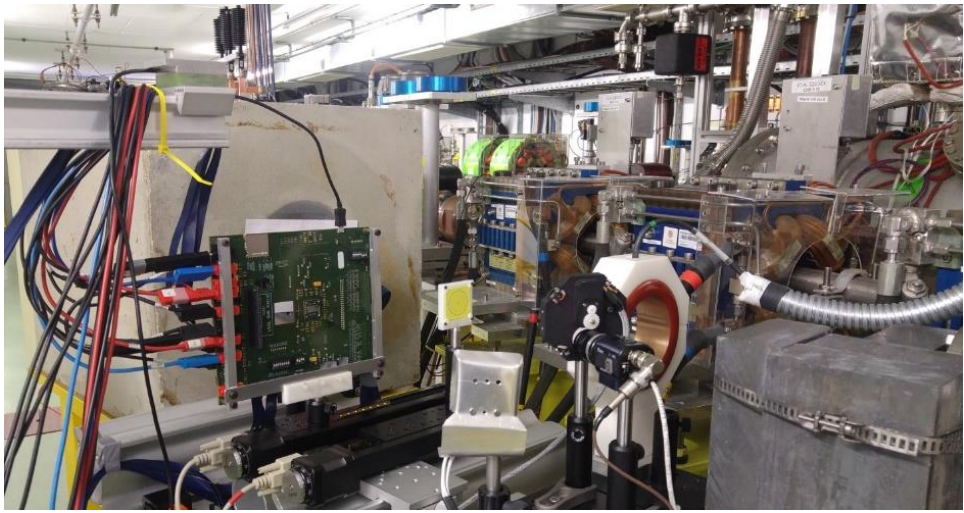
Heavy Ions – HD IO Hard Failure

- Observed permanent stuck at failure of HD IOs (operation at 3.3V) input
  - Output driver is still operating correctly
  - Input is stuck at 1 or 0
  - Occurred during high LET tests (Xe and Ni)
  - Does not seem to be contention with tester
    - 100 Ohm resistor connected between

High-Energy Electron – Facility

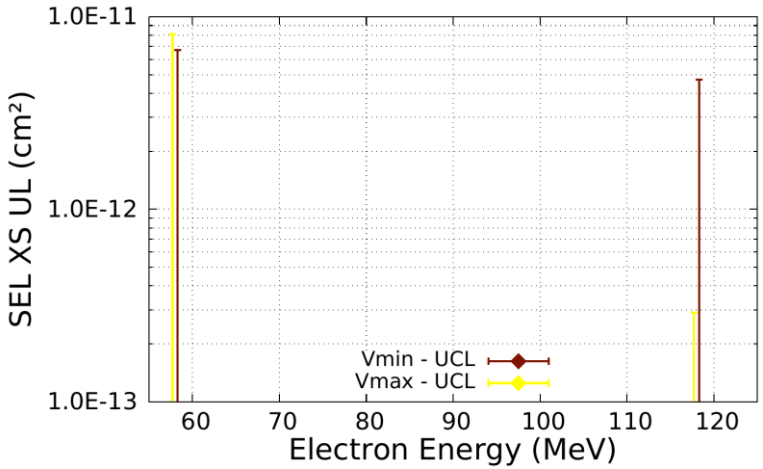
- VESPER
  - Energy Range: 60 – 200 MeV
  - Flux: $7x10^6$ – $1x10^8$ e-/cm²/s
  - Beam delivered as pulses, with 0.8-10 Hz frequency
  - Beam size: 2 cm x 2 cm

- SEE mechanisms
  - Indirect ionization
  - Direct ionization is negligible (LET ≈ $1x10^{-3}$ MeV/cm²/mg)



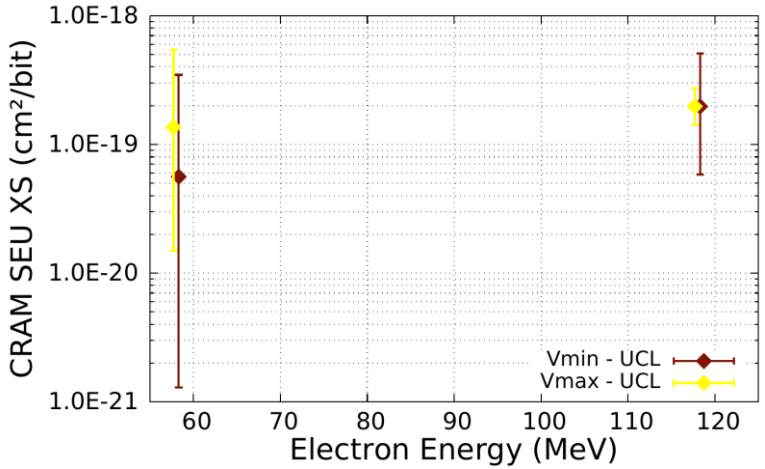
HE Electron – SEL Test Results

- No SEL events observed on any power domain

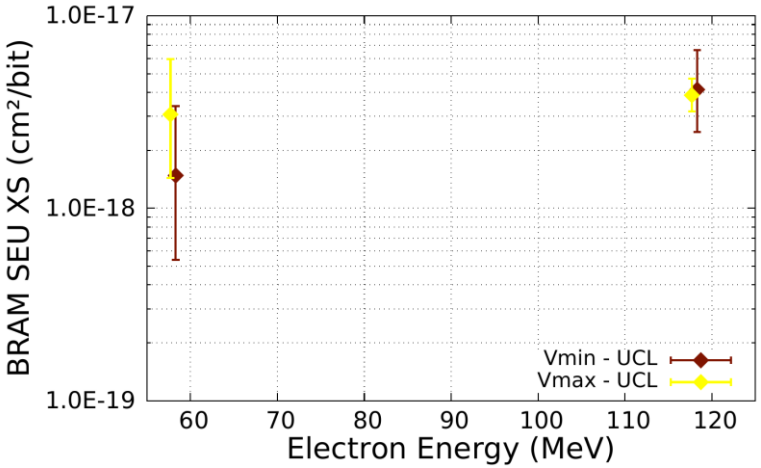


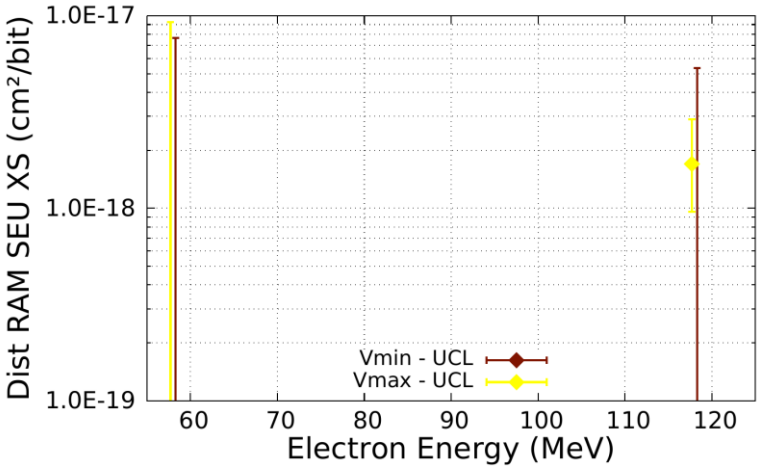
HE Electron – SEU Test Results

❑ Configuration RAM



❑ BRAM and Distributed RAM





Conclusion and Future Work

- Radiation test results for the Xilinx Ultrascale+ ZU3EG MP-SoC FPGA
  - Implemented test setup
  - Overview of used test facilities
  - SEE sensitivity
    - Standard and ultra-high energy heavy-ion
    - High-energy electron
- Further tests and analysis
  - Low Energy Protons (RADEF)
  - High Energy Protons (PSI)
- Deeper analysis of the Processing System

Thank You!

Questions?

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