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Single Event Characterization of a Xilinx UltraScale+ MP-SoC FPGA

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Due to the technology scaling, more and more complex applications can be implemented on configurable devices, such as the new Xilinx FPGAs and MP-SoCs. In addition, devices manufactured in new process technologies, e.g. FD-SOI and FinFet, show a much lower sensitivity to Single Event Effects than previous generation bulk processes. These aspects and their affordable cost, especially in comparison to Application Specific Integrated Circuits (ASICs), make configurable devices more attractive for space applications.

The focus of our study is to evaluate the radiation sensitivity of a Xilinx Ultrascale+ ZU3EG MP-SoC FPGA. The device embeds 4 ARM A53 APU, 2 ARM R5 RPU cores and an FPGA based on the Ultrascale architecture. In order to measure the Single Event Effect (SEE) sensitivity of the device, it was tested under standard heavy-ion (at UCL), ultra-high energy heavy-ion (at the H8 beam line, extracted from SPS, CERN) and high-energy electrons irradiation (at VESPER, CERN) and will be tested further under high energy protons (at PSI) and low energy protons irradiation (at RADEF). Therefore, a custom test board has been designed which allows the measurement of the SEE cross-sections. Single Event Latch-UPs (SELs) are detected by the independent current monitoring on all power domains of the device under test and the observation of sudden current increases (typically signature for SELs). Further, an FPGA test vehicle has been developed which measures the SEU cross-sections of several FPGA elements, as well as the functional failure rate of the embedded R5 processor. The Configuration RAM is monitored with the help of the Xilinx SEM-IP. The Block RAM and Distributed RAM are tested by using an external tester and standard memory test algorithms. Two different shift register chains are used to evaluate the FPGA Flip-Flops SEU rates in normal and TMR configuration.

In this presentation, we will describe the implemented test setup, give an overview of the used test facilities and show SEE sensitivity measured during the campaigns.

Summary

We present the radiation test results for a Xilinx Ultrascale+ ZE3EG MP-SoC FPGA, tested under standard and ultra-high energy heavy-ion irradiation, as well as high energy electron irradiation.

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