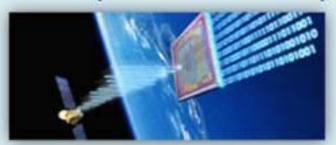
First Design-In Experiences of Xilinx's, 20 nm, Kintex UltraScale KU060 for Space Applications and 16 nm UltraScale+ RFSoC for Ground Segment

Dr. Rajan Bedi

Spacechips
The Global Space-Electronics Company



On-Board Processing Products, Design Consultancy in Space Electronics, Technical Marketing, Training and Business-Intelligence Services

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Space-Grade/COTS FPGAs

	Xilinx	NanoXplore	NanoXplore	Xilinx	Microsemi	Microsemi
	V5QV	NG-ULTRA	NG-LARGE	KU060	RTG4	IGLOO2/SF2
Core Voltage (V)	1.0	TBD (< 1V)	1.2	0.9	1.2	1.2
Speed (MHz)	450	TBD	TBD	1000	300	300
Memory (Mb)	10.9	32	9.8	38	5	0.7 to 5
No. of LUTs (k)	87.9	TBD	137	331	151	6 to 146
No. of Flip Flops (k)	87.9	TBD	129	663	151	6 to 146
Transceivers	18 at 3.125 Gbps	? at 12.5 Gbps	24 at 6.25 Gbps	32 at 12.5 Gbps	24 at 3.125 Gbps	0 to 16 at 5 Gbps
User I/O	836	TBD	TBD	624	720	209 to 574

20 nm Fabrication Technology Advantages

- 20 nm delivers higher bandwidth, more logic resources at lower power.
- Power Consumption Advantages
 - Lower power operation due to a core voltage of 0.9 V and smaller capacitive loads:
 - Pdynamic α CV² 25% lower than equivalent 1.0/1.2 V FPGAs

$$P_{dynamic} = \begin{bmatrix} \frac{1}{2}CV^2 + Q_{ShortCircuit}V \end{bmatrix} f \cdot activity$$
 Capacitance charging Short circuit charge during switching Percent of circuit that switches each cycle

- Pstatic αV^3

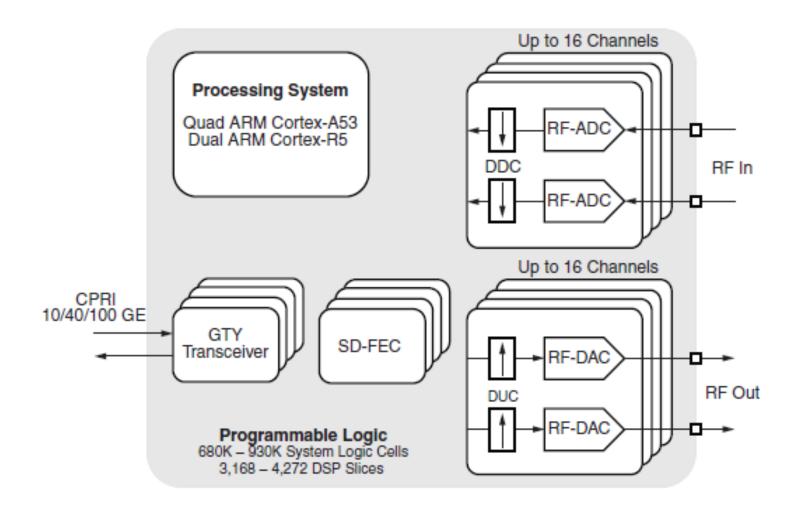
> 30% lower than equivalent 1.0/1.2 V FPGAs

Radiation Hardness

- Same silicon as commercial version
- Scaling benefits
- *SEL* (*Sandia*) = 79.2 *MeV-cm*²/*mg*
- TID = 100 Krad (Si)
- TMR FT MicroBlaze, 32-bit RISC CPU
- CRAM is interleaved, SEM IP for mitigation
- User triplication, EDAC and scrubbing

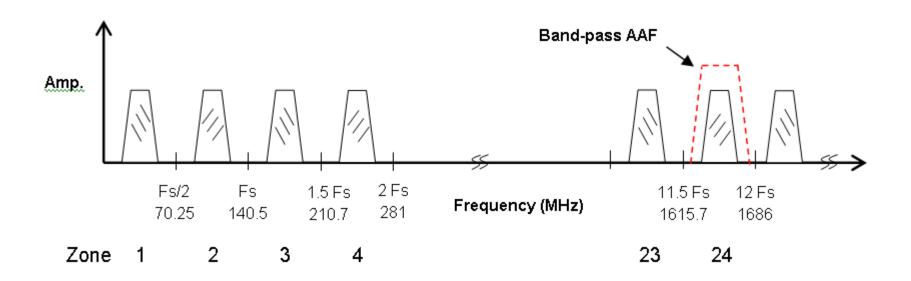


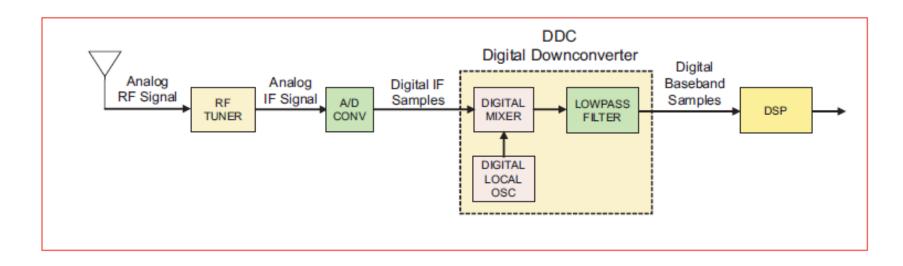
16 nm MPSoC

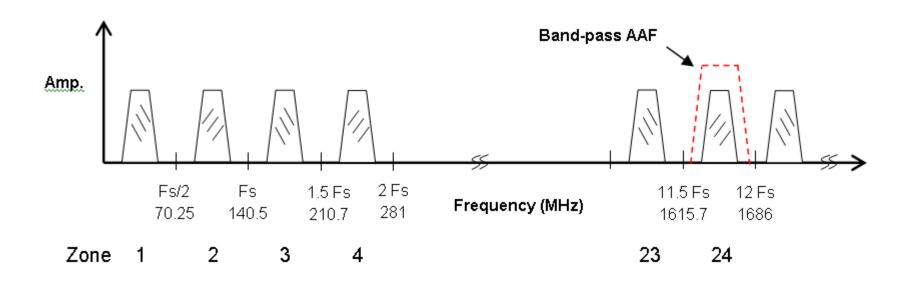


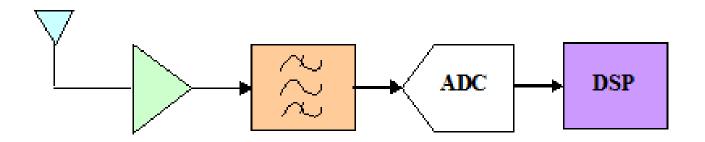
XCZU21DR XCZU25DR XCZU27DR XCZU28DR XCZU29DR 12-bit, 4GSPS RF-ADC w/ DDC 0 8 8 8 0 12-bit, 2GSPS RF-ADC w/ DDC 0 0 0 0 16 14-bit, 6.4GSPS RF-DAC w/ DUC 0 8 8 8 16 8 SD-FEC 0 O 8 O Quad-core ARM Cortex-A53 MPCore with CoreSight™; NEON and Single/Double Precision Floating Application Processing Unit Point: 32KB/32KB L1 Cache, 1MB L2 Cache Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Real-Time Processing Unit Cache, and TCM 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Embedded and External Memory Quad-SPI; NAND; eMMC 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; Watchdog Timers; Triple General Connectivity Timer Counters High-Speed Connectivity 4 PS-GTR; PCIe® Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII System Logic Cells 678,318 930,300 930,300 930,300 930,300 CLB Flip-Flops 850,560 620,176 850,560 850,560 850,560 310,088 425,280 CLB LUTs 425,280 425,280 425,280 Distributed RAM (Mb) 13.0 9.6 13.0 13.0 13.0 Block RAM Blocks 1,080 792 1.080 1.080 1.080 Block RAM (Mb) 38.0 27.8 38.0 38.0 38.0 UltraRAM Blocks 80 48 80 80 80 UltraRAM (Mb) 22.5 13.5 22.5 22.5 22.5 DSP Slices 4,272 3,145 4,272 4,272 4,272

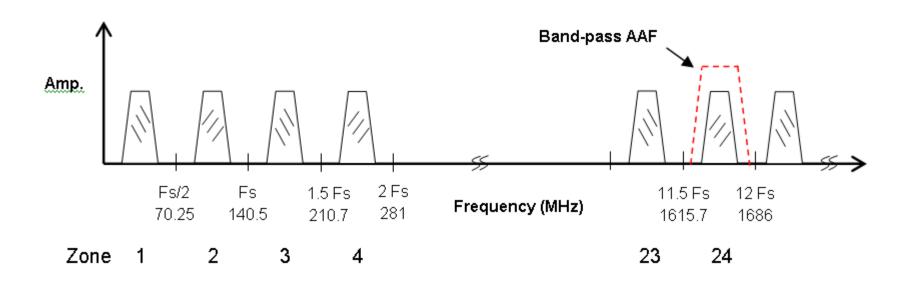
70% utilisation = 13W

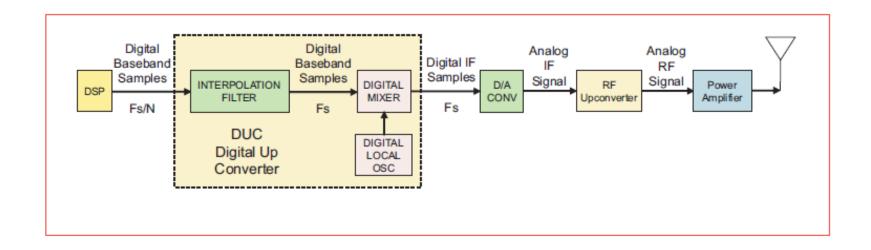


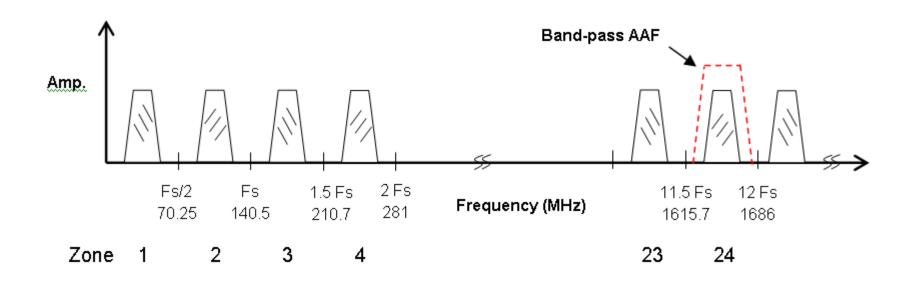


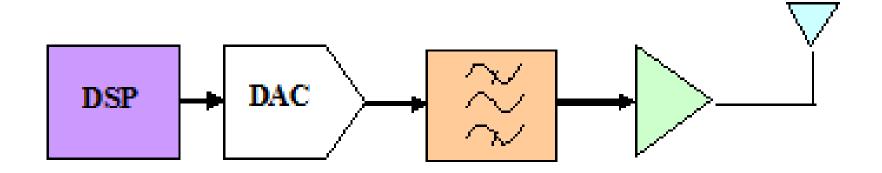


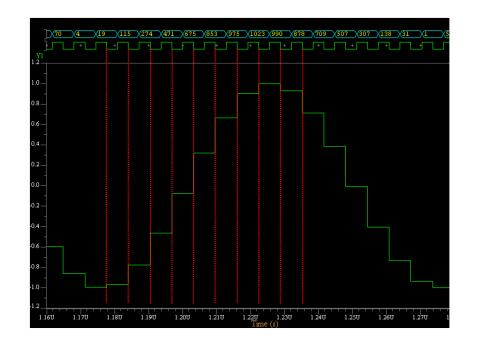


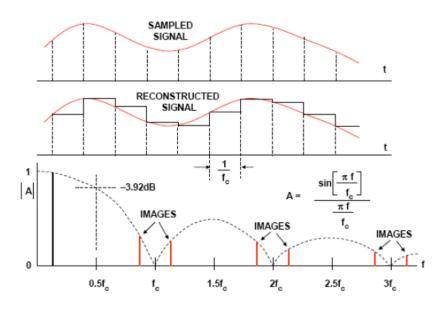




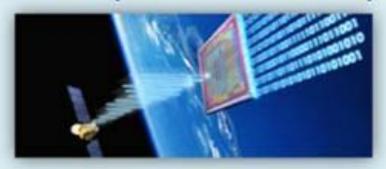








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