A Comparison of 65 nm Space-Grade and COTS FPGAs : RTG4 vs. V5QV vs. NG-MEDIUM vs. NG-LARGE vs. IGLOO2 vs. SmartFusion2

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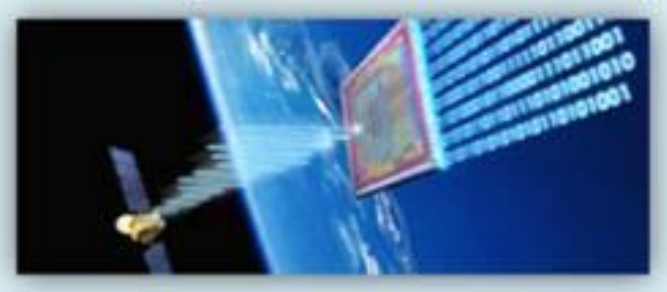

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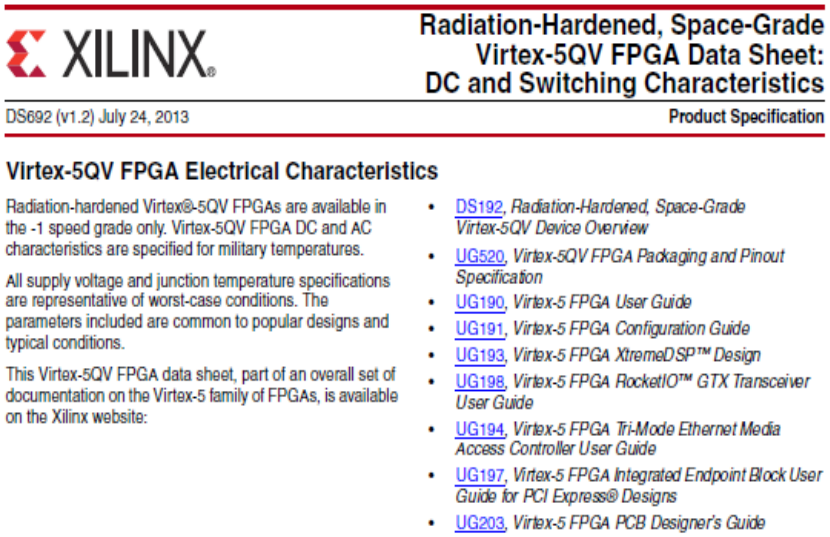
65 nm Space-Grade/COTS FPGAs

	Xilinx V5QV	NanoXplore NG-MEDIUM	NanoXplore NG-LARGE	Microsemi RTG4	Microsemi IGLOO2/SF2
Core Voltage (V)	1.0	1.2	1.2	1.2	1.2
Speed (MHz)	450	250	TBD	300	300
Memory (Mb)	10.9	2.8	9.8	5	0.7 to 5
No. of LUTs (k)	87.9	34.2	137	151	6 to 146
No. of Flip Flops (k)	87.9	32.2	129	151	6 to 146
Transceivers	18 at 3.125 Gbps	×	24 at 6.25 Gbps	24 at 3.125 Gbps	0 to 16 at 5 Gbps
User I/O	836	390/208	TBD	720	209 to 574

Xilinx Radiation-Hardened V5QV



XILINX

Radiation-Hardened, Space-Grade Virtex-5QV FPGA Data Sheet: DC and Switching Characteristics

DS692 (v1.2) July 24, 2013 — **Product Specification**

Virtex-5QV FPGA Electrical Characteristics

Radiation-hardened Virtex®-5QV FPGAs are available in the -1 speed grade only. Virtex-5QV FPGA DC and AC characteristics are specified for military temperatures.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical conditions.

This Virtex-5QV FPGA data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- DS192, *Radiation-Hardened, Space-Grade Virtex-5QV Device Overview*
- UG520, *Virtex-5QV FPGA Packaging and Pinout Specification*
- UG190, *Virtex-5 FPGA User Guide*
- UG191, *Virtex-5 FPGA Configuration Guide*
- UG193, *Virtex-5 FPGA XtremeDSP™ Design*
- UG198, *Virtex-5 FPGA RocketIO™ GTX Transceiver User Guide*
- UG194, *Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller User Guide*
- UG197, *Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs*
- UG203, *Virtex-5 FPGA PCB Designer's Guide*

RHBP

65 nm – TID = 1 MRad(Si)

Thin Epi for SEL immunity

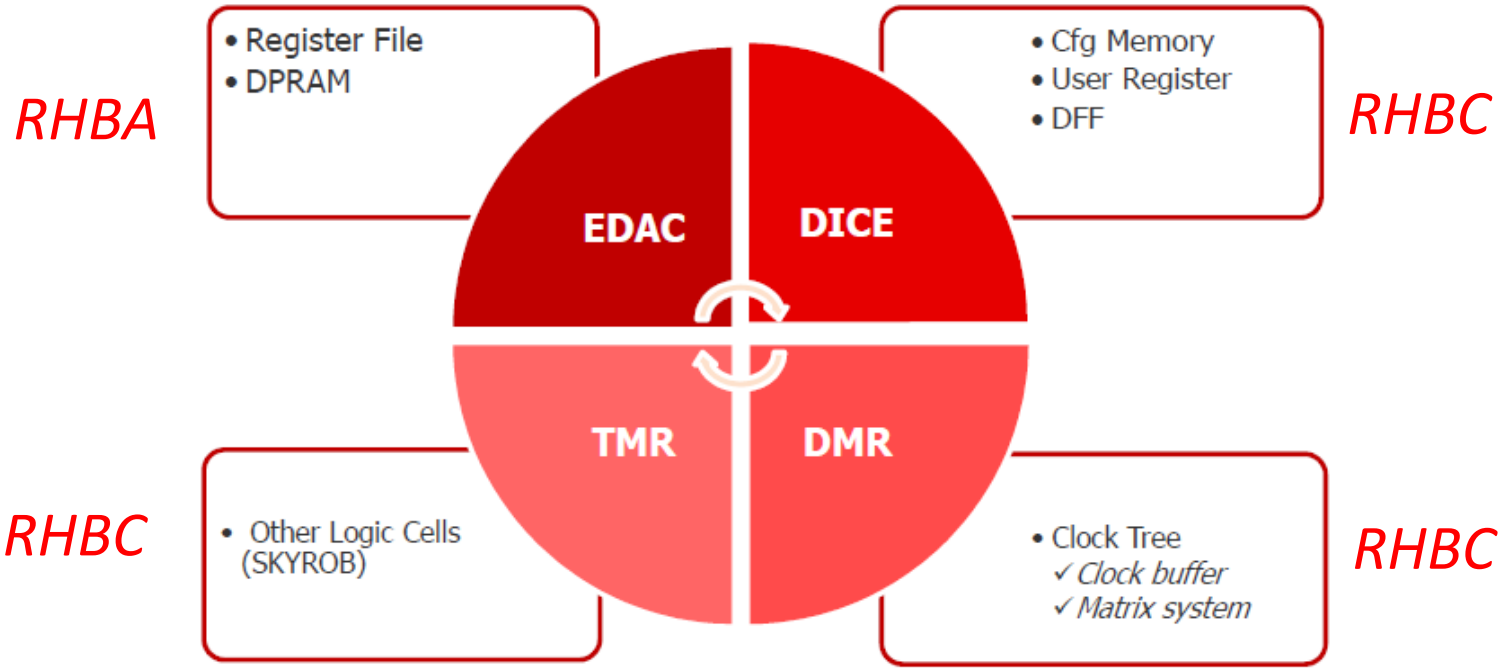
RHBL

Interleaved CRAM

- *RHBC & RHBA*
- *Hardened CRAM cells*
- *SEU & SET Hardened CRAM & JTAG Ctrl logic using TMR*
- *BRAM EDAC with autonomous write back*
- *SEU Hardened I/O Flip Flops*
- *SEU & SET Hardened DCI Control*
- *SEU & SET Hardened CLB Flip Flops.*
- *Hardened MGTs*

BRAVE, ITAR/EAR-Free Rad-Hard FPGAs

All logic of NX FPGAs is hardened by design (RHBD)
and simulated with TFIT software



On top of it,
Embedded Configuration Memory Integrity Check ("CMIC")

RHBD BRAVE

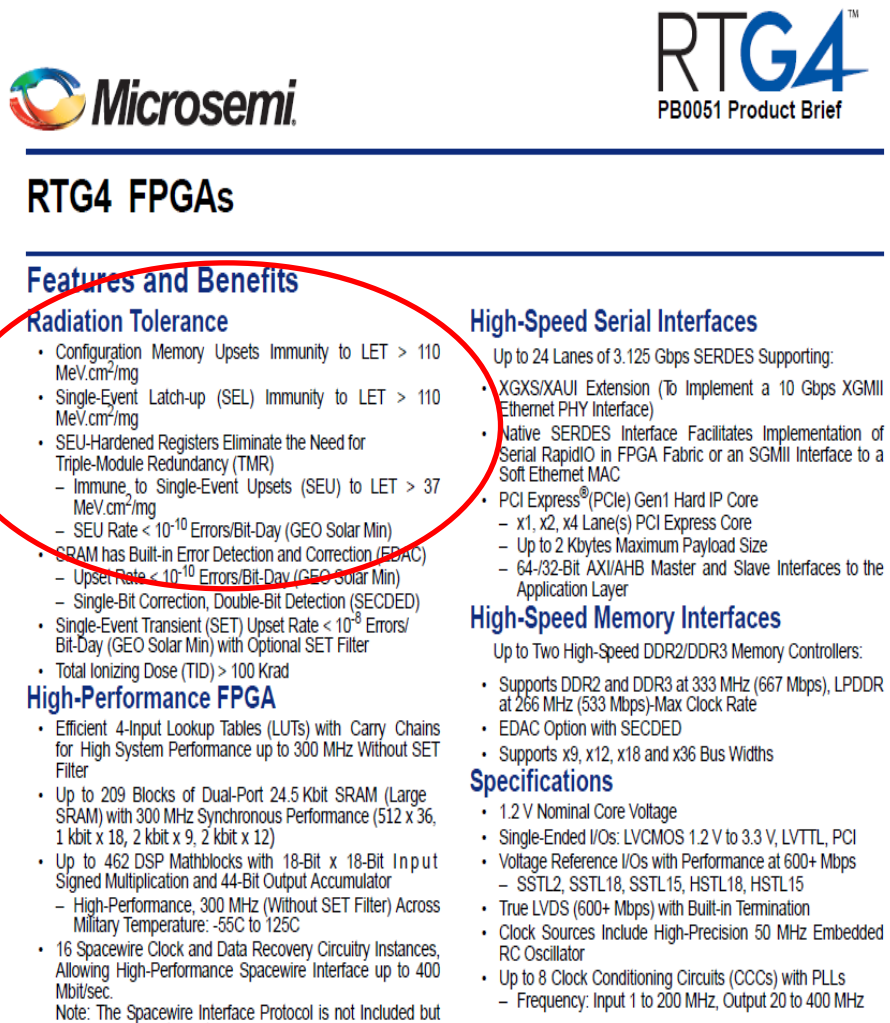
RHBP

- SEL immune
  - ST 65nm technology with PDK space design rules provides immunity at 60MeV/mg cm2, 125ºC, 1.32V
  - SEL TCAD simulations performed on IO buffers
- SEU / SET immune for LEO / GEO applications
  - Cell level hardening by design:
    - Implement a certain level redundancy
    - Optimize layout to reduce charge collection on critical nodes
    - Validate susceptibility with cross section simulation tools
  - Functional level hardening:
    - Use error detection and correction functions
    - Implement filters on critical signals (i.e. clock, reset)
  - System level:
    - Check bit stream integrity with signatures (FIC)
    - Check configuration integrity at run time (CMIC)

RHBL

RHBA

Flash RTG4



Microsemi

RTG4™

PB0051 Product Brief

RTG4 FPGAs

Features and Benefits

Radiation Tolerance

- Configuration Memory Upsets Immunity to LET > 110 MeV.cm^2/mg
- Single-Event Latch-up (SEL) Immunity to LET > 110 MeV.cm^2/mg
- SEU-Hardened Registers Eliminate the Need for Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to LET > 37 MeV.cm^2/mg
  - SEU Rate < 10^{-10} Errors/Bit-Day (GEO Solar Min)
- SRAM has Built-in Error Detection and Correction (EDAC)
  - Upset Rate < 10^{-10} Errors/Bit-Day (GEO Solar Min)
  - Single-Bit Correction, Double-Bit Detection (SECDED)
- Single-Event Transient (SET) Upset Rate < 10^{-8} Errors/Bit-Day (GEO Solar Min) with Optional SET Filter
- Total Ionizing Dose (TID) > 100 Krad

High-Performance FPGA

- Efficient 4-Input Lookup Tables (LUTs) with Carry Chains for High System Performance up to 300 MHz Without SET Filter
- Up to 209 Blocks of Dual-Port 24.5 Kbit SRAM (Large SRAM) with 300 MHz Synchronous Performance (512 x 36, 1 kbit x 18, 2 kbit x 9, 2 kbit x 12)
- Up to 462 DSP Mathblocks with 18-Bit x 18-Bit Input Signed Multiplication and 44-Bit Output Accumulator
  - High-Performance, 300 MHz (Without SET Filter) Across Military Temperature: -55C to 125C
- 16 Spacewire Clock and Data Recovery Circuitry Instances, Allowing High-Performance Spacewire Interface up to 400 Mbit/sec.
  Note: The Spacewire Interface Protocol is not Included but can be Implemented in the FPGA Fabric.

High-Speed Serial Interfaces

Up to 24 Lanes of 3.125 Gbps SERDES Supporting:

- XGXS/XAUI Extension (To Implement a 10 Gbps XGMII Ethernet PHY Interface)
- Native SERDES Interface Facilitates Implementation of Serial RapidIO in FPGA Fabric or an SGMII Interface to a Soft Ethernet MAC
- PCI Express® (PCIe) Gen1 Hard IP Core
  - x1, x2, x4 Lane(s) PCI Express Core
  - Up to 2 Kbytes Maximum Payload Size
  - 64-/32-Bit AXI/AHB Master and Slave Interfaces to the Application Layer

High-Speed Memory Interfaces

Up to Two High-Speed DDR2/DDR3 Memory Controllers:

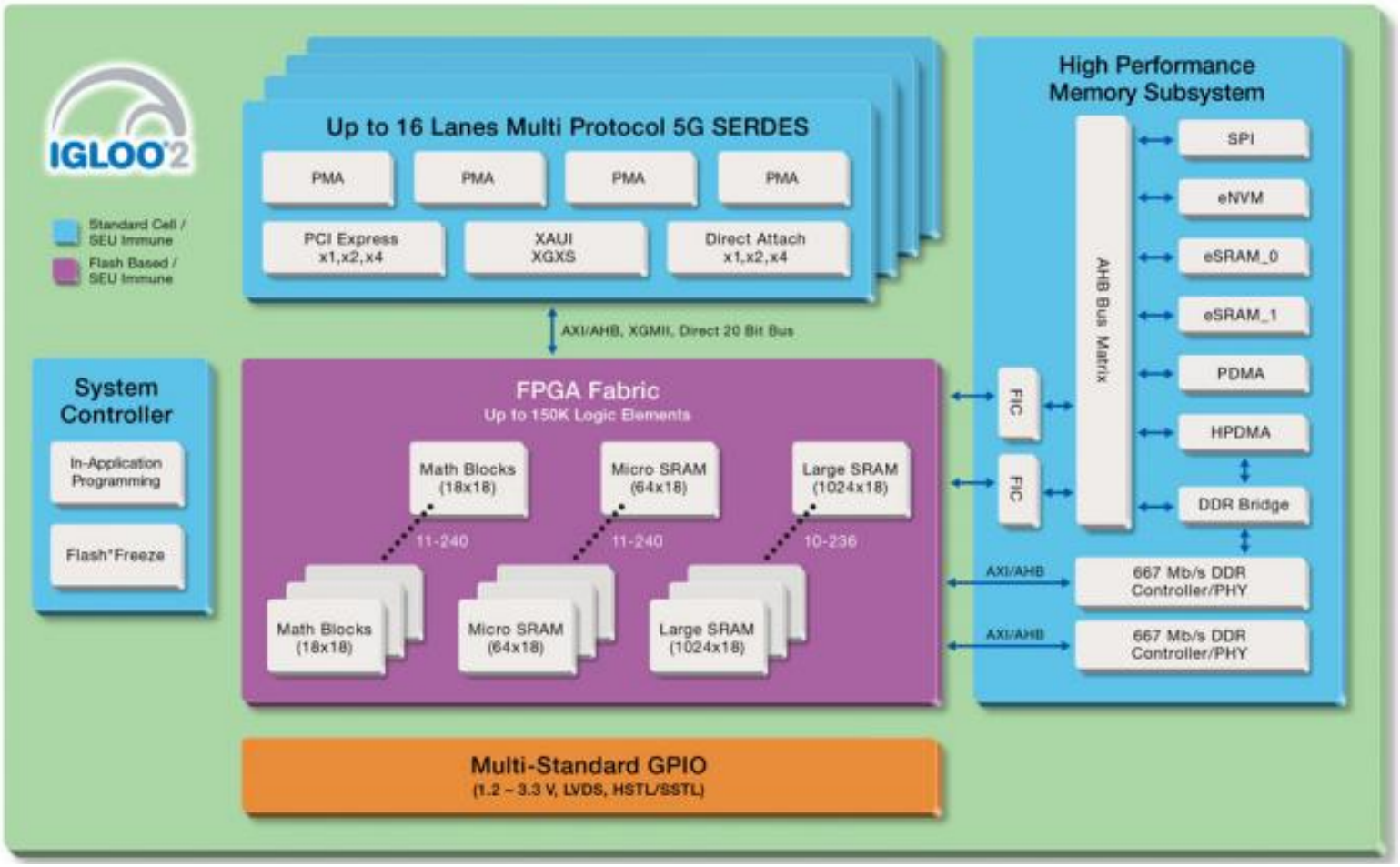
- Supports DDR2 and DDR3 at 333 MHz (667 Mbps), LPDDR at 266 MHz (533 Mbps)-Max Clock Rate
- EDAC Option with SECDED
- Supports x9, x12, x18 and x36 Bus Widths

Specifications

- 1.2 V Nominal Core Voltage
- Single-Ended I/Os: LVCMOS 1.2 V to 3.3 V, LVTTL, PCI
- Voltage Reference I/Os with Performance at 600+ Mbps
  - SSTL2, SSTL18, SSTL15, HSTL18, HSTL15
- True LVDS (600+ Mbps) with Built-in Termination
- Clock Sources Include High-Precision 50 MHz Embedded RC Oscillator
- Up to 8 Clock Conditioning Circuits (CCCs) with PLLs
  - Frequency: Input 1 to 200 MHz, Output 20 to 400 MHz

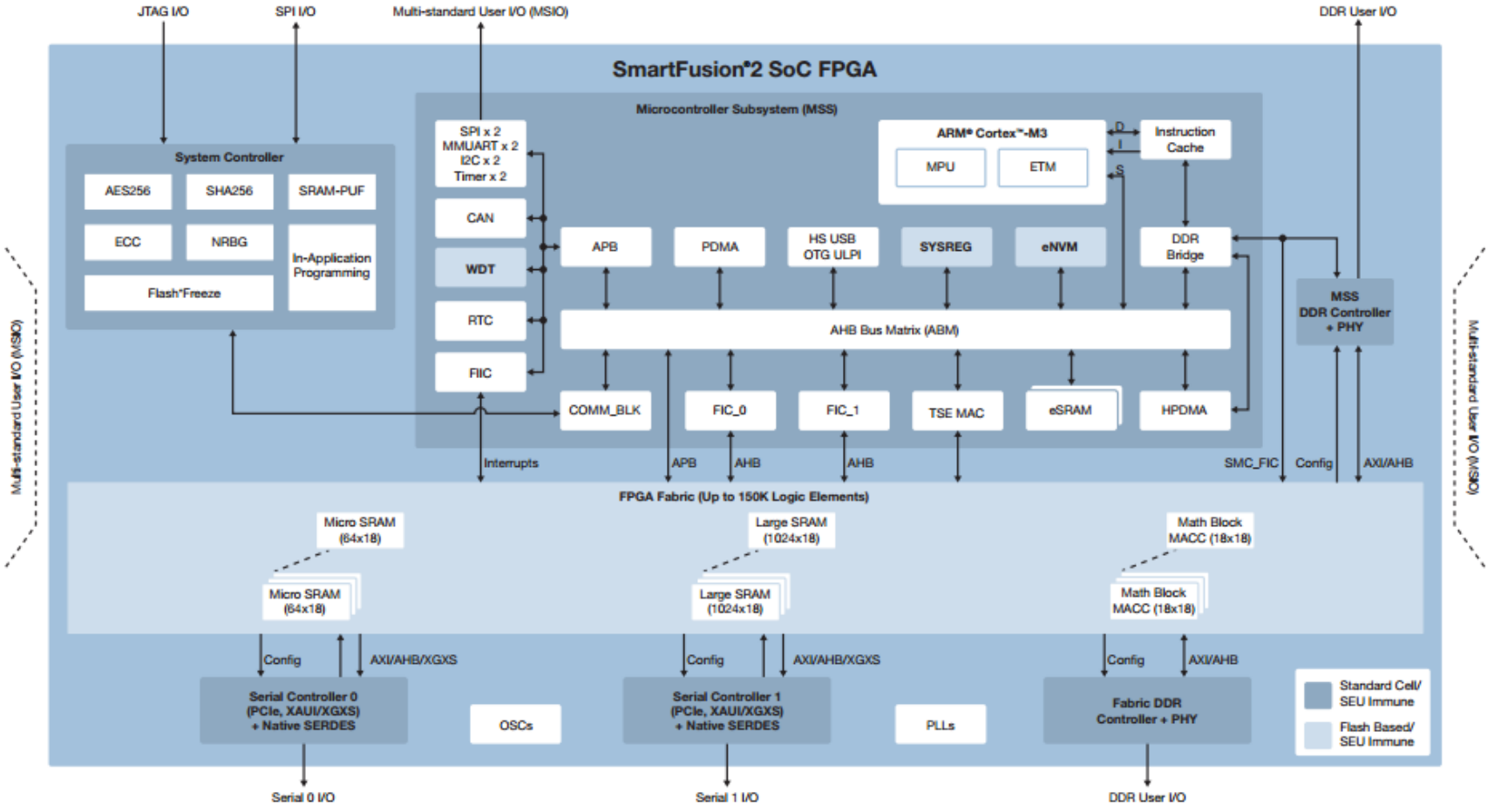
- *Flash configuration immune to radiation*
- *65 nm and Epi for SEL immunity - RHBP*
- *Indirectly Coupled Interconnected for TID*
- *SET & SEU Hardened Flip Flops using TMR - RHBC*
- *SECDED EDAC on LSRAM and uSRAM - RHBA*
- *Interleaving of memory cells - RHBL*

65nm, Flash, Microsemi IGLOO2

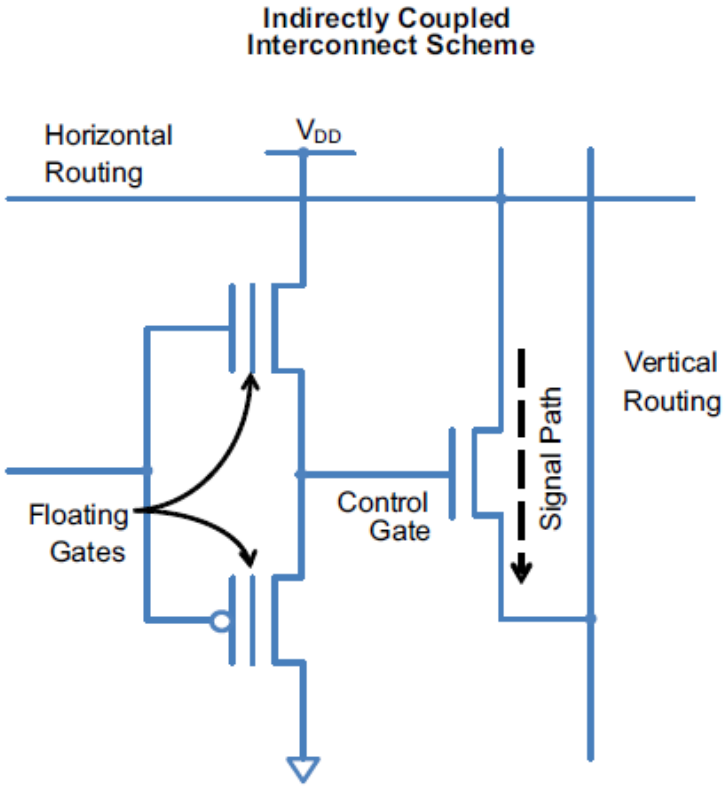


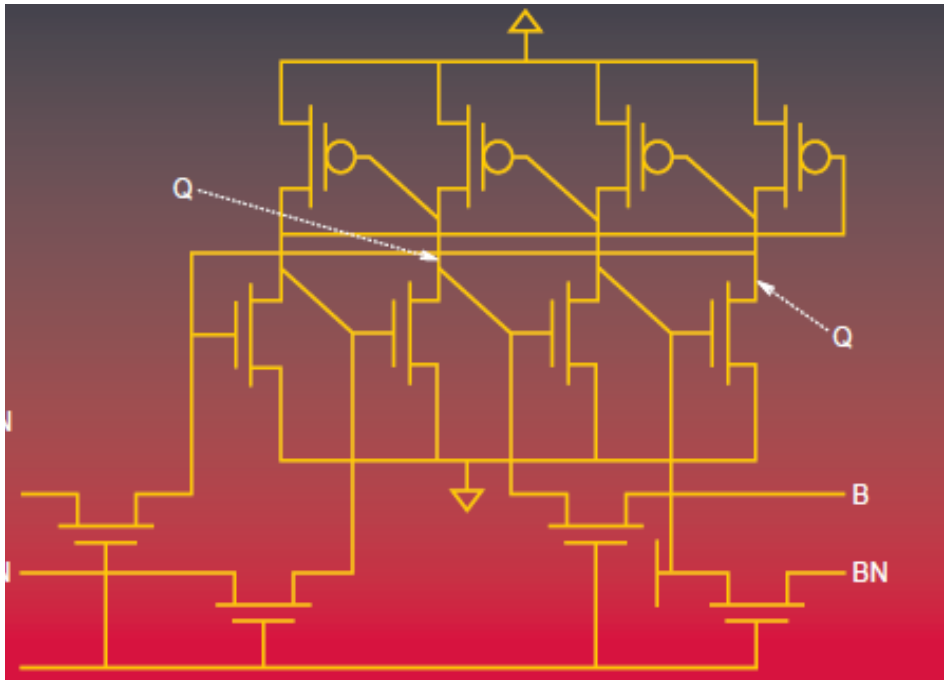
Non-destructive single event latch-ups were encountered in heavy ion testing at energy levels of 24 MeV-cm^2/mg and higher, making the SmartFusion2 SoC FPGAs and IGLOO2 FPGAs unsuitable for space-flight applications.

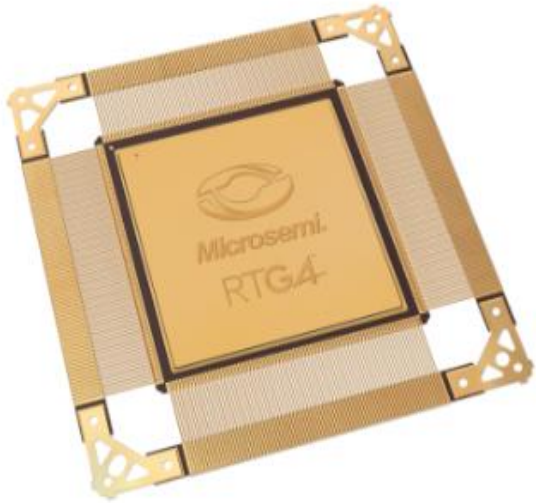
65nm, Flash, Smart Fusion 2 SoC



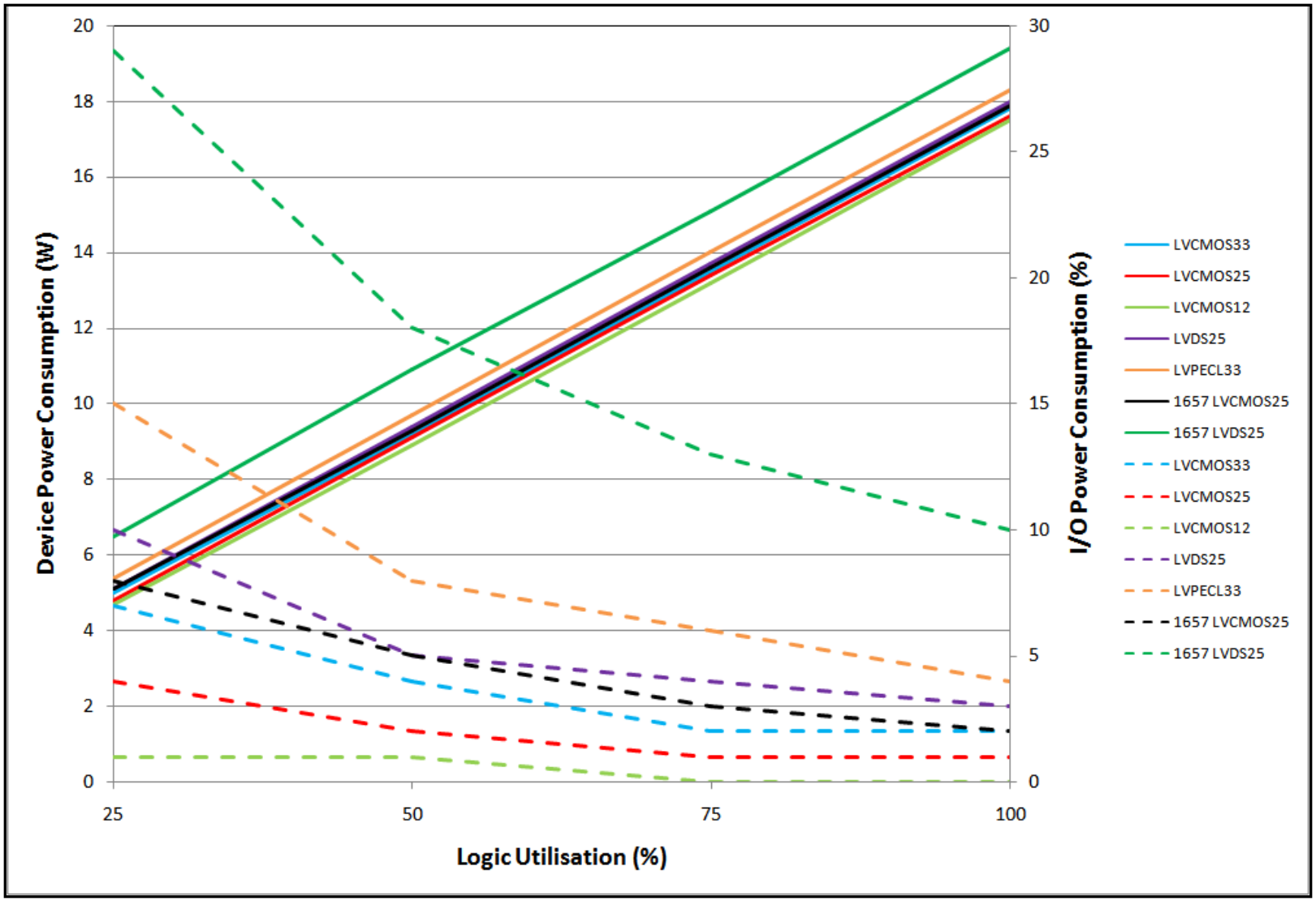
RTG4 vs. Hardened SRAM Configuration







Peripherals	Features	RT4G150	
	Packages	CCGA/CLGA1657	CQ352
Logic/DSP	Maximum logic elements (LUT4 + TMR flip-flop)[1]	151,824	151,824
	Mathblocks (18-bit × 18-bit)	462	462
	Radiation-tolerant PLLs	8	8
Memory	LSRAM 24.5 kbit blocks	209	209
	uSRAM 1.5 kbit blocks	210	210
	Total SRAM Mbits	5.2	5.2
	uPROM kbits	374	374
High-Speed Interface	SerDes lanes	24	4
	PCIe endpoints	2	1
	DDR SDRAM controllers With ECC	2	0
	SpaceWire clock and data recovery circuits	16	4
User I/Os	MSIO (3.3 V)	240	166
	MSIOD (2.5 V)	300	0
	DDRIO (2.5 V)	180	0
	Total User I/Os (Non-SerDes)	720	166


Device Power Consumption (W)
I/O Power Consumption (%)
Logic Utilisation (%)
0
2
4
6
8
10
12
14
16
18
20
0
5
10
15
20
25
30
25
50
75
100
LVCMOS33
LVCMOS25
LVCMOS12
LVDS25
LVPECL33
1657 LVCMOS25
1657 LVDS25
LVCMOS33
LVCMOS25
LVCMOS12
LVDS25
LVPECL33
1657 LVCMOS25
1657 LVDS25

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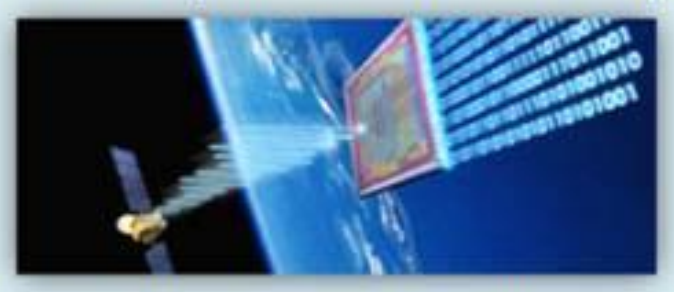

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