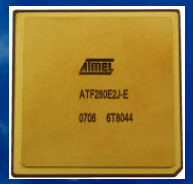
WELCOME

SEFUW:
SpacE FPGA Users Workshop
4th Edition

David Merodio Codinachs (ESA)
David Dangla (CNES)

9-10-11 April 2018



WELCOME TO ESTEC

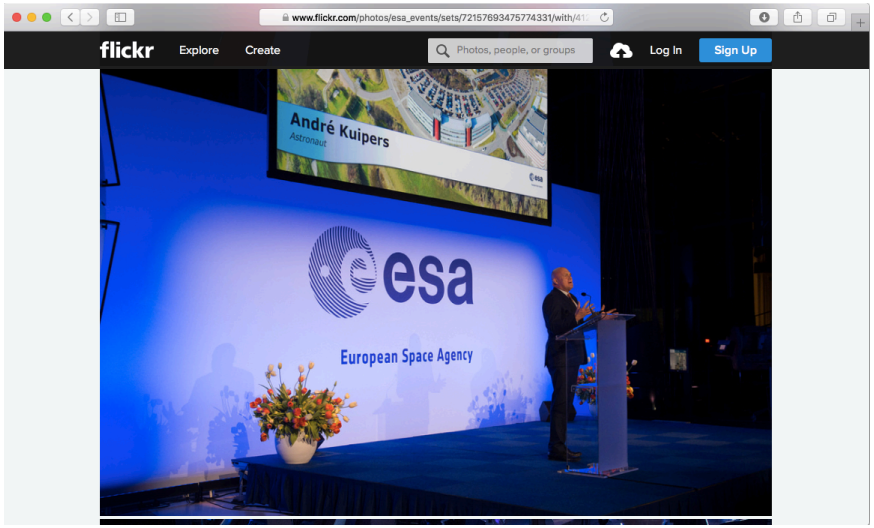
European Space Research and Technology Centre (ESTEC)

http://www.esa.int/About_Us/ESTEC

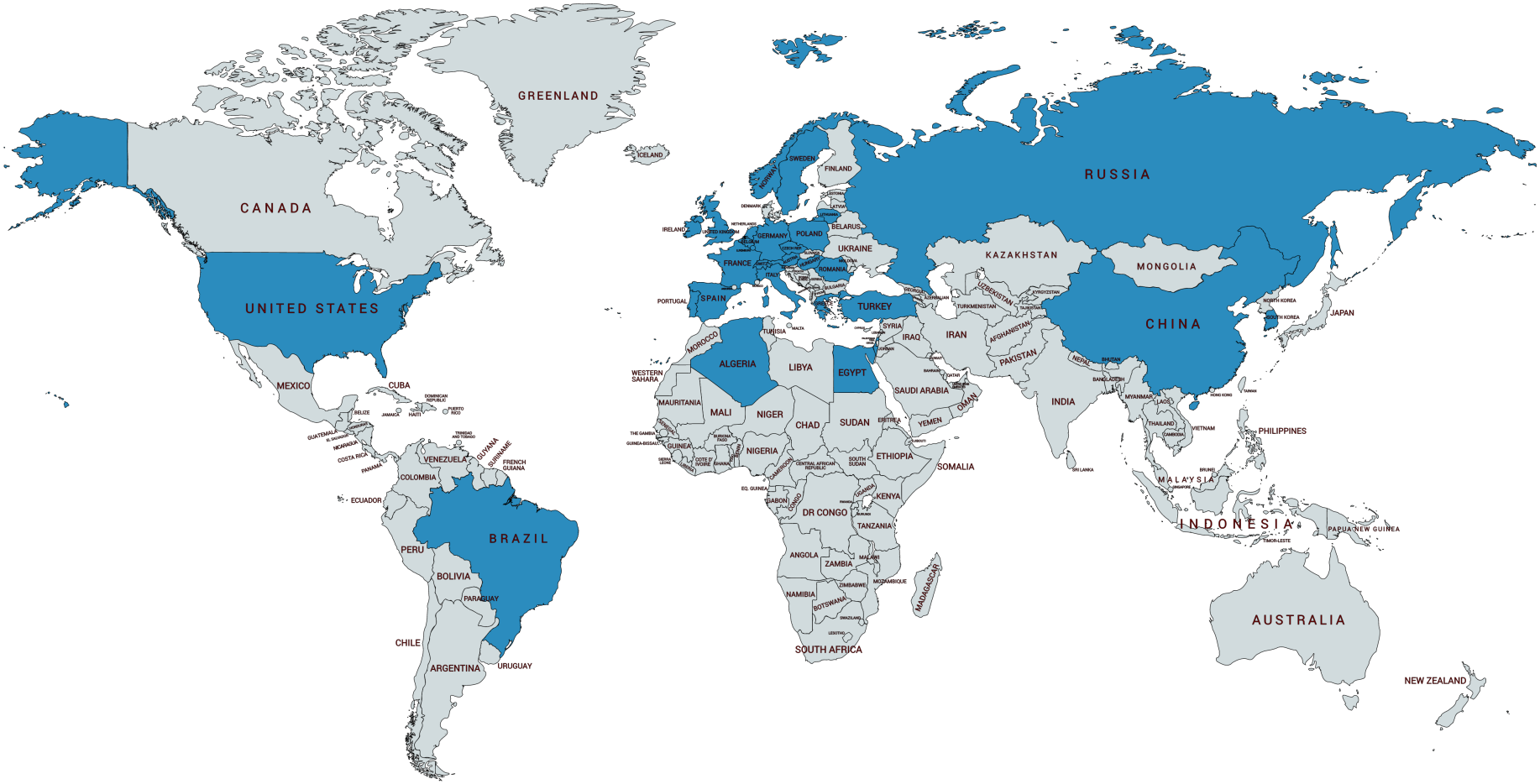
50 Years of ESTEC

http://esamultimedia.esa.int/docs/ESTEC/50ESTEC_BR-339_final.pdf

3rd April 1968



SEFUW registrants map



Created with mapchart.net ©

Sponsors

Coffee breaks and

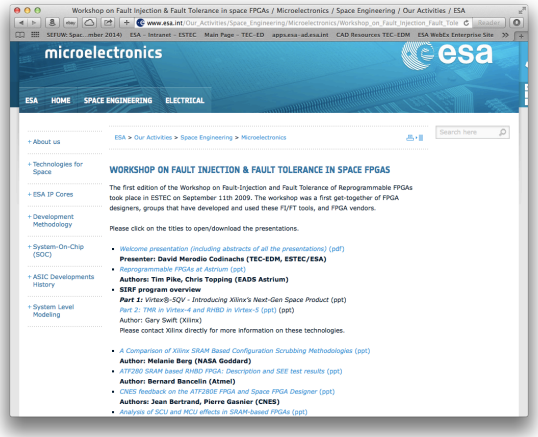
Cocktail reception during the Demo Session are sponsored by

Precursor experiences and SEFUW editions

http://spacefpga.atmel-nantes.fr/spacefpga/

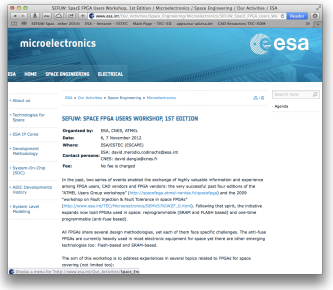
***ATMEL** Aerospace FPGA working group: Workshops and website*

***Workshop** on Fault Injection & Fault Tolerance in space FPGAs (2009)*



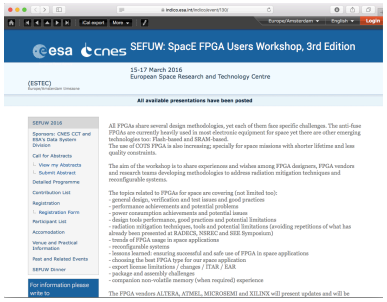
http://www.esa.int/TEC/Microelectronics/SEMV57KIWZF_0.html

1st **SEFUW**, Oct **2012**



2nd **SEFUW**, Sep **2014**

4TH **SEFUW**, Mar **2016**

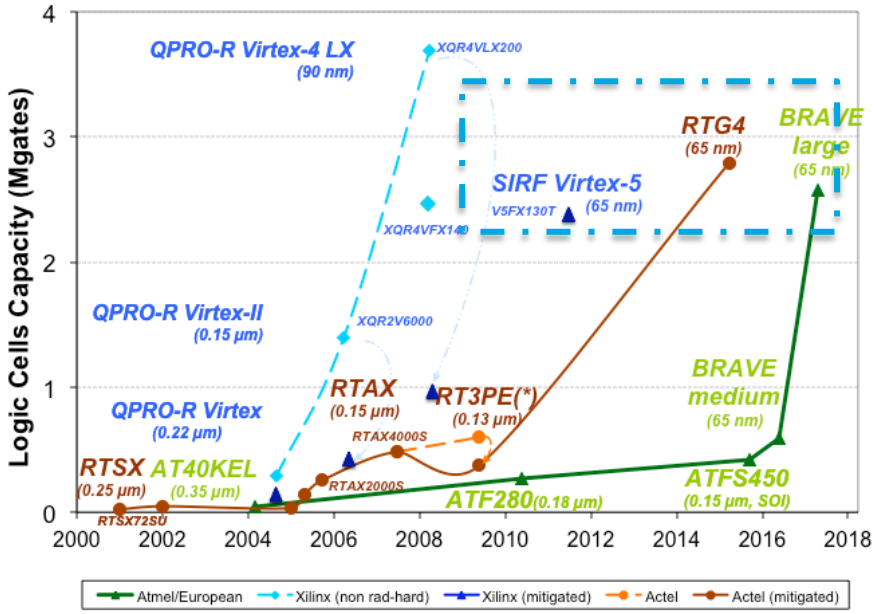


SEFUW Objective

Exchange of highly valuable information and experience among **FPGA users**, **researchers**, **Tool vendors** and **FPGA vendors**

FPGA Updates and trends

- **FPGA usage in space has a long heritage**
- **Larger and higher performance FPGAs are available for space**
- **Design methodology and tools**
  - FPGA development requires methodologies and tools
  - As FPGA complexity increases, more and better tools are required
  - For space, FPGA designers have extra needs (specially for COTS !)

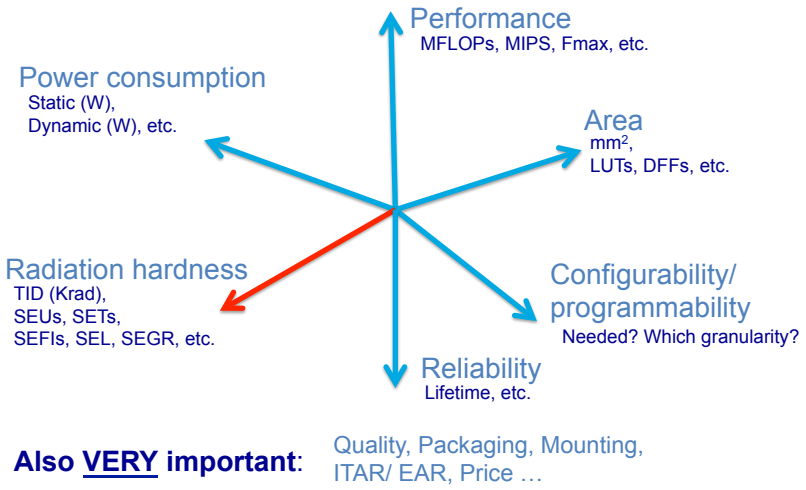


Note 1: Logic capacities shown is design-dependent

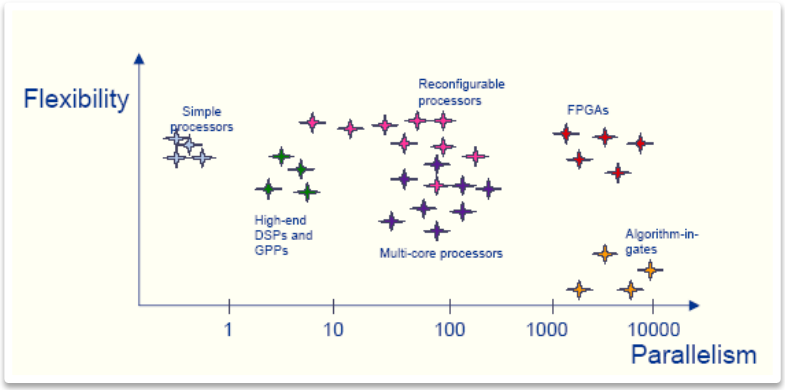
Note 2: RTG4, ATFS450 and BRAVE dates are for Engineering Samples

FPGA Updates and trends

- **COTS FPGA usage is growing**
  - The **trade-offs** in the use of COTS FPGAs to meet the mission requirements needs to be carefully assessed
  - Potentially even larger and higher performance



Also VERY important: Quality, Packaging, Mounting, ITAR/ EAR, Price …



Source: BDTi, "Benchmarking Multithreaded, Multicore and Reconfigurable Processors", 2006

- **FPGA application domain is expanding**:
  - High performance with FPGAs
  - Re-programmability

FPGA vendors and Tool vendors

- **Space FPGA vendors in SEFUW 2018:**

Microsemi

XILINX ALL PROGRAMMABLE™

NanoXplore

- **Tool vendors in SEFUW 2018:**

SYNOPSYS®

Mentor® A Siemens Business

VSYNC circuits

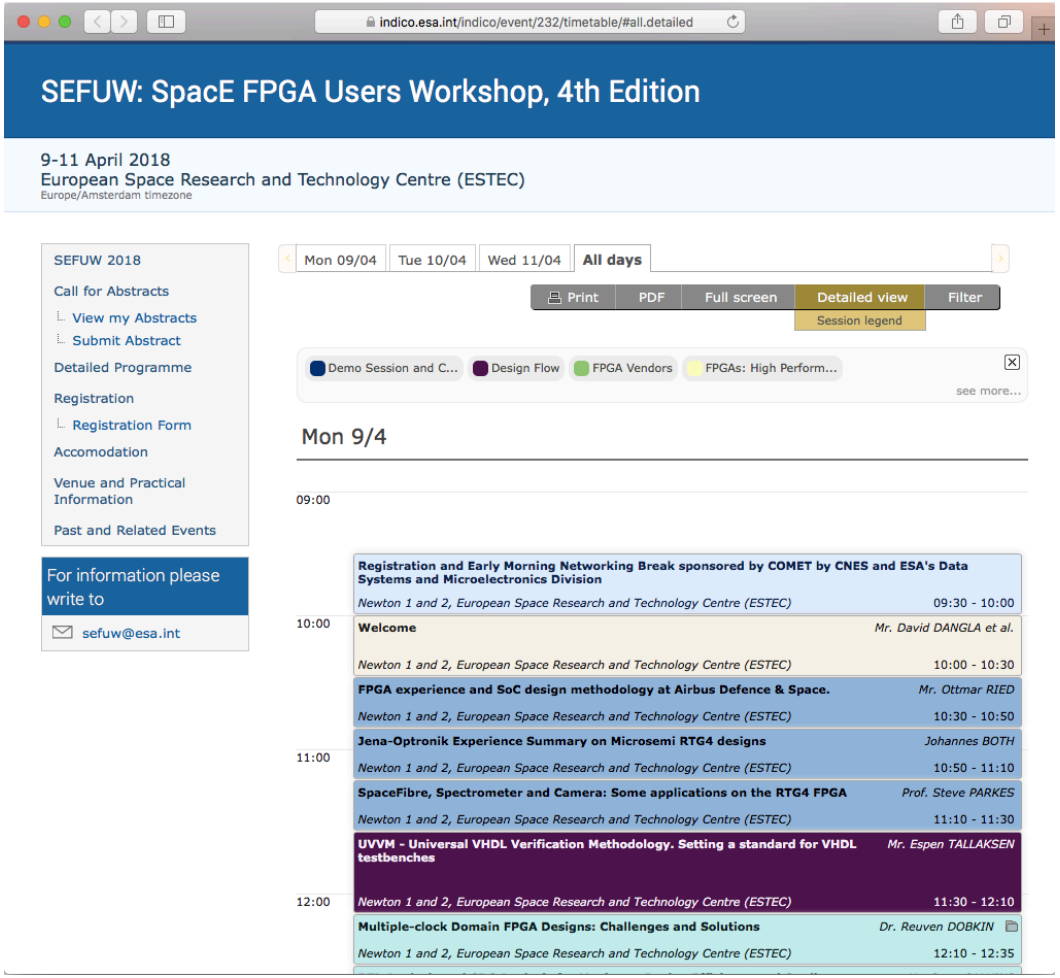
Blue Pearl Software

MathWorks®

Agenda (1/3)

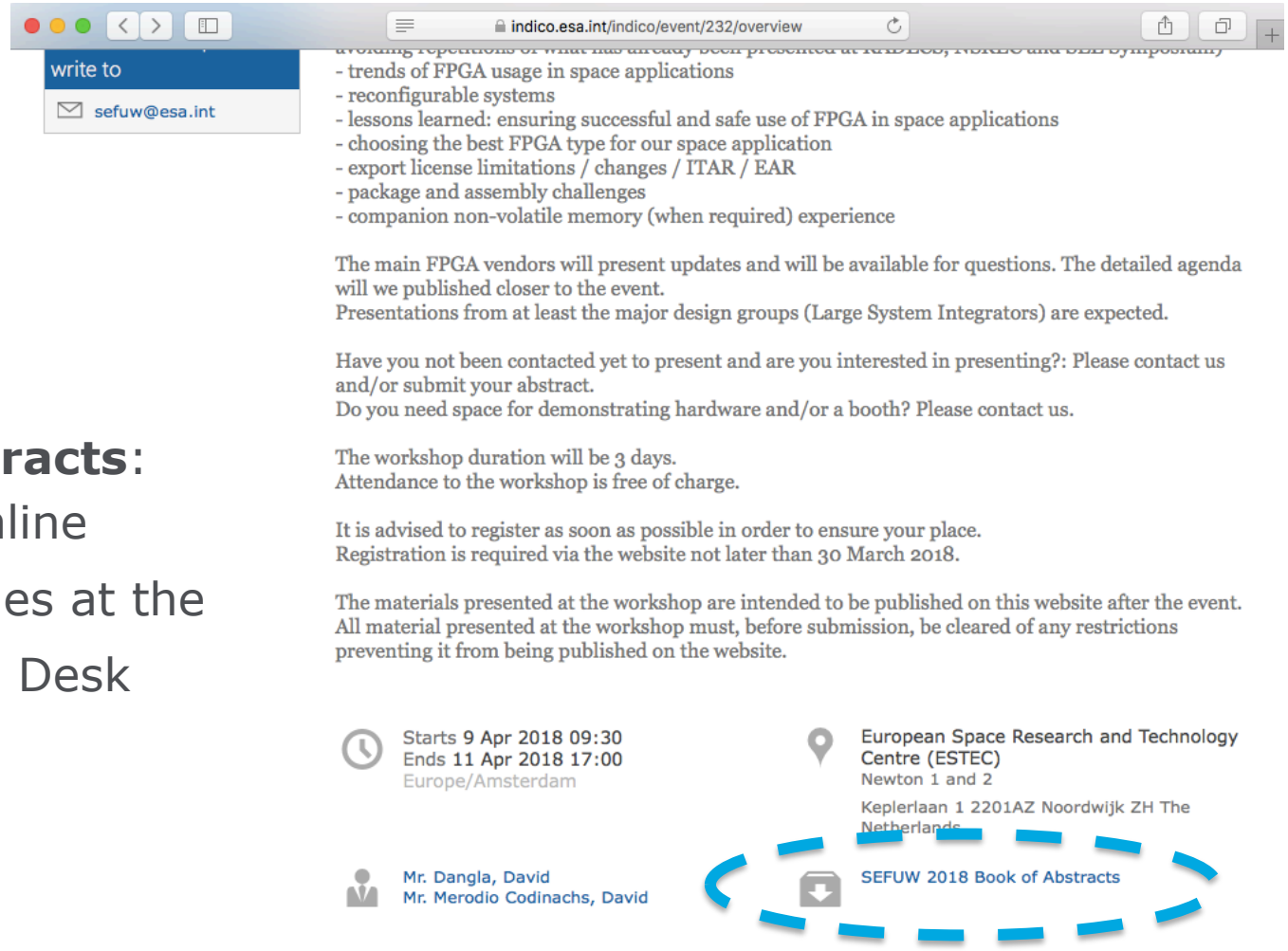
https://indico.esa.int/indico/event/232/timetable/#all.detailed

The agenda has been distributed among the participants



Agenda (2/3)

https://indico.esa.int/indico/event/232/overview



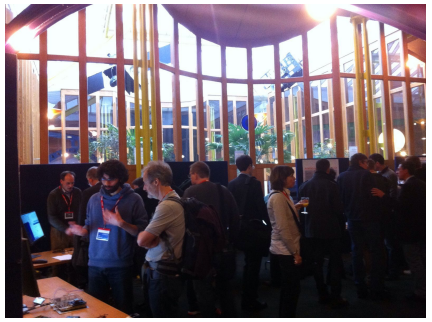
SEFUW 2018

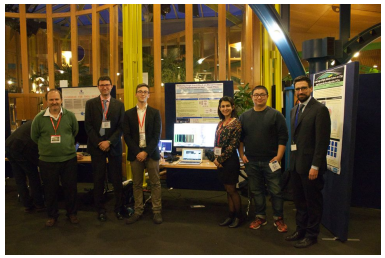
Books of Abstracts:

- available online
- Printed copies at the Registration Desk

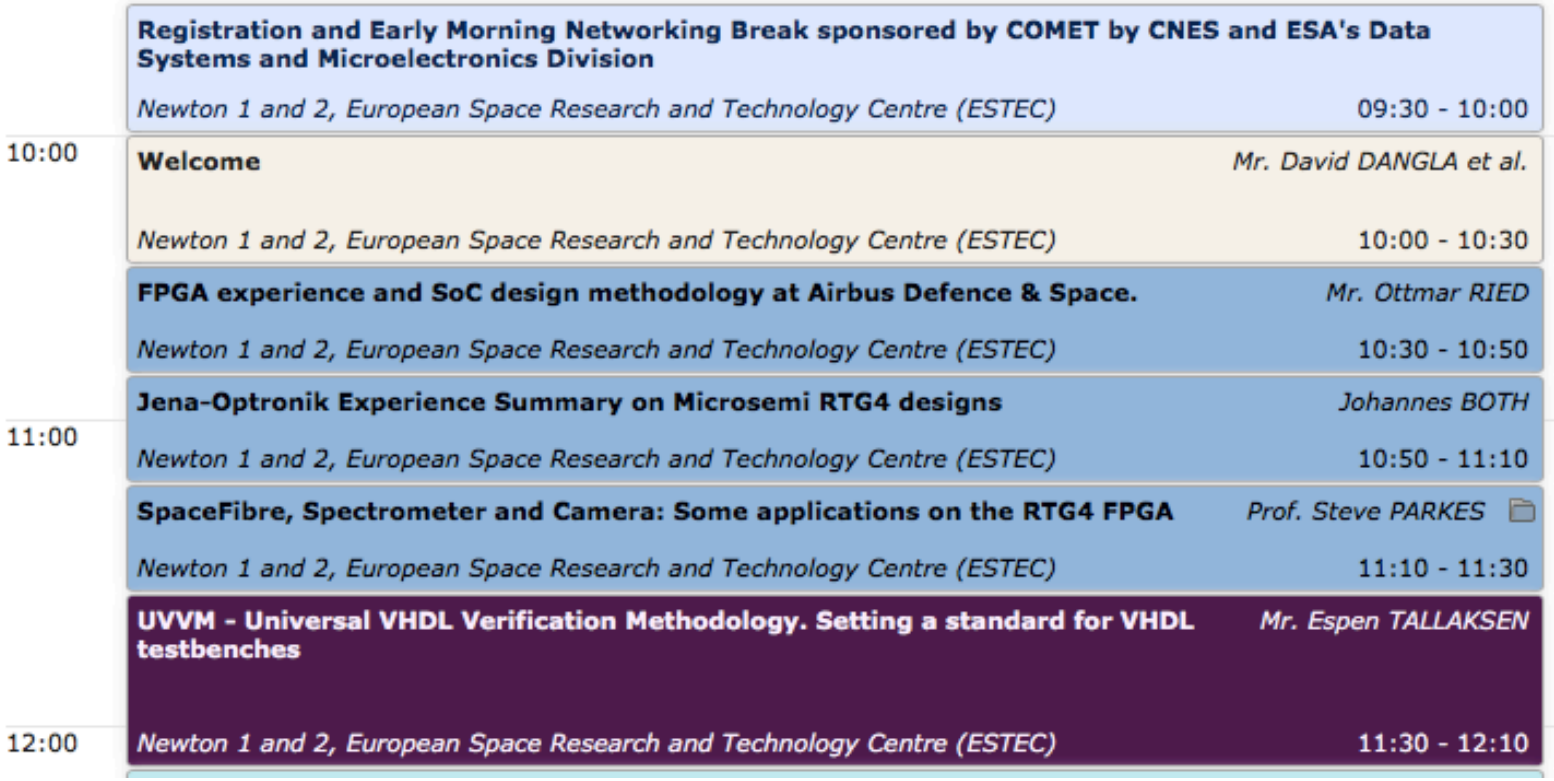
Agenda (3/3)

- **Sessions**
  - FPGA Vendors
  - Tools Vendors
  - Design Flow
  - Fault Tolerant Methodologies and tools
  - Radiation
  - Reconfiguration
  - High Performance
  - Industrial experiences
- **Demo session**





Monday 9-April-2018 (1/3)



Session

Industrial Experiences

(David Dangla)

Design Flow

(David Merodio)

Monday 9-April-2018 (2/3)

	Multiple-clock Domain FPGA Designs: Challenges and Solutions	*Dr. Reuven DOBKIN*
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	12:10 - 12:35
	RTL Analysis and CDC Analysis for Maximum Design Efficiency and Quality	*Mr. Scott CALKINS*
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	12:35 - 13:00
13:00	**Networking Luncheon**	
	ESTEC Canteen	13:00 - 14:00
14:00	**Build and Debug Highly Reliably FPGA-based Designs**	*Mr. Philipp JACOBSOHN*
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	14:00 - 14:25
	Advanced Verification for FPGAs	*Mr. Simone CATENACCI*
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	14:25 - 14:50
	Exhaustively Verify SEU Mitigation Techniques Using Formal Verification	*Mr. Mark HANDOVER*
15:00	*Newton 1 and 2, European Space Research and Technology Centre (ESTEC)*	14:50 - 15:10

Session

Tool Vendors

Florent Manni

Monday 9-April-2018 (3/3)

Evaluation of MATLAB/Simulink and RTL VHDL HDL environment — *Mr. Klemen BRAVHAR et al.*
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 15:10 - 15:30

FUSIO RT: A New Space Modular Computer Core based on Nanoxplore NG-Medium FPGA — *Mr. Pierre-Xiao WANG et al.*

Analysis and Mitigation of Single Event Upsets in Configuration Memory of Xilinx Kintex7 SRAM-based FPGA — *Dr. BOYANG DU*

16:00

Fault injection for space: FT-Unshades2 updates, experiences and roadmap — *Prof. Hipólito GUZMÁN-MIRANDA*

Networking Coffee Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 16:30 - 17:00

17:00

Demo Session and Cocktail Reception sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division
Mr. David Dangla, Mr. David Merodio Codinachs
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 17:00 - 18:45

18:00

Session

Several Demo-related

Lucana Santos

Organization notes

- **Presenters**:
  - Provide the presentations:
    - Preferably by the day before your presentation
    - Preferably using the Indico system (online)
    - Alternatively during the breaks or have your laptop ready.

- **All attendees, transportation**:
  - Taxi and Shuttle options
  - Check the "SEFUW 2018 Book of Abstracts"

http://www.esa.int/About_Us/ESTEC/Transport_to_and_from_ESTEC

Organization notes

- **Round Table** (**Tue 10 at 17:30**):
  - **Initial topics**:
    - New space and COTS: risks and advantages
    - More complex FPGAs for Space: are all teams ready to manage them?
    - High-performance: FPGAs enabling acceleration and new application.
    - Re-configurability: relatively new for space.
    - High Level Languages: pros and cons, experiences
  - **To all**:
    - Would you like to provide written feedback?
      - PowerPoint Slide/s, text, …
    - Do you have more topics to propose?
    - Send an email to david.merodio.codinachs@esa.int

Useful Information

- **Networking Coffee Break sponsored by COMET by CNES and ESA's Data System and Microelectronics Division (TEC-ED)**

- **Networking Luncheon** at ESTEC main canteen

- **Wireless access**:
  - Login and password included at the back of your visitor badge. Valid throughout the workshop

SSID: **esa-public** Authentication: Open
Username: *d.merodiocodinachs*
Password: *xxxxxx*

If your badge does NOT include this information,

please report to the Registration Desk

Optional Social Dinner

Restaurant: ESTEC Canteen

Date: 10-April-2018

At 6:45pm

Price: 50 EUR

The price includes a small plates menu served buffet-style and a drink arrangement.

MENU

Selection of Starters

* *

Selection of Main courses

* *

Dessert Buffet

Example Menu 1

Starters

* *

Marinated Salmon
Green salad with dressing
Quinoa salad with grilled Tofu
Bread & Butter

Main course

* *

Salmon with wine sauce
Grilled veal steak with mustard tarragon sauce
Tomato with Quinoa and Ratatouille
Potato cakes
Courgette and eggplant gratin


ENJOY THE WORKSHOP !!!