

WELCOME

SEFUW: Space FPGA Users Workshop 4th Edition

David Merodio Codinachs (ESA)
David Dangla (CNES)

9-10-11 April 2018



European Space Research and Technology Centre (ESTEC)

http://www.esa.int/About_Us/ESTEC



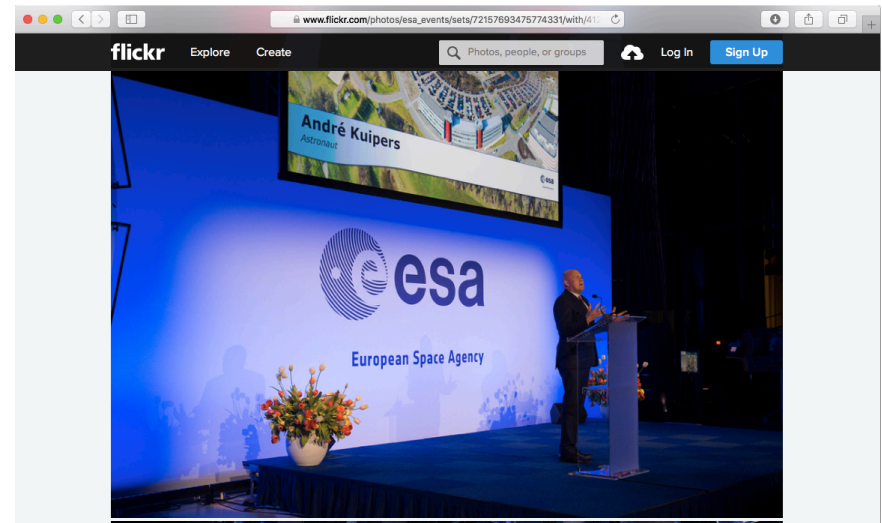
50 Years of ESTEC

http://esamultimedia.esa.int/docs/ESTEC/50ESTEC_BR-339_final.pdf

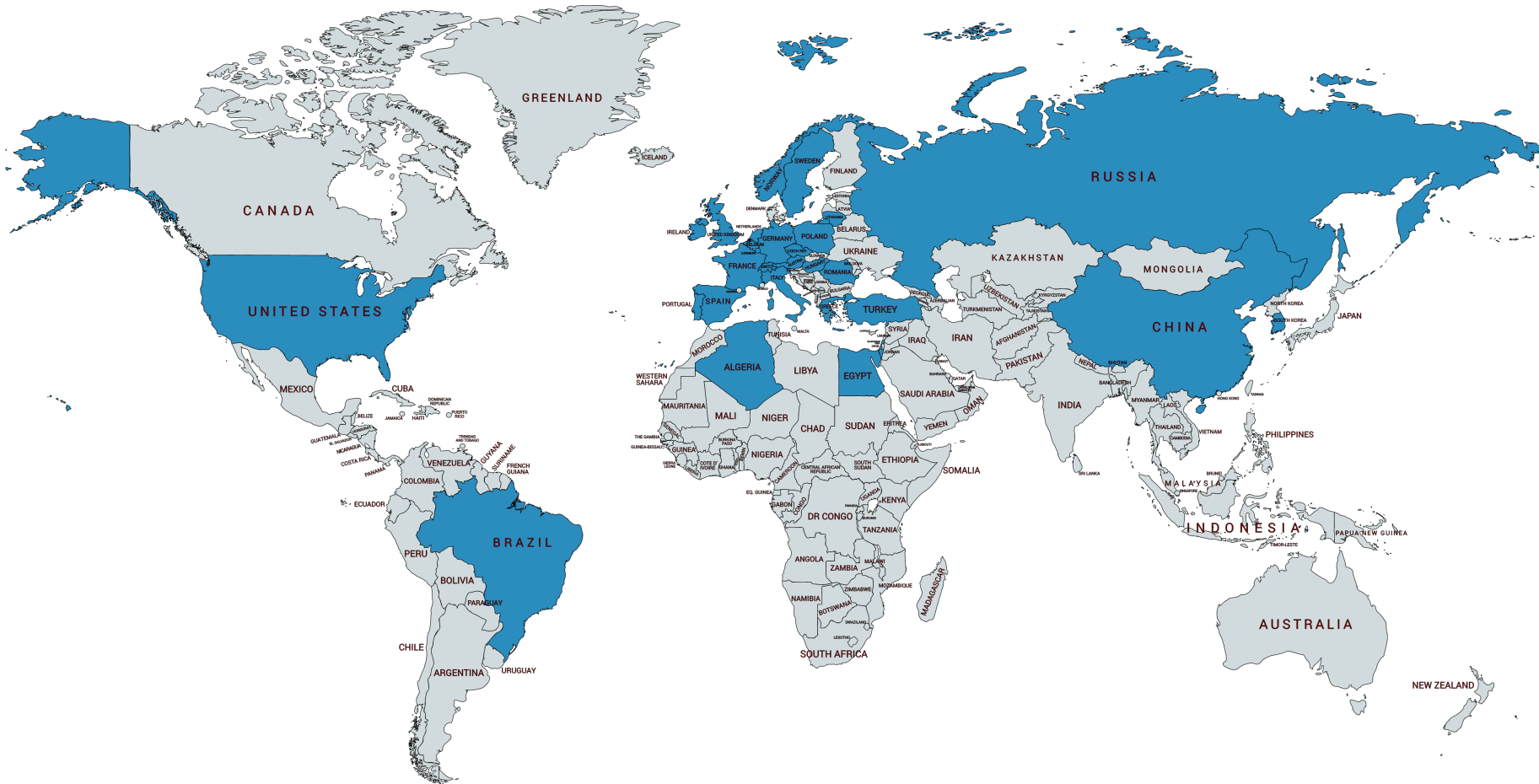


→ ROYAL INAUGURATION

3rd April 1968



SEFUW registrants map



Created with mapchart.net ©



Coffee breaks and Cocktail reception during the Demo Session are sponsored by



Precursor experiences and SEFUW editions

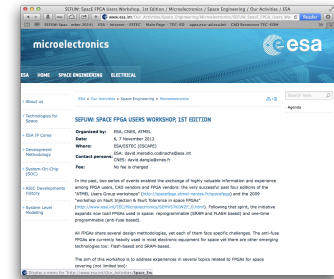


<http://spacefpga.atmel-nantes.fr/spacefpga/>

ATMEL Aerospace
FPGA working group:
Workshops and
website

**Workshop on Fault
Injection & Fault
Tolerance in space
FPGAs (2009)**

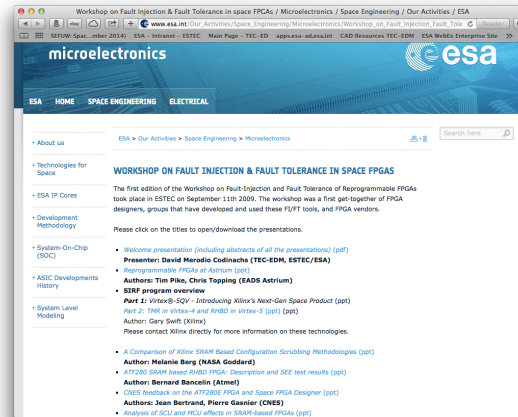
1st SEFUW, Oct 2012



2nd SEFUW, Sep 2014



4th SEFUW, Mar 2016

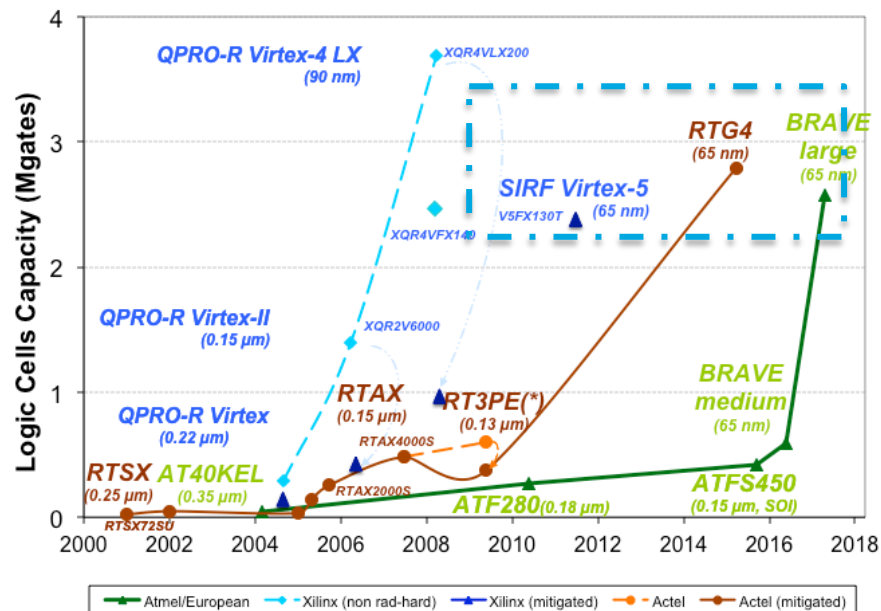


http://www.esa.int/TEC/Microelectronics/SEMV57KIWZF_0.html



Exchange of highly valuable
information and experience among
**FPGA users, researchers, Tool
vendors and FPGA vendors**

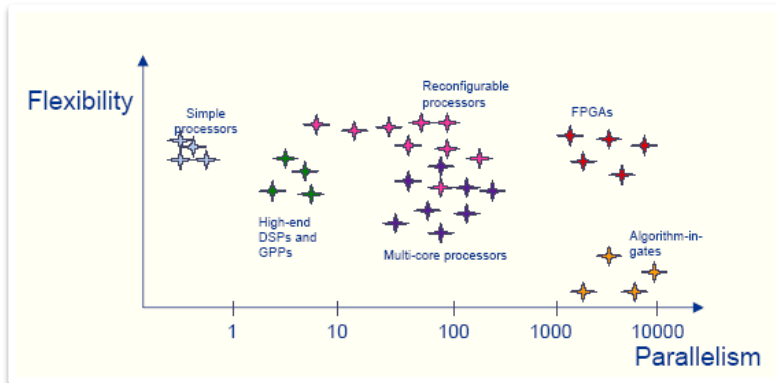
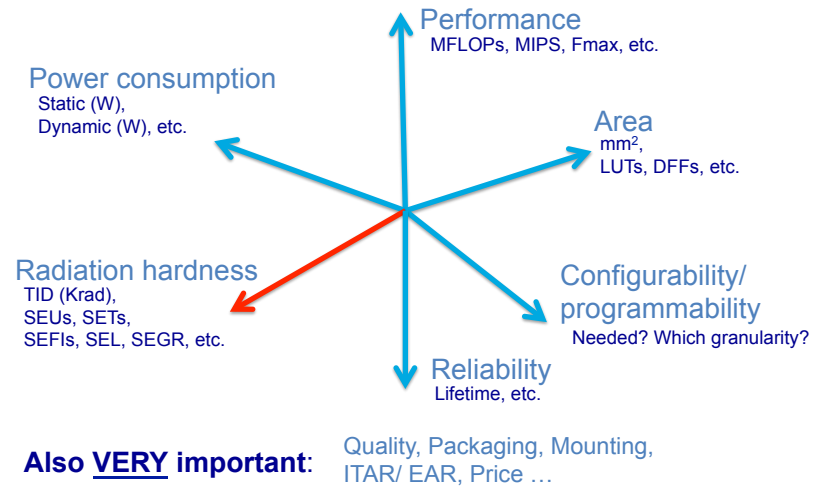
- **FPGA usage in space has a long heritage**
- **Larger and higher performance FPGAs are available for space**
- **Design methodology and tools**
 - FPGA development requires methodologies and tools
 - As FPGA complexity increases, more and better tools are required
 - For space, FPGA designers have extra needs (specially for COTS !)



Note 1: Logic capacities shown is design-dependent

Note 2: RTG4, ATFS450 and BRAVE dates are for Engineering Samples

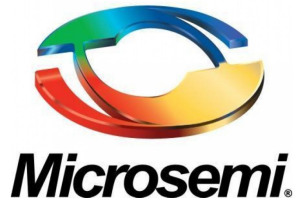
- **COTS FPGA usage is growing**
 - The **trade-offs** in the use of COTS FPGAs to meet the mission requirements needs to be carefully assessed
 - Potentially even larger and higher performance



Source: BDTi, “Benchmarking Multithreaded, Multicore and Reconfigurable Processors”, 2006

- **FPGA application domain is expanding:**
 - High performance with FPGAs
 - Re-programmability

- **Space FPGA vendors in SEFUW 2018:**

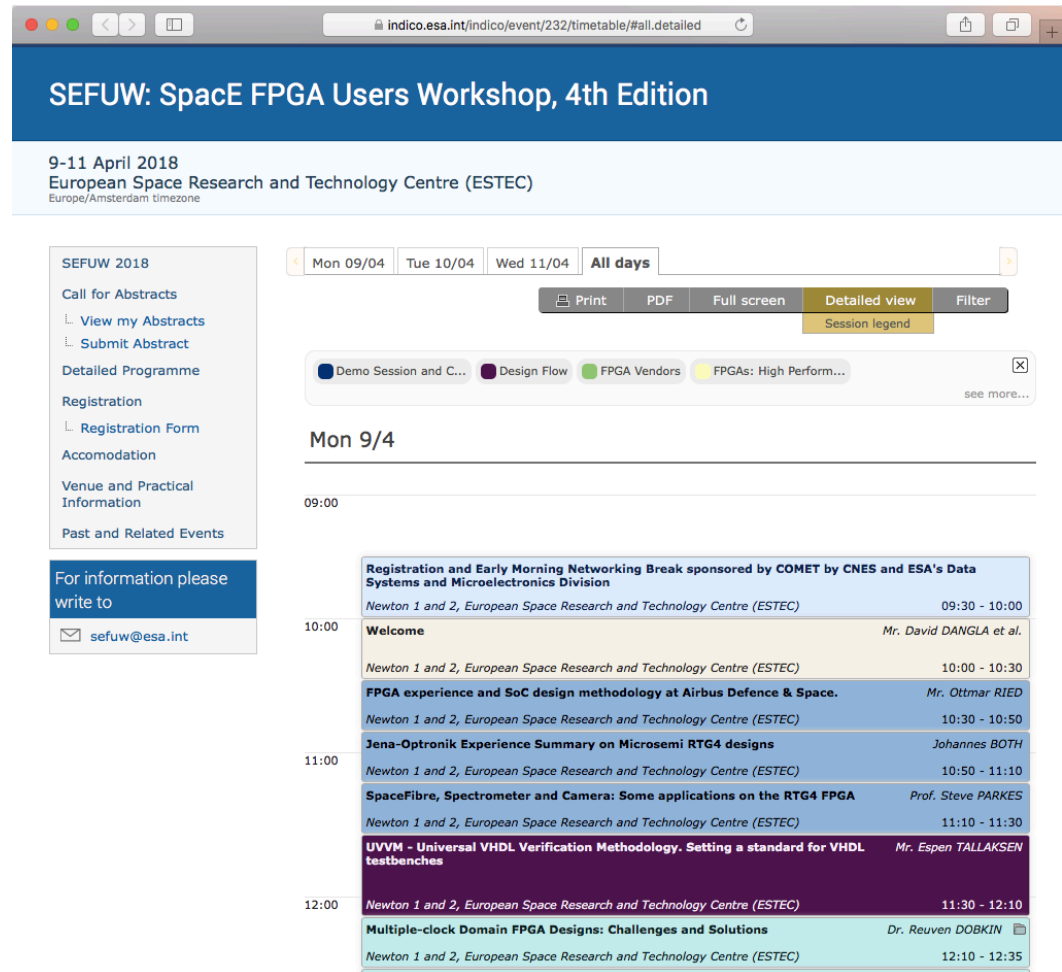


- **Tool vendors in SEFUW 2018:**



<https://indico.esa.int/indico/event/232/timetable/#all.detailed>

The agenda has been distributed among the participants



SEFUW: Space FPGA Users Workshop, 4th Edition

9-11 April 2018
European Space Research and Technology Centre (ESTEC)
Europe/Amsterdam timezone

SEFUW 2018

- Call for Abstracts
 - View my Abstracts
 - Submit Abstract
- Detailed Programme
- Registration
 - Registration Form
- Accommodation
- Venue and Practical Information
- Past and Related Events

For information please write to sefuw@esa.int

Mon 09/04 | Tue 10/04 | Wed 11/04 | **All days**

Print | PDF | Full screen | **Detailed view** | Filter

Session legend

Demo Session and C... | Design Flow | FPGA Vendors | **FPGAs: High Perform...** | see more...

Mon 9/4

09:00

Registration and Early Morning Networking Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 09:30 - 10:00

10:00 **Welcome** *Mr. David DANGLA et al.*
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 10:00 - 10:30

FPGA experience and SoC design methodology at Airbus Defence & Space. *Mr. Ottmar RIED*
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 10:30 - 10:50

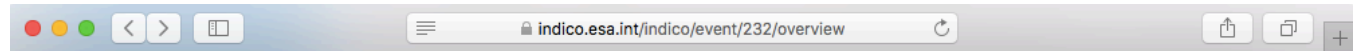
11:00 **Jena-Optronik Experience Summary on Microsemi RTG4 designs** *Johannes BOTH*
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 10:50 - 11:10

SpaceFibre, Spectrometer and Camera: Some applications on the RTG4 FPGA *Prof. Steve PARKES*
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 11:10 - 11:30

UVVM - Universal VHDL Verification Methodology. Setting a standard for VHDL testbenches *Mr. Espen TALLAKSEN*

12:00 **Multiple-clock Domain FPGA Designs: Challenges and Solutions** *Dr. Reuven DOBKIN*
Newton 1 and 2, European Space Research and Technology Centre (ESTEC) 12:10 - 12:35

<https://indico.esa.int/indico/event/232/overview>



write to
✉ sefuw@esa.int

- trends of FPGA usage in space applications
- reconfigurable systems
- lessons learned: ensuring successful and safe use of FPGA in space applications
- choosing the best FPGA type for our space application
- export license limitations / changes / ITAR / EAR
- package and assembly challenges
- companion non-volatile memory (when required) experience

The main FPGA vendors will present updates and will be available for questions. The detailed agenda will be published closer to the event. Presentations from at least the major design groups (Large System Integrators) are expected.

Have you not been contacted yet to present and are you interested in presenting?: Please contact us and/or submit your abstract. Do you need space for demonstrating hardware and/or a booth? Please contact us.

The workshop duration will be 3 days. Attendance to the workshop is free of charge.

It is advised to register as soon as possible in order to ensure your place. Registration is required via the website not later than 30 March 2018.

The materials presented at the workshop are intended to be published on this website after the event. All material presented at the workshop must, before submission, be cleared of any restrictions preventing it from being published on the website.

🕒 Starts 9 Apr 2018 09:30
Ends 11 Apr 2018 17:00
Europe/Amsterdam

👤 Mr. Dangla, David
Mr. Merodio Codinachs, David

📍 European Space Research and Technology Centre (ESTEC)
Newton 1 and 2
Keplerlaan 1 2201AZ Noordwijk ZH The Netherlands



SEFUW 2018

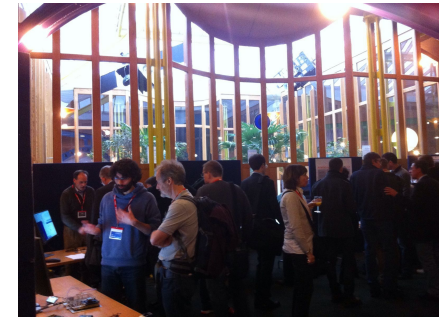
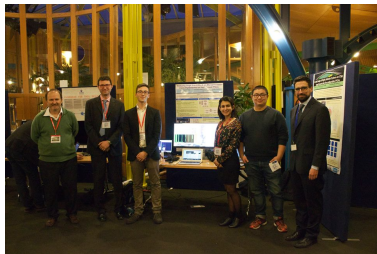
Books of Abstracts:


- available online
- Printed copies at the Registration Desk

- **Sessions**

- FPGA Vendors
- Tools Vendors
- Design Flow
- Fault Tolerant Methodologies and tools
- Radiation
- Reconfiguration
- High Performance
- Industrial experiences

- **Demo session**



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10:00	Welcome	<i>Mr. David DANGLA et al.</i>
	<i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i>	10:00 - 10:30
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	<i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i>	10:30 - 10:50
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Session

Industrial Experiences

(David Dangla)

Design Flow

(David Merodio)

Session

Tool Vendors

Florent Manni

	Multiple-clock Domain FPGA Designs: Challenges and Solutions Dr. Reuven DOBKIN  <i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 12:10 - 12:35
	RTL Analysis and CDC Analysis for Maximum Design Efficiency and Quality Mr. Scott CALKINS  <i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 12:35 - 13:00
13:00	Networking Luncheon <i>ESTEC Canteen</i> 13:00 - 14:00
14:00	Build and Debug Highly Reliably FPGA-based Designs Mr. Philipp JACOBSON  <i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 14:00 - 14:25
	Advanced Verification for FPGAs Mr. Simone CATENACCI  <i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 14:25 - 14:50
15:00	Exhaustively Verify SEU Mitigation Techniques Using Formal Verification Mr. Mark HANDOVER  <i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 14:50 - 15:10

Session

Several Demo-related

Lucana Santos

	<p>Evaluation of MATLAB/Simulink and RTL VHDL HDL environment <i>Mr. Klemen BRAVHAR et al.</i></p> <p><i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 15:10 - 15:30</p>
	<p>FUSIO RT: A New Space Modular Computer Core based on Nanoplore NG-Medium FPGA <i>Mr. Pierre-Xiao WANG et al.</i></p>
16:00	<p>Analysis and Mitigation of Single Event Upsets in Configuration Memory of Xilinx Kintex7 SRAM-based FPGA <i>Dr. BOYANG DU</i></p>
	<p>Fault injection for space: FT-Unshades2 updates, experiences and roadmap <i>Prof. Hipólito GUZMÁN-MIRANDA</i></p>
	<p>Networking Coffee Break sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division</p> <p><i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 16:30 - 17:00</p>
17:00	<p>Demo Session and Cocktail Reception sponsored by COMET by CNES and ESA's Data Systems and Microelectronics Division</p> <p><i>Mr. David Dangla, Mr. David Merodio Codinachs</i></p>
18:00	<p><i>Newton 1 and 2, European Space Research and Technology Centre (ESTEC)</i> 17:00 - 18:45</p>

- **Presenters:**

- Provide the presentations:

- Preferably by the day before your presentation
 - Preferably using the Indico system (online)
 - Alternatively during the breaks or have your laptop ready.

- **All attendees, transportation:**

- Taxi and Shuttle options
 - Check the "SEFUW 2018 Book of Abstracts"

http://www.esa.int/About_Us/ESTEC/Transport_to_and_from_ESTEC

- **Round Table (Tue 10 at 17:30):**
 - **Initial topics:**
 - New space and COTS: risks and advantages
 - More complex FPGAs for Space: are all teams ready to manage them?
 - High-performance: FPGAs enabling acceleration and new application.
 - Re-configurability: relatively new for space.
 - High Level Languages: pros and cons, experiences
 - **To all:**
 - Would you like to provide written feedback?
 - PowerPoint Slide/s, text, ...
 - Do you have more topics to propose?
 - Send an email to david.merodio.codinachs@esa.int

- **Networking Coffee Break sponsored by COMET by CNES and ESA's Data System and Microelectronics Division (TEC-ED)**
- **Networking Luncheon** at ESTEC main canteen
- **Wireless access:**
 - Login and password included at the back of your visitor badge. Valid throughout the workshop

SSID: esa-public Authentication: Open
Username: *d.merodiocodinachs*
Password: *xxxxxxx*

If your badge does NOT include this information,
please report to the Registration Desk

Optional Social Dinner

Restaurant: ESTEC Canteen

Date: 10-April-2018

At 6:45pm

Price: 50 EUR



The price includes a small plates menu served buffet-style and a drink arrangement.

MENU

Selection of Starters

* *

Selection of Main courses

* *

Dessert Buffet

Example Menu 1

Starters

* *

Marinated Salmon
Green salad with dressing
Quinoa salad with grilled Tofu
Bread & Butter

Main course

* *

Salmon with wine sauce
Grilled veal steak with mustard
tarragon sauce
Tomato with Quinoa and Ratatouille
Potato cakes
Courgette and eggplant gratin



ENJOY THE WORKSHOP !!!