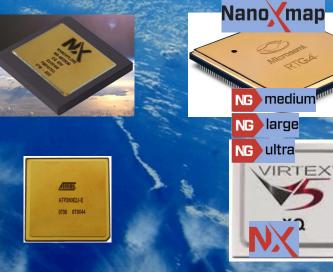


WELCOME

SEFUW: Space FPGA Users Workshop 4th Edition

David Merodio Codinachs (ESA) David Dangla (CNES)

9-10-11 April 2018



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European Space Agency





European Space Research and Technology Centre (ESTEC)

http://www.esa.int/About_Us/ESTEC



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50 Years of ESTEC

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http://esamultimedia.esa.int/docs/ESTEC/50ESTEC BR-339 final.pdf





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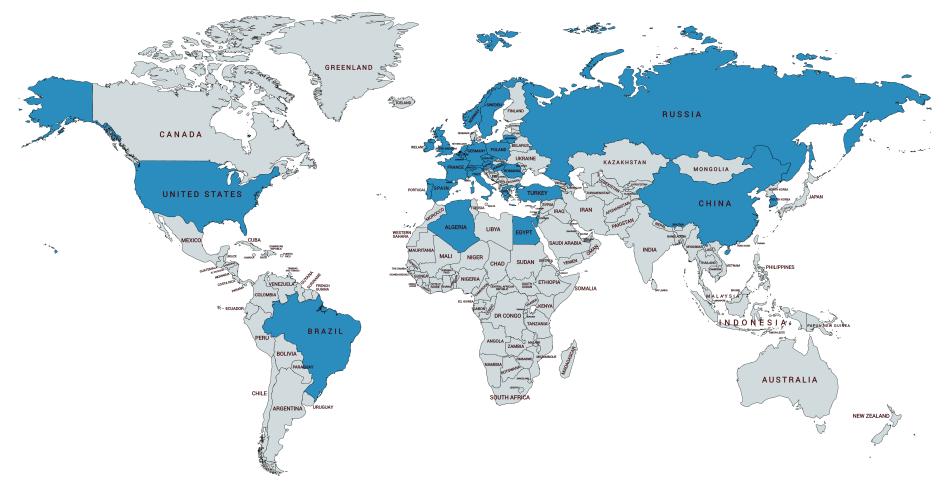
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SEFUW registrants map





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Sponsors



Coffee breaks and Cocktail reception during the Demo Session are sponsored by



Microsystèmes et Composants Electroniques

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Precursor experiences and SEFUW editions

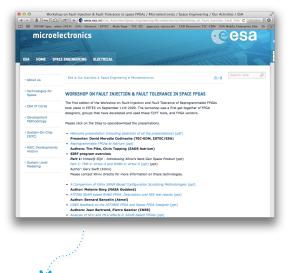


http://spacefpga.atmel-nantes.fr/spacefpga/

ATMEL Aerospace FPGA working group: Workshops and website



Workshop on Fault Injection & Fault Tolerance in space FPGAs (2009)



http://www.esa.int/TEC/Microelectronics/ SEMV57KIWZF_0.html

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1st SEFUW, Oct 2012



2nd SEFUW, Sep 2014

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	alexport More +	2	Europe/Amsterdam	D. Nerodio Codinad
@esa 🕁	cnes ^{SEFL}	JW: SpacE FPGA Use	ers Worksho	p, 2nd Edition
(ESTEC)	16-18 5 Europe	September 2014 an Space Research and Technolo	ogy Centre	
	Note: all availab	le presentations have been posted	on the website	
SEPUW 2014 Sponsor: Thales Communications & Security Cell for Abstracts	FPGAs are curren technologies too:	several design methodologies, yet ea rity heavily used in most electronic e Flash-based and SRAM-based. vekshop is to address experiences in ited tool:	quipment for space ye	t there are other emerging
L View my Abstracts L Submit Abstract Detailed Programme Contribution List	 performance ar power consump design tools per radiation mitig 	verification and test issues and good hisvements and potential problems iton achievements and potential issu- formance, good practices and potential seried at RADECS. NEREC and SEE seried at RADECS.	ies ial limitations limitations (avoiding r	epetitions of what has
Ny Conference L. Ny Contributions Registration L. Modify my Registration	 trends of FPGA lessons learned choosing the be export license li package and as 	usage in space applications ensuring successful and safe use of at FPGA type for our space applicatio mitations / changes / ITAR / EAR sembly challenges -volatile memory (when required) so	FPGA in space applica m	tions
Participant List Accorrectation Verse and Practical Information	The FPGA vendo cuesticos.	-volatile memory (when required) eo rs ATMEL, MICROSEMI and XILIN m at least the major design groups ()	X will present updates	and will be available for
Past and Related Events	Have you not be	n contacted yet to present and are w	o interested in preser	ting?: Please contact us

4TH SEFUW, Mar 2016

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Casa da	SE SE	FUW: SpacE FPGA Use	rs Workshop	, 3rd Edition
(ESTEC)		7 March 2016 pean Space Research and Technolog	gy Centre	
(ESTEC) Europy/InnazerDen Umsaane				
	A	I available presentations have been pos	ned	
SEFUW 2016	AT EDG as de	are several design methodologies, vet each	and these free coordinates	hallowers. The certifican
Sponsons: CNES CCT and ESA's Data System Details	FPGAs are cu technologies (rrently heavily used in most electronic eq too: Flash-based and SRAM-based. ITS FPGA is also increasing: specially for	pripment for space yet t	here are other emerging
Call for Abstracts	quality constr	vists.	space assessed when we	ALL INCLUS AND AND
- View my Abstracts	The aim of th	e workshop is to share experiences and w	ishes among FPGA des	imers, FPGA venders
- Submit Abstract	and research reconfigurabl	teams developing methodologies to addre	no rediation mitigation	techniques and
Detailed Programme	reconfigurate	e systems.		
Cantribution List	The topics rel	ated to FPGAs for space are covering (not gn, verification and test issues and good 1	t Emited too):	
Registration	 general desi performano 	gn, verification and test issues and good 3 achievements and potential problems	practices	
1. Registration Form		imption achievements and potential issue		
Perticipant List	 design tools radiation mi 	performance, good practices and potenti tigation techniques, tools and potential li	al irrefutors insitations (avoiding res	withings of what has
Accompdation	already been	presented at RADECS, NSREC and SEE 5	(ymposium)	
Venue and Practical	 trends of FP reconfigural 	GA mage in space applications		
Information	- Peccengirin	ne systems and: ensuring successful and safe use of P	IRGA in space emplication	201
Post and Related Events		best FPGA type for our space application		48
SEPUR Davier	- export licen	se limitations / charges / ITAR / EAR		
		assembly challenges non-volatile memory (when required) ext		
For information please	- coorparison	investoration constrainty (which reducted) esd	PRIMA	
write to	The FPGA ver	sdors ALTERA, ATMEL, MICROSEMI an	od XILINX will present	updates and will be

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Exchange of highly valuable information and experience among FPGA users, researchers, Tool vendors and FPGA vendors

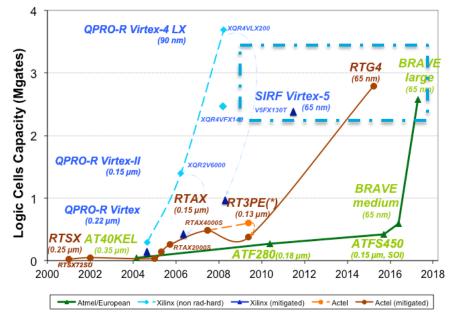
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FPGA Updates and trends



- FPGA usage in space has a long heritage
- Larger and higher performance FPGAs are available for space
- Design methodology and tools
 - FPGA development requires methodologies and tools
 - As FPGA complexity increases, more and better tools are required
 - For space, FPGA designers have extra needs (specially for COTS !)



Note 1: Logic capacities shown is design-dependent

Note 2: RTG4, ATFS450 and BRAVE dates are for Engineering Samples

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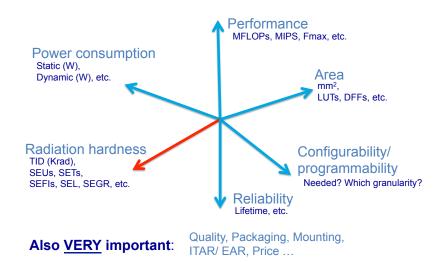
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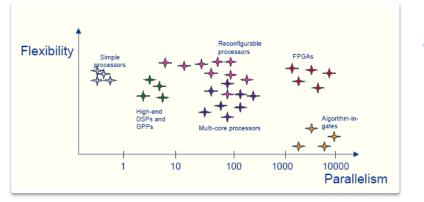
FPGA Updates and trends



• COTS FPGA usage is growing

- The trade-offs in the use of COTS FPGAs to meet the mission requirements needs to be carefully assessed
- Potentially even larger and higher performance





Source: BDTi, "Benchmarking Multithreaded, Multicore and Reconfigurable Processors", 2006

- FPGA application domain is expanding:
 - High performance with FPGAs
 - Re-programmability

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FPGA vendors and Tool vendors



• Space FPGA vendors in SEFUW 2018:







• Tool vendors in SEFUW 2018:











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Agenda (1/3)



https://indico.esa.int/indico/event/232/timetable/#all.detailed

The agenda has been distributed among the participants

	■ indico.esa.int/indico/event/232/timetable/#all.detailed	
SEFUW: SpacE FPGA	Users Workshop, 4th Edition	
9-11 April 2018 European Space Research and Tecl Europe/Amsterdam timezone	nnology Centre (ESTEC)	
SEFUW 2018	09/04 Tue 10/04 Wed 11/04 All days	>
Call for Abstracts		ed view Filter
	Demo Session and C Design Flow FPGA Vendors FPGAs: High Perform	x see more
Registration Form	n 9/4	
Venue and Practical Information 09:00 Past and Related Events		
For information please	Registration and Early Morning Networking Break sponsored by COMET by CNE Systems and Microelectronics Division	S and ESA's Data
write to	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	09:30 - 10:00
Sefuw@esa.int 10:00	Welcome	Mr. David DANGLA et al.
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:00 - 10:30
	FPGA experience and SoC design methodology at Airbus Defence & Space.	Mr. Ottmar RIED
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:30 - 10:50
	Jena-Optronik Experience Summary on Microsemi RTG4 designs	Johannes BOTH
11:00	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:50 - 11:10
	SpaceFibre, Spectrometer and Camera: Some applications on the RTG4 FPGA	Prof. Steve PARKES
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	11:10 - 11:30
	UVVM - Universal VHDL Verification Methodology. Setting a standard for VHDL testbenches	Mr. Espen TALLAKSEN
12:00	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	11:30 - 12:10
	Multiple-clock Domain FPGA Designs: Challenges and Solutions	Dr. Reuven DOBKIN 🛅
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	12:10 - 12:35

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Agenda (2/3)



https://indico.esa.int/indico/event/232/overview

	Indico.esa.int/indico/event/232/overview	
write to Sefuw@esa.int	 trends of FPGA usage in space applications reconfigurable systems lessons learned: ensuring successful and safe use of FPGA in space applications choosing the best FPGA type for our space application 	
	 - encoding the best FFGA type for our space application - export license limitations / changes / ITAR / EAR - package and assembly challenges - companion non-volatile memory (when required) experience 	
	The main FPGA vendors will present updates and will be available for questions. The detailed agenda will we published closer to the event. Presentations from at least the major design groups (Large System Integrators) are expected.	
SEFUW 2018	Have you not been contacted yet to present and are you interested in presenting?: Please contact us and/or submit your abstract. Do you need space for demonstrating hardware and/or a booth? Please contact us.	
Books of Abstracts :	The workshop duration will be 3 days. Attendance to the workshop is free of charge.	
- available online	It is advised to register as soon as possible in order to ensure your place. Registration is required via the website not later than 30 March 2018.	
- Printed copies at the	The materials presented at the workshop are intended to be published on this website after the event. All material presented at the workshop must, before submission, be cleared of any restrictions	
Registration Desk	preventing it from being published on the website.	



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Agenda (3/3)

Sessions

- FPGA Vendors
- Tools Vendors
- Design Flow
- Fault Tolerant Methodologies and tools
- Radiation
- Reconfiguration
- High Performance
- Industrial experiences
- Demo session



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Monday 9-April-2018 (1/3)



	Registration and Early Morning Networking Break sponsored by COMET by CNES Systems and Microelectronics Division	S and ESA's Data	
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	09:30 - 10:00	
10:00	Welcome	Mr. David DANGLA et al.	
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:00 - 10:30	Session
	FPGA experience and SoC design methodology at Airbus Defence & Space.	Mr. Ottmar RIED	Industrial
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:30 - 10:50	Experiences
	Jena-Optronik Experience Summary on Microsemi RTG4 designs	Johannes BOTH	(David
11:00	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:50 - 11:10	Dangla)
	SpaceFibre, Spectrometer and Camera: Some applications on the RTG4 FPGA	Prof. Steve PARKES 🗎	
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	11:10 - 11:30	
	UVVM - Universal VHDL Verification Methodology. Setting a standard for VHDL testbenches	Mr. Espen TALLAKSEN	Design Flow
12:00	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	11:30 - 12:10	(David Merodio)

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Monday 9-April-2018 (2/3)



Session

	Multiple-clock Domain FPGA Designs: Challenges and Solutions	Dr. Reuven DOBKIN 🗎
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	12:10 - 12:35
	RTL Analysis and CDC Analysis for Maximum Design Efficiency and Quality	Mr. Scott CALKINS 🗎
	Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	12:35 - 13:00
13:00	Networking Luncheon	
	ESTEC Canteen	13:00 - 14:00
14:00	ESTEC Canteen Build and Debug Highly Reliably FPGA-based Designs	13:00 - 14:00 Mr. Philipp JACOBSOHN 🛅
14:00		
14:00	Build and Debug Highly Reliably FPGA-based Designs	Mr. Philipp JACOBSOHN 🗎
14:00	Build and Debug Highly Reliably FPGA-based Designs Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	Mr. Philipp JACOBSOHN 🛅 14:00 - 14:25
14:00	Build and Debug Highly Reliably FPGA-based Designs Newton 1 and 2, European Space Research and Technology Centre (ESTEC) Advanced Verification for FPGAs	Mr. Philipp JACOBSOHN 14:00 - 14:25 Mr. Simone CATENACCI

Tool Vendors Florent Manni

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Monday 9-April-2018 (3/3)



Evaluation of MATLAB/Simulink and RTL VHDL HDL environment	Mr. Klemen BRAVHAR et al.
Newton 1 and 2, European Space Research and Technology Centre (ESTEC,	C) 15:10 - 15:30
FUSIO RT: A New Space Modular Computer Core based on Nanoxplo Medium FPGA	ore NG- Mr. Pierre-Xiao WANG et al.
Analysis and Mitigation of Single Event Upsets in Configuration Men Kintex7 SRAM-based FPGA	mory of Xilinx Dr. BOYANG DU
Fault injection for space: FT-Unshades2 updates, experiences and roadmap	Prof. Hipólito GUZMÁN-MIRANDA 🛅
Networking Coffee Break sponsored by COMET by CNES and ESA's D Division	Data Systems and Microelectronics
Newton 1 and 2, European Space Research and Technology Centre (ESTEC,	C) 16:30 - 17:00
Demo Session and Cocktail Reception sponsored by COMET by CNES Microelectronics Division	S and ESA's Data Systems and
Mr. David Dangla, Mr. David Merodio Codinachs	

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Organization notes



• Presenters:

- Provide the presentations:
 - Preferably by the day before your presentation
 - Preferably using the Indico system (online)
 - Alternatively during the breaks or have your laptop ready.

• All attendees, transportation:

- Taxi and Shuttle options
- Check the "SEFUW 2018 Book of Abstracts"

http://www.esa.int/About_Us/ESTEC/Transport_to_and_from_ESTEC

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Organization notes



- Round Table (Tue 10 at 17:30):
 - Initial topics:
 - New space and COTS: risks and advantages
 - More complex FPGAs for Space: are all teams ready to manage them?
 - High-performance: FPGAs enabling acceleration and new application.
 - Re-configurability: relatively new for space.
 - High Level Languages: pros and cons, experiences
 - To all:
 - Would you like to provide written feedback?
 - PowerPoint Slide/s, text, ...
 - Do you have more topics to propose?
 - Send an email to <u>david.merodio.codinachs@esa.int</u>

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Useful Information



- Networking Coffee Break sponsored by COMET by CNES and ESA's Data System and Microelectronics Division (TEC-ED)
- Networking Luncheon at ESTEC main canteen
- Wireless access:
 - Login and password included at the back of your visitor badge.
 Valid throughout the workshop

SSID: **esa-public** Authentication: Open **Username**: *d.merodiocodinachs* **Password**: *xxxxx*

If your badge does NOT include this information, please report to the Registration Desk

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Optional Social Dinner

Restaurant: ESTEC Canteen

Date: 10-April-2018 At 6:45pm Price: 50 EUR

The price includes a small plates menu served buffet-style and a drink arrangement.

MENU

Selection of Starters * * Selection of Main courses * * Dessert Buffet





Example Menu 1

Starters * *

Marinated Salmon Green salad with dressing Quinoa salad with grilled Tofu Bread & Butter

> Main course * *

Salmon with wine sauce Grilled veal steak with mustard tarragon sauce Tomato with Quinoa and Ratatouille Potato cakes Courgette and eggplant gratin

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ENJOY THE WORKSHOP !!!