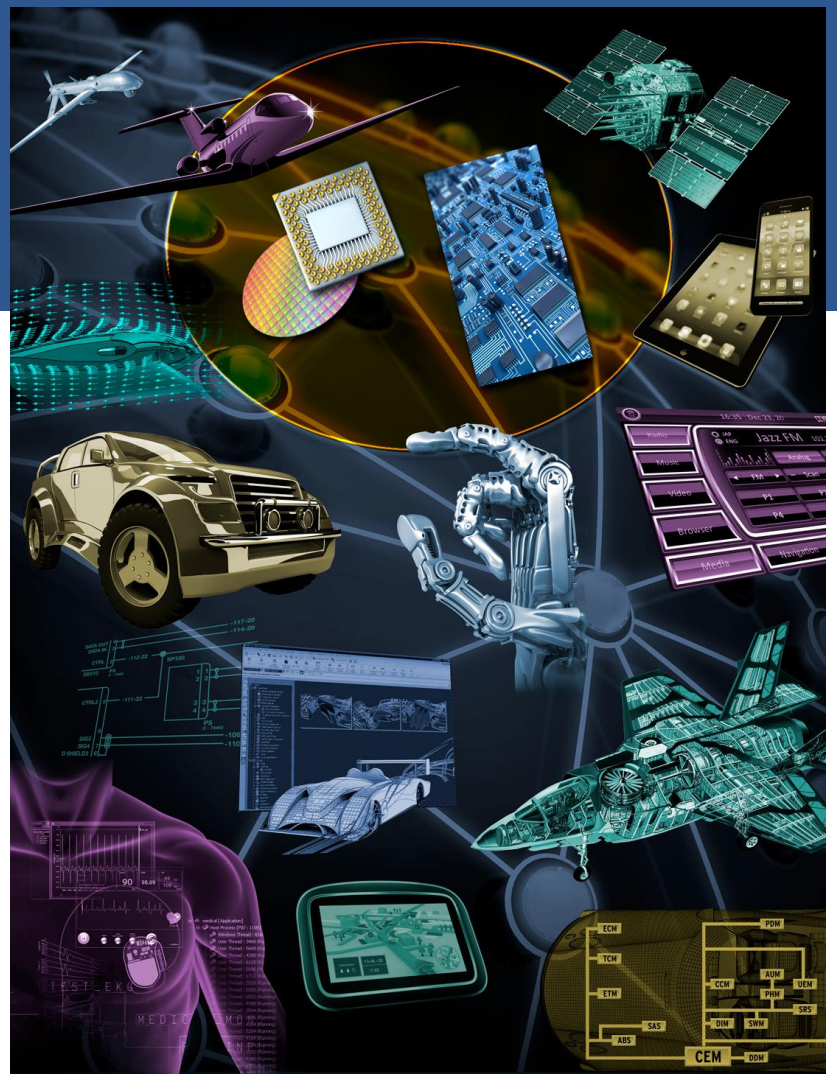

Advanced Verification for FPGAs

Simone Catenacci

Application Engineer

IC Verification Solutions

April 9, 2018

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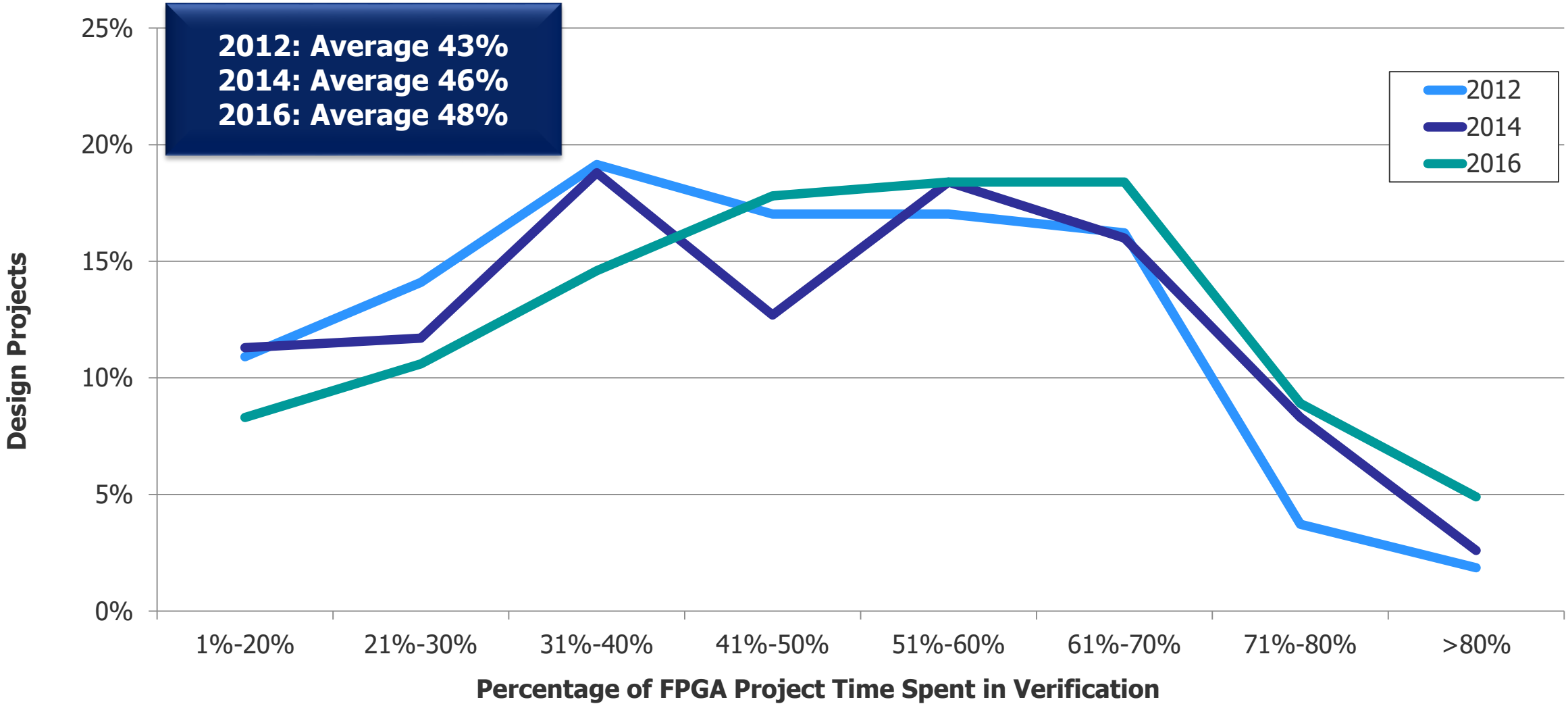
Agenda

- Industry Trends and Challenges for FPGA Development
- Staying competitive with Advanced Verification
- Final Thoughts

INDUSTRY TRENDS AND CHALLENGES FOR FPGA DEVELOPMENT

FPGA Verification Project Time

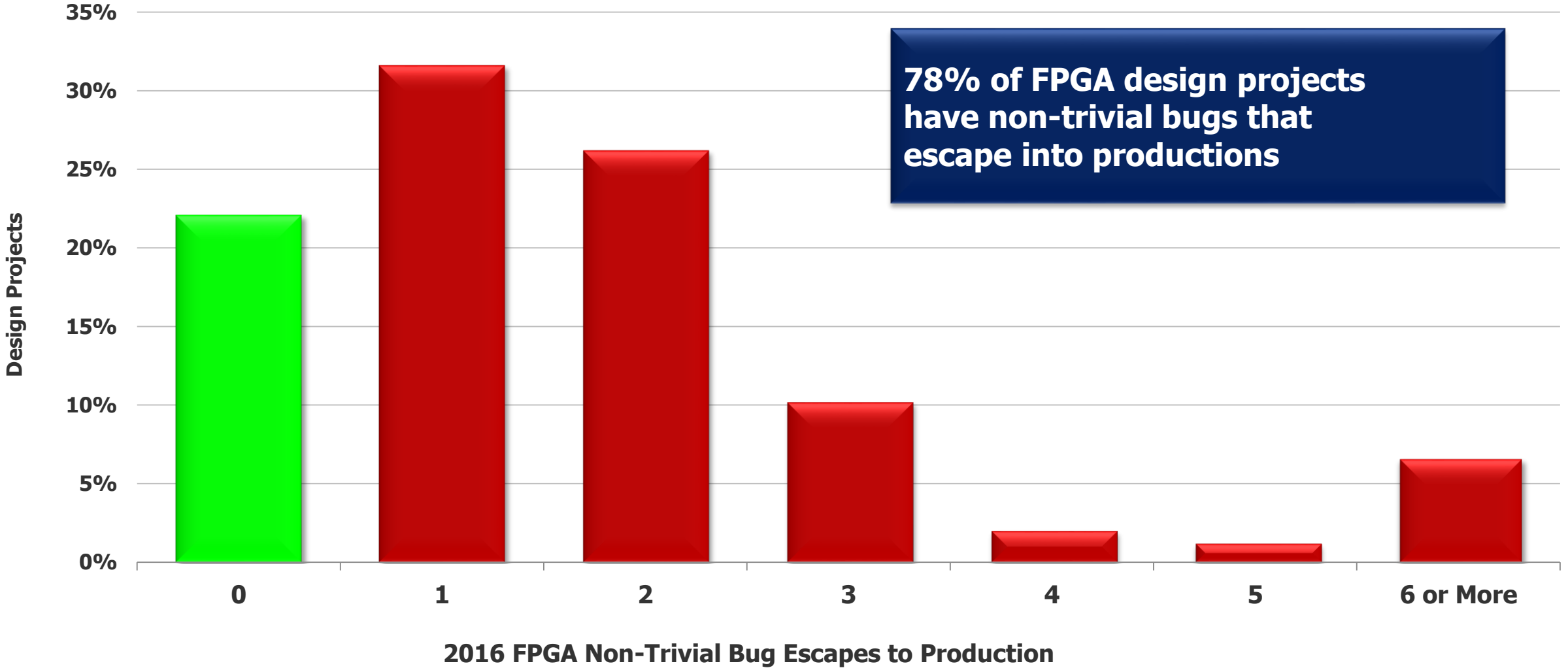
FPGA verification consumes majority of project time



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Number of FPGA Bug Escapes to Production

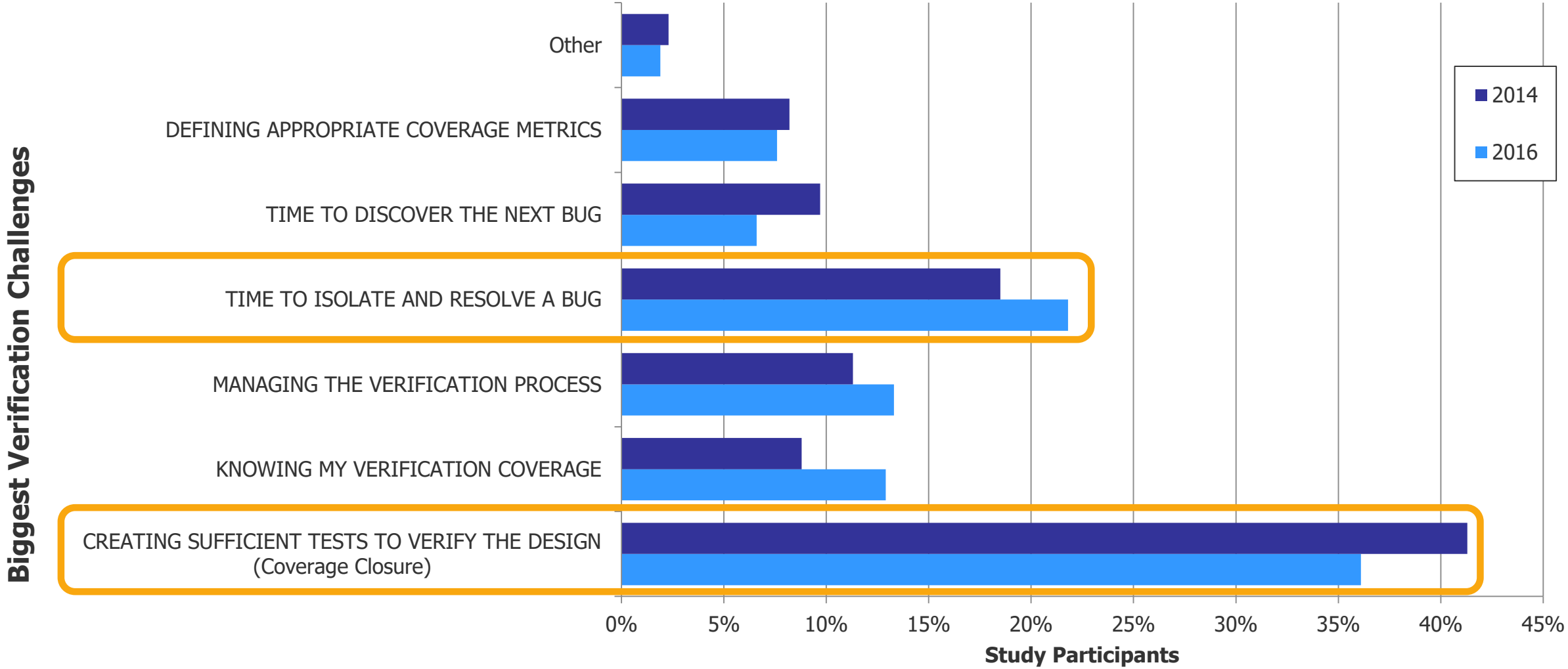
Bugs found late in the development cycle are exponentially more expensive



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Biggest FPGA Verification Challenges

Sufficient testing and improving debug efficiency are the biggest challenges



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

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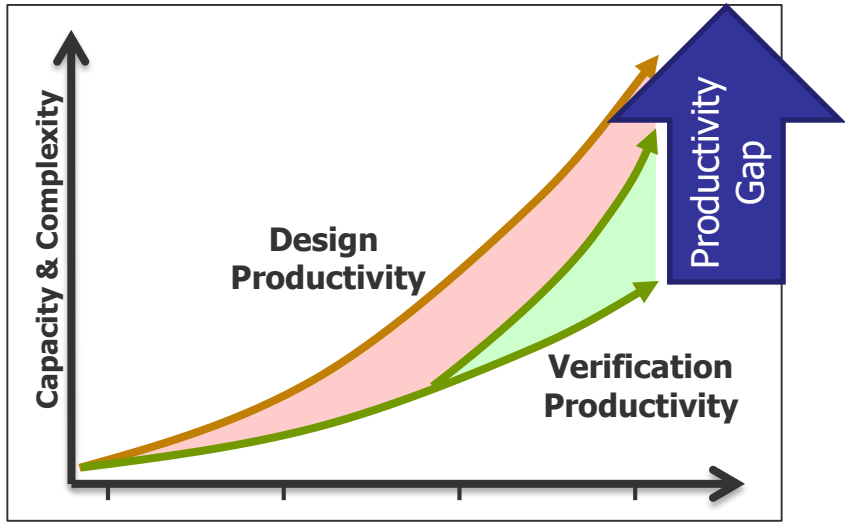
FPGA Productivity Gap

Verification must evolve to keep pace with design innovations

- FPGA vendors continue with design innovations
  - Hardened blocks – Reuse
  - IP - Reuse
  - SOC – Reuse
  - Graphical system builders - Automation
  - HLS – Abstraction



- "Design Productivity" alone ≠ faster "Time to Market"
  - Designs must also work and be of high quality to gain adoption
  - TTM depends on maximizing design and verification productivity

- Verification must similarly evolve to keep pace
  - Maximize reuse
  - Improve automation
  - Raise the level of abstraction

STAYING COMPETITIVE WITH ADVANCED VERIFICATION

How Do You Improve Verification Productivity?

Reuse, automation and abstraction to the rescue

Maximize Reuse

- Reuse test environments from project to project
- Minimizes time spent developing TB environments
- Minimizes TB debug time
- VIP for bus protocols & memory models

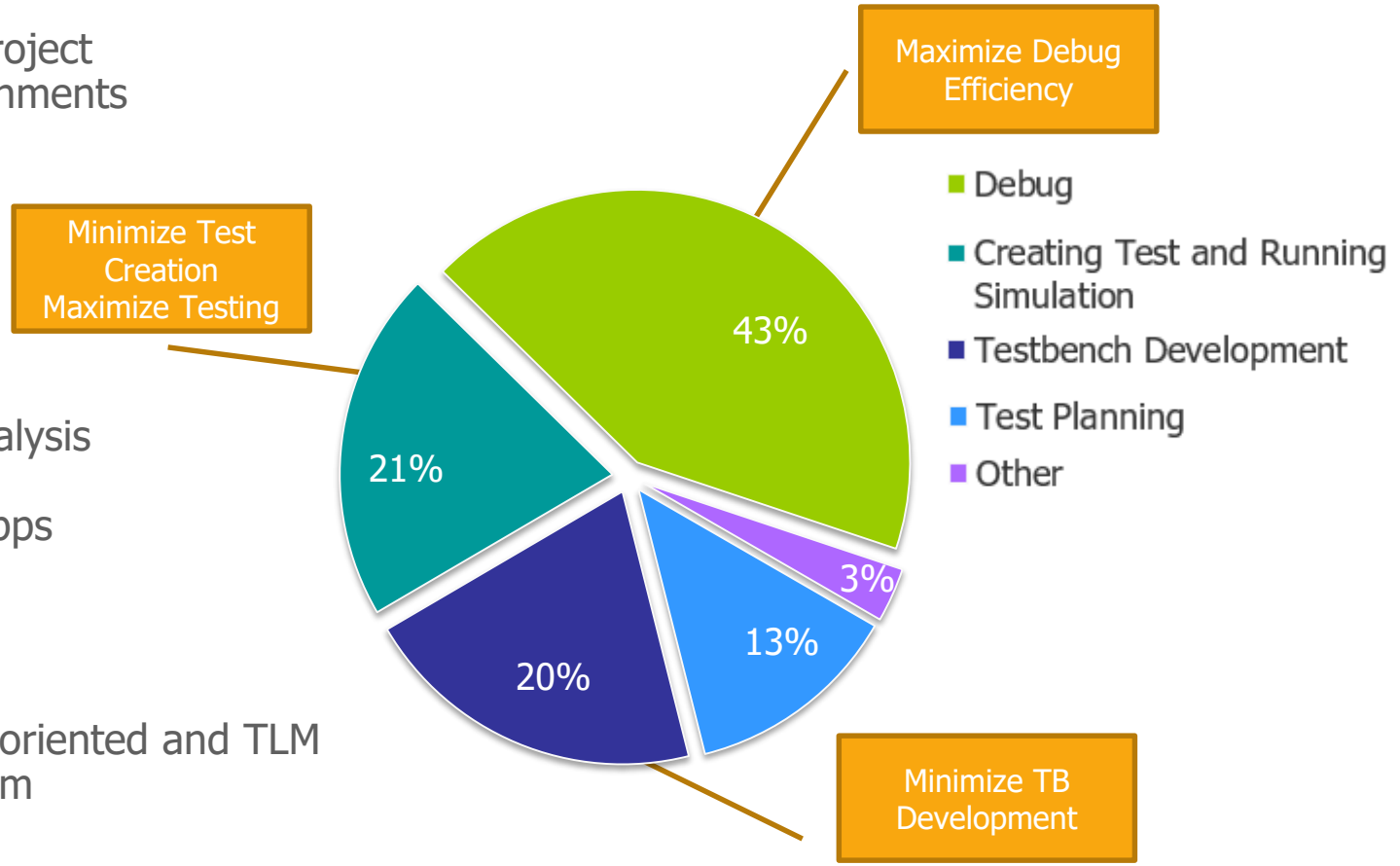
Improve Automation

- Automate TB creation
- Automate regressions
- Automate results/metrics collection and analysis
- Automatic testing with Formal Apps
- Accelerate coverage closure with Formal Apps
- Automate requirements tracing

Raise Abstraction Level

- Improve TB creation efficiency with object oriented and TLM
- Write tests at scenario level to match system
- Debug at a higher level than pin wiggles

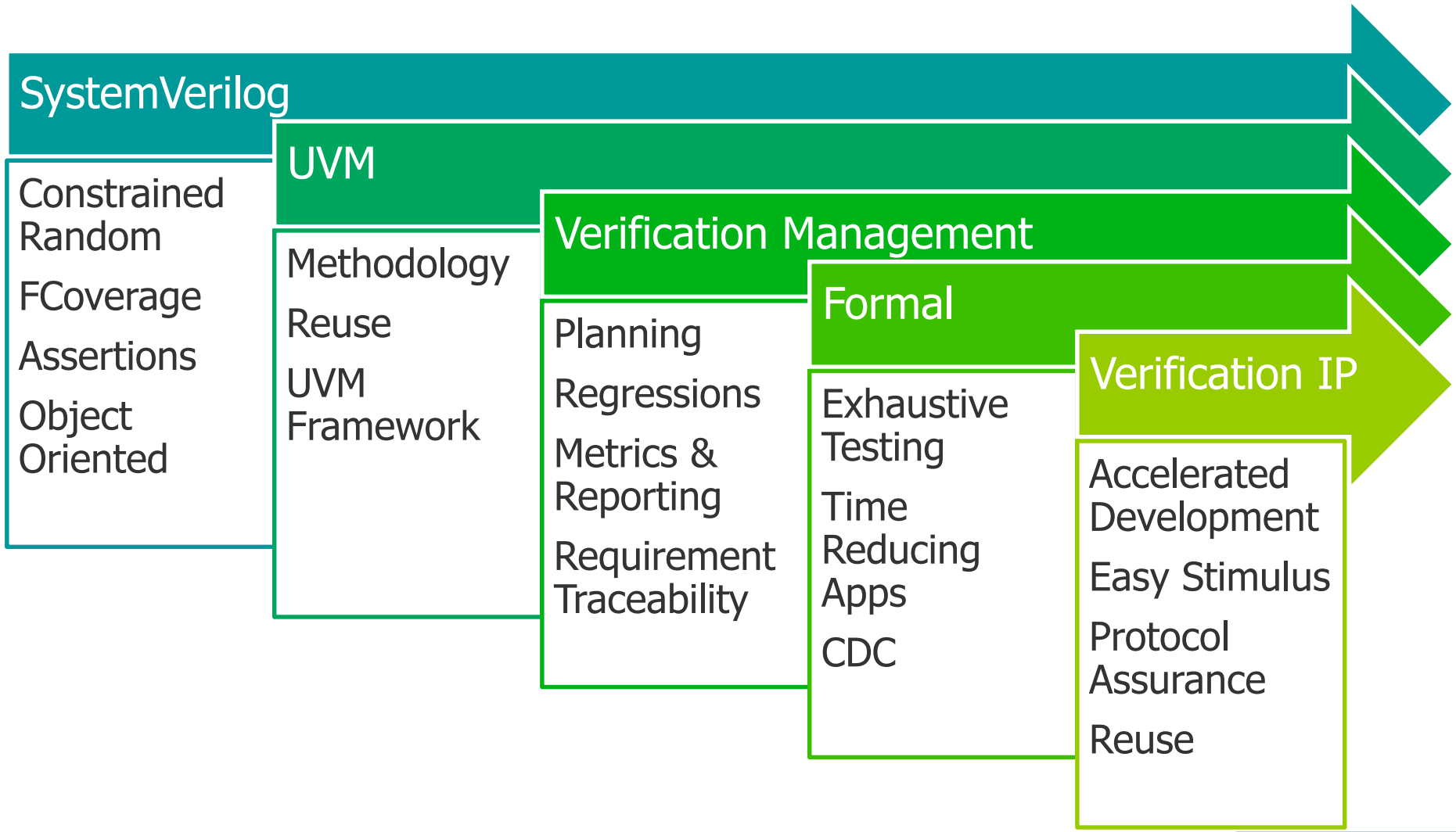
Where do spend your time for FPGA verification?



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Improving with Advanced Verification

From the lab to the modern age for better quality and productivity



Advantages

- More testing
- Improved quality
- Find bugs early
- Greater insight
- Faster debug
- Greater reuse
- Shorter cycles
- Schedule predictability

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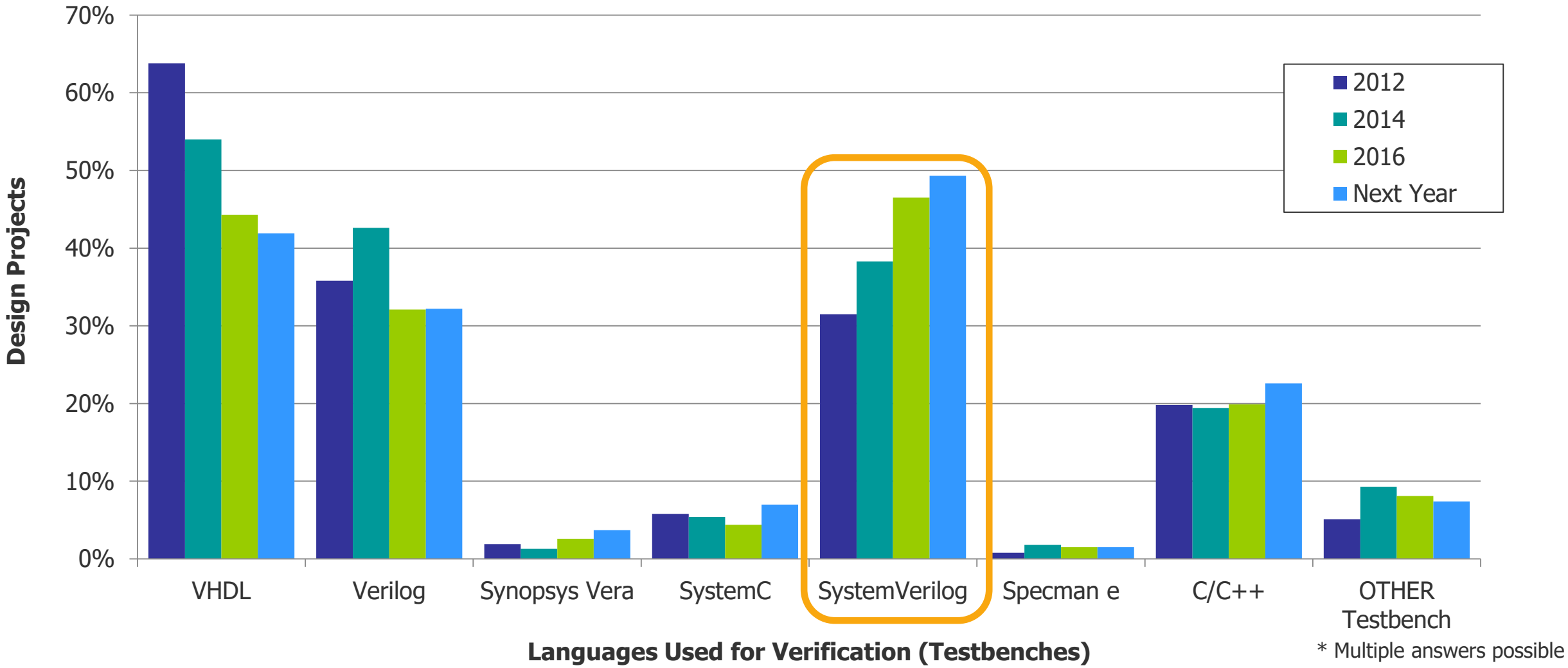
FPGA Verification Language Adoption Trends

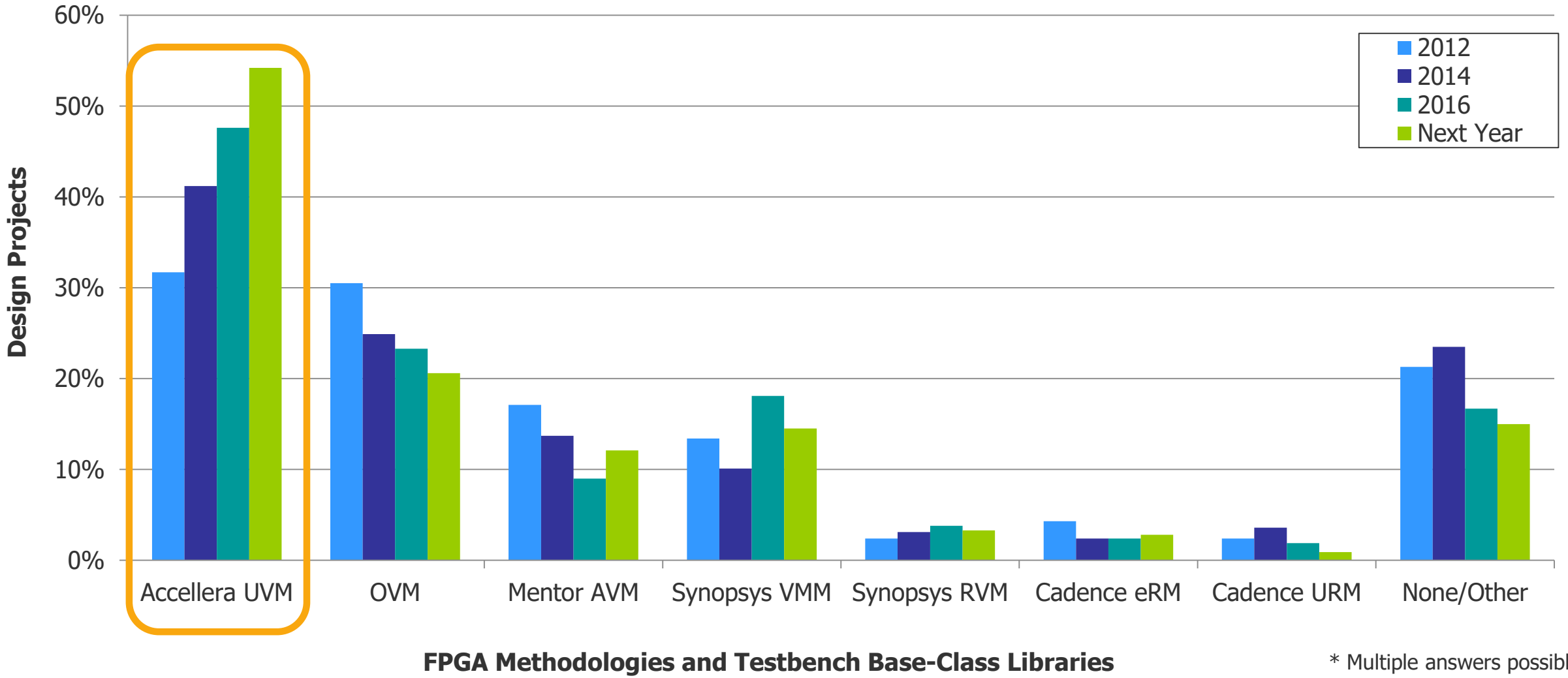
SystemVerilog is now the leading FPGA verification language



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

FPGA Testbench Methodology Adoption Trends

UVM is the clear leader in FPGA testbench methodologies

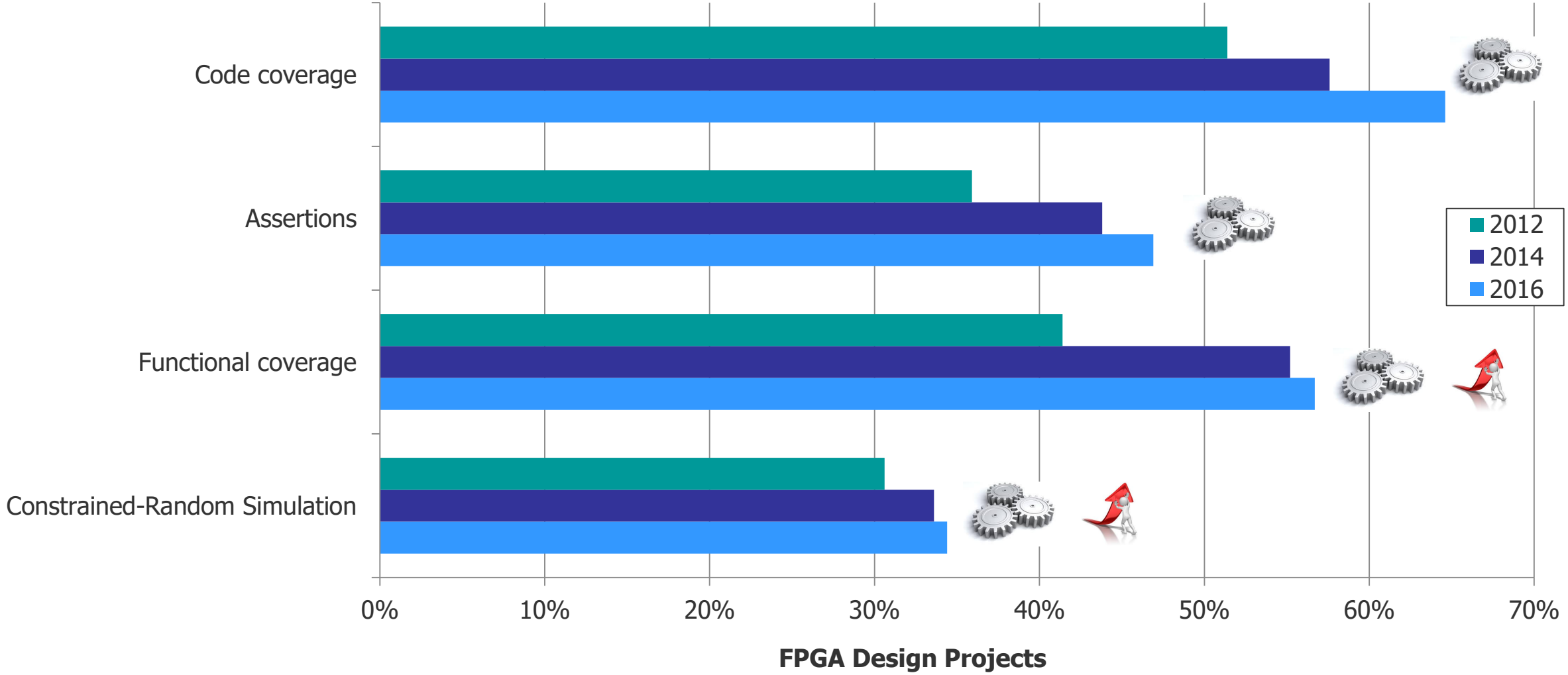


* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

FPGA Dynamic Verification Adoption Trends

Adoption of advanced verification techniques continue to grow for FPGA verification

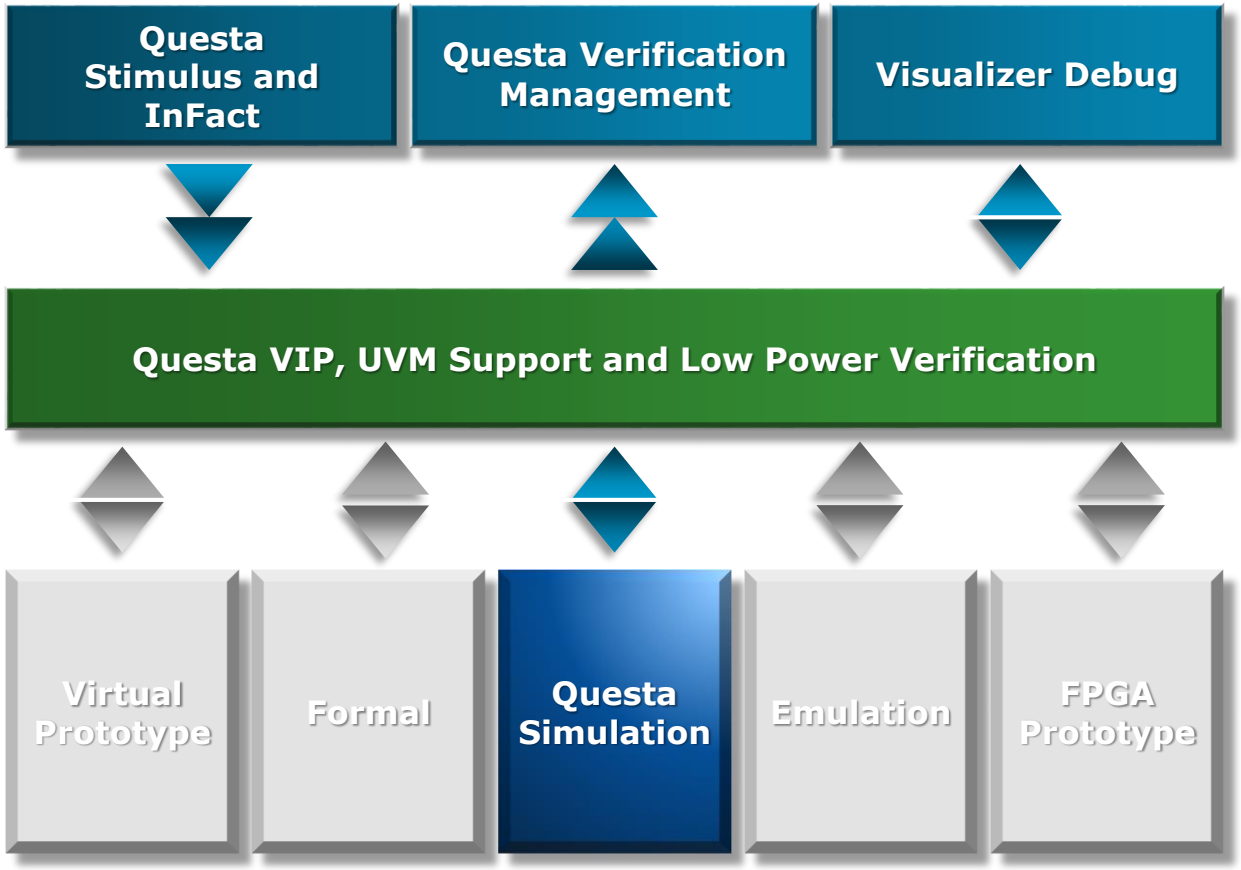


Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

Questa Simulation

Verification Productivity with High Performance Simulation at its Core

- Complete Solution with Mentor Enterprise Verification Platform
- Most Comprehensive Support of Methodologies for Increased Verification Productivity
  - Assertion-Based Verification
  - SV-UVM
  - Coverage/Plan Driven Verification
  - Regression Creation and Management
  - Test Bench Automation



Mentor UVM Framework (UVMF) for Easier UVM

Making the transition to UVM possible

UVM Jumpstart

- Immediately productive while learning UVM
- Layer on top of UVM that hides UVM details
- Allows team to focus on verifying product features
- Promotes reuse increasing productivity

UVM Testbench Generators

- Code generators to create a UVM testbench in minutes
- Saves 3-4 weeks of effort on every project
- UVMF is open source and no cost – Delivered in Questa

Helped over 40 companies adopt UVM

- 75% are FPGA customers
- Over half are in mil-aero industry
- Majority use VHDL for design and have no SystemVerilog experience

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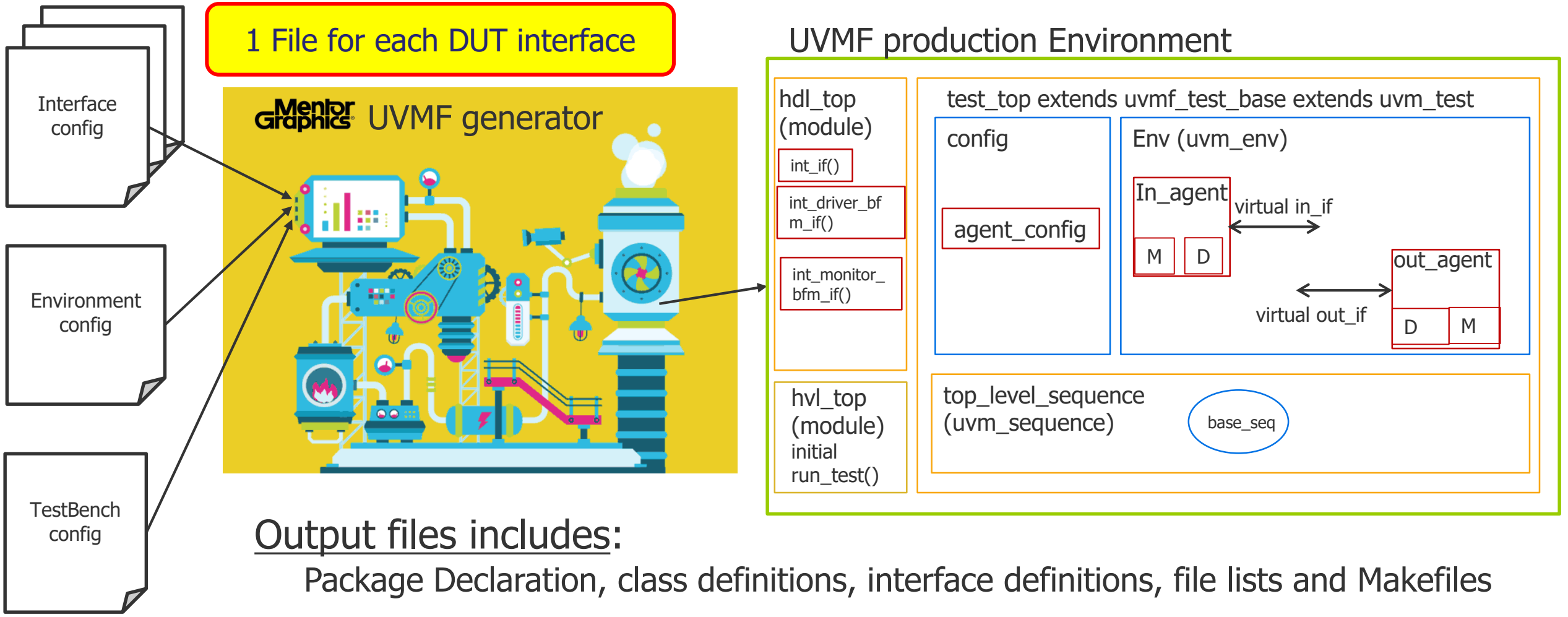
UVMF-Generator Flow

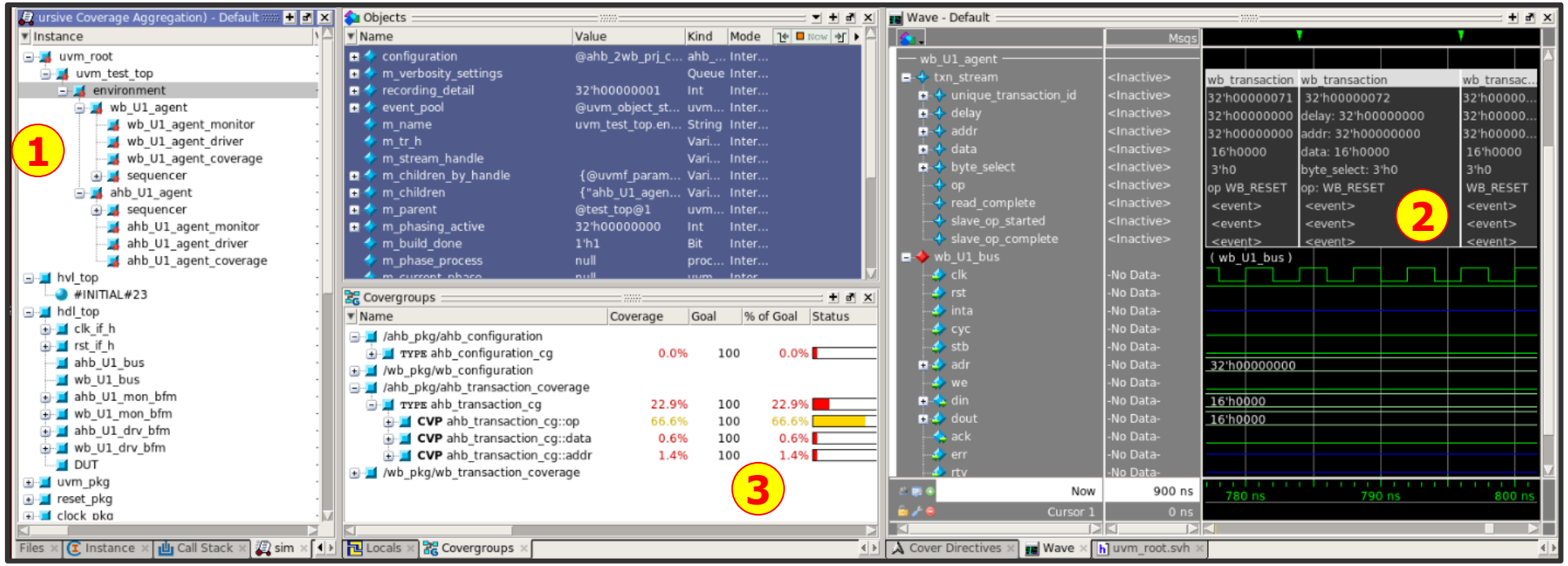


Output files includes:

Package Declaration, class definitions, interface definitions, file lists and Makefiles

Working Simulation Out Of The Box

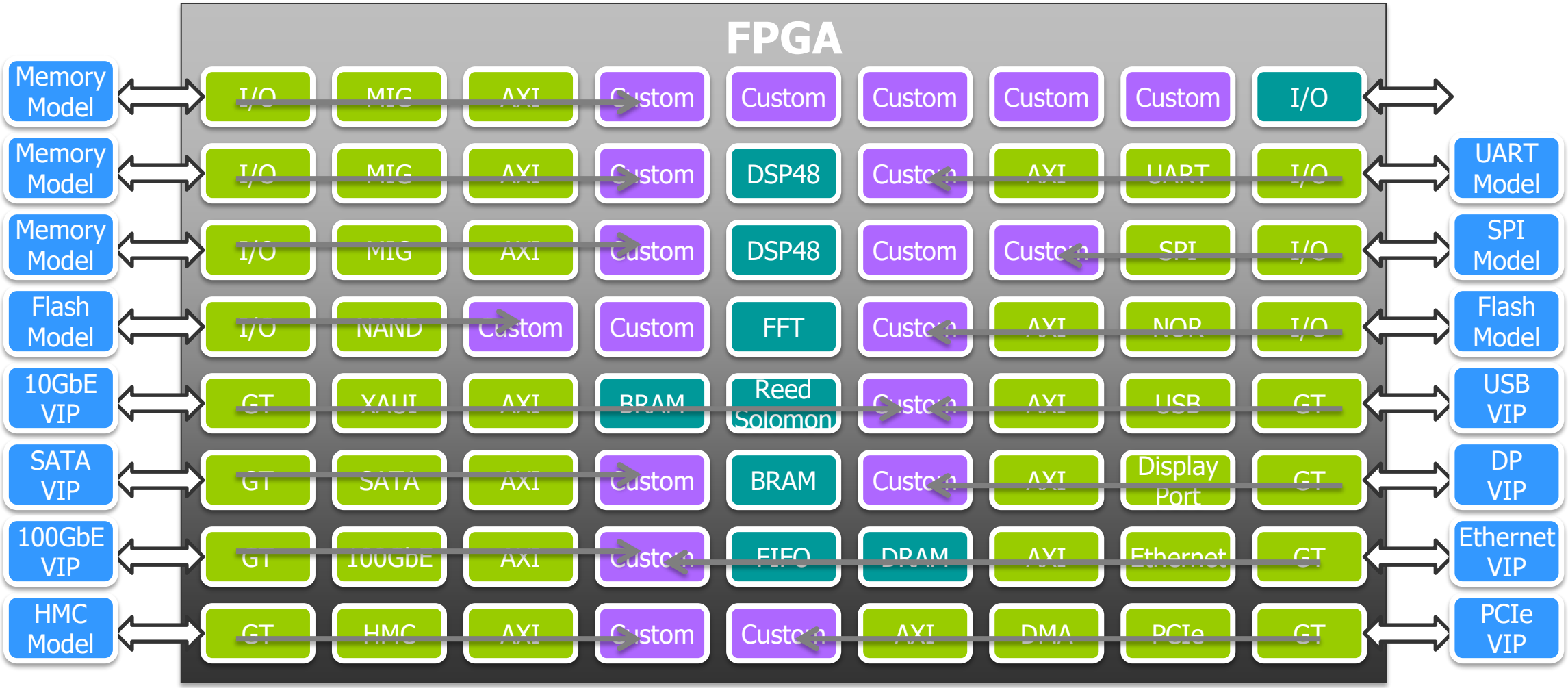
- 'make debug' to bring up interactive simulation



1. Complete Dual Top UVM environment compiles & simulates
2. Monitor transactions automatically added to the wave window
3. Covergroups automatically created and collect coverage

Verification IP Enables Rapid Testbench Development

Enabling verification of your custom application without deep protocol expertise or effort



Verification IP: Off The Shelf Protocol Test Environments

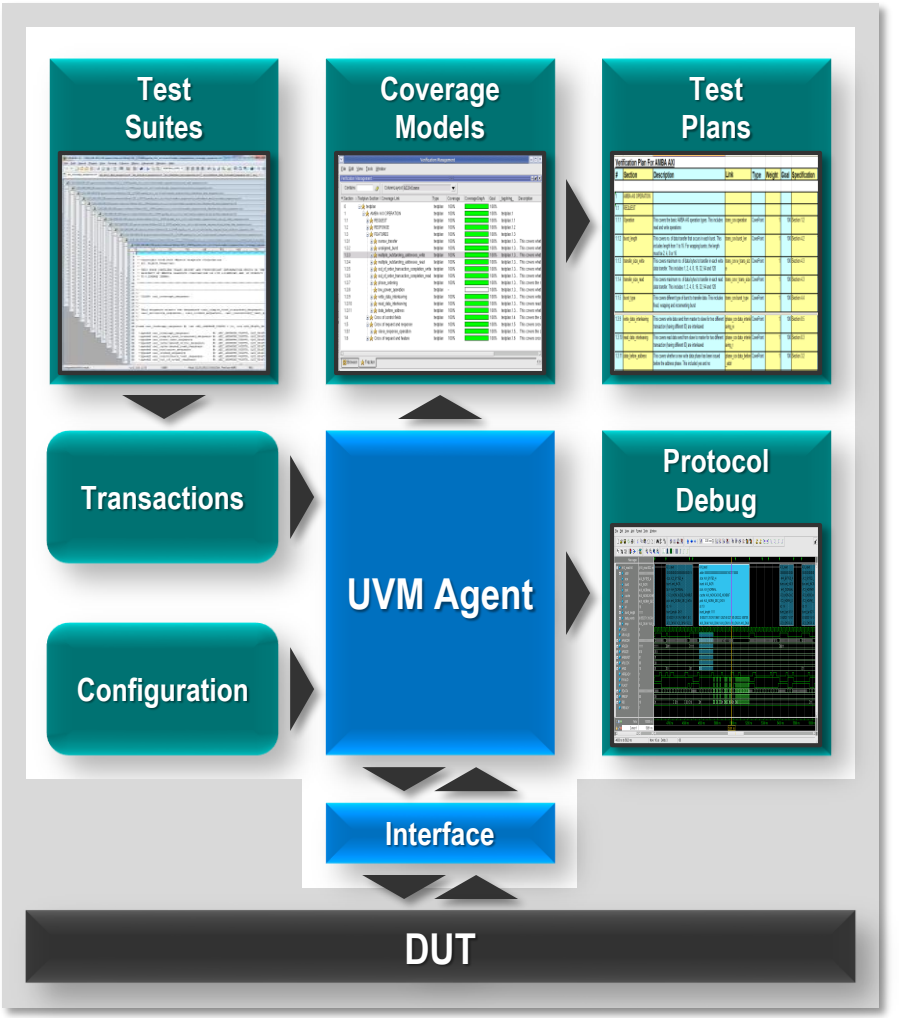
"Protocol Expertise" Reduces Time, Effort & Risk for IP Centric Designs

- What is Verification IP?
  - Reusable test environments
  - Built around standard protocols

- Reduces Verification Effort
  - Provides completed TB at standard interfaces
  - Provides functionality to create and run tests
  - Less time creating TB and more time testing

- Eliminates Protocol Expertise
  - Deep protocol knowledge not needed for TB creation
  - Provides out of the box protocol stimulus and checking
  - Enhanced debug productivity with transactions and assertions

- VIP Reduces Risk
  - Re-usable VIP building blocks
  - Common design architectures & protocols
  - Complete protocol assurance



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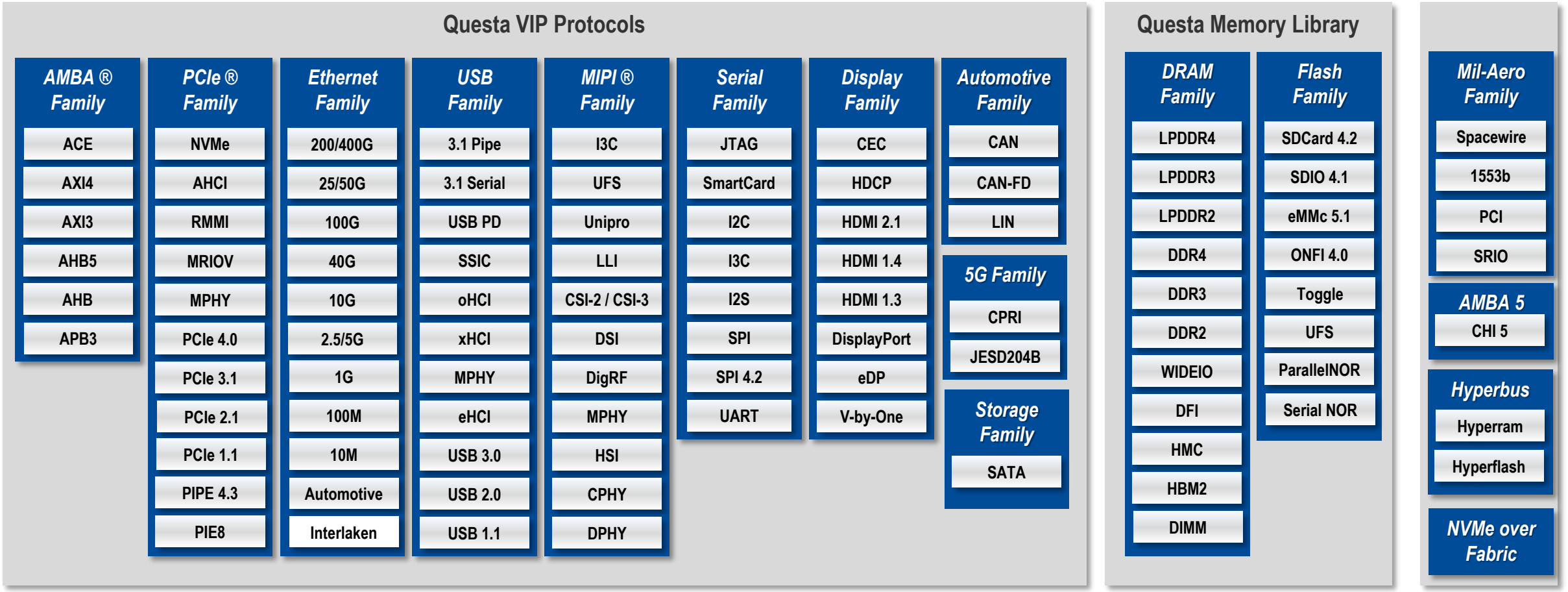
A Complete VIP Solution for FPGA Designs

Mentor Graphics Questa Verification IP Library



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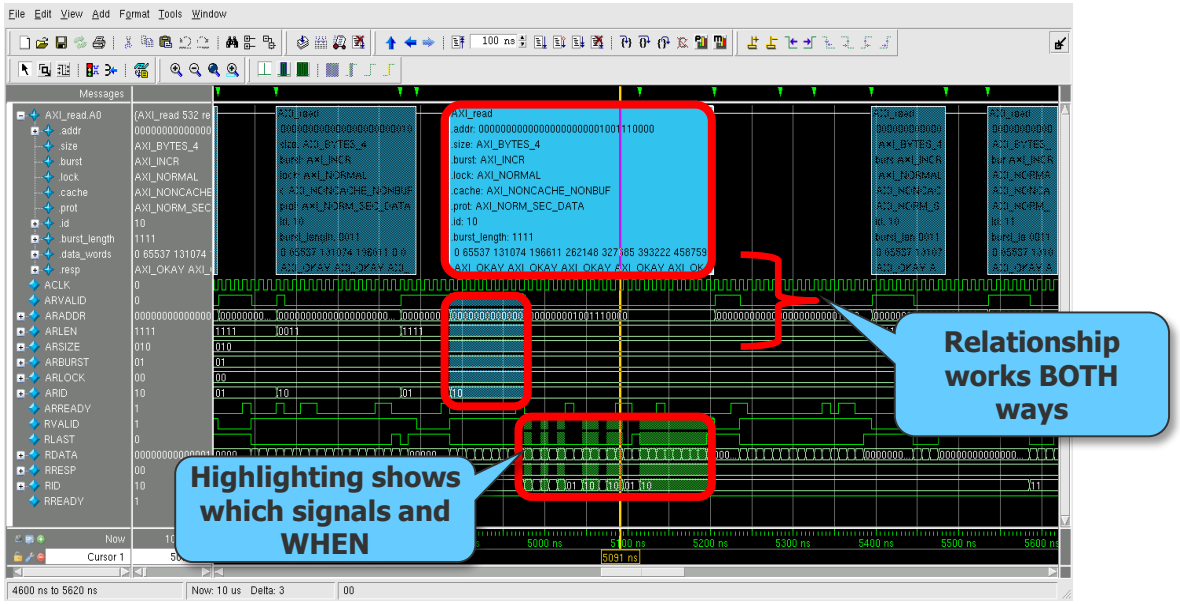
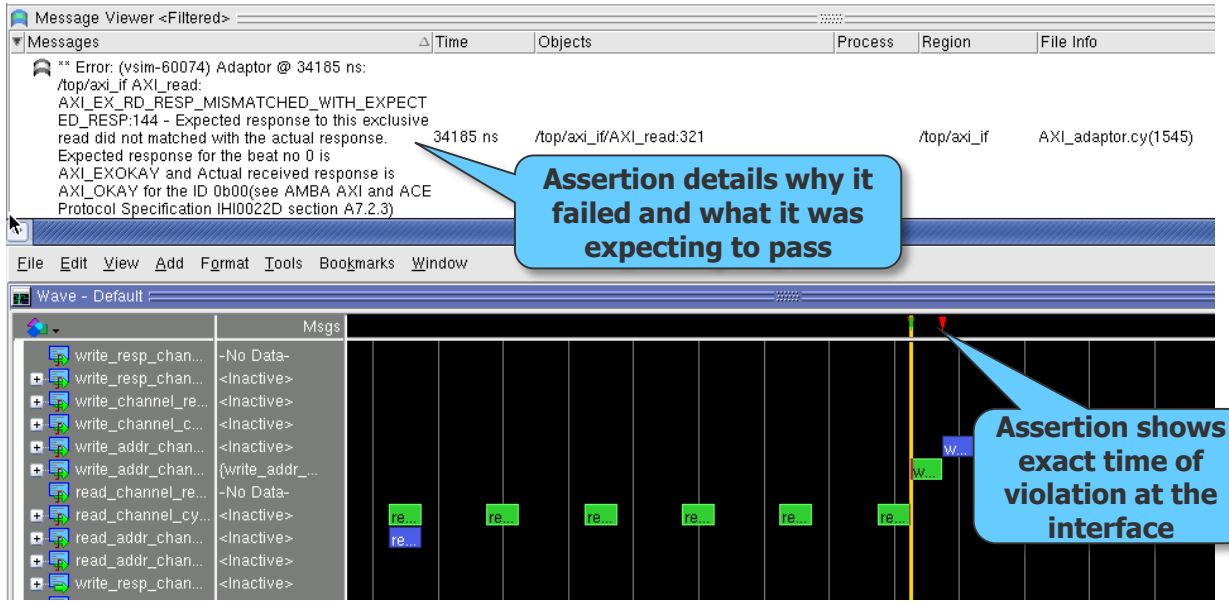
Debug Faster with Questa Verification IP

QVIP Improves debug abstraction and automation to boost productivity

- Transaction recording
  - Debug at a higher level with integrated transactions
  - Quickly understand and analyze bus activity
  - Automatically links transactions to signals

- Protocol assertions
  - Integrated assertions automate protocol checking
  - Protocol assertions immediately pinpoint source of failure
  - Quickly understand integration of your design with IP





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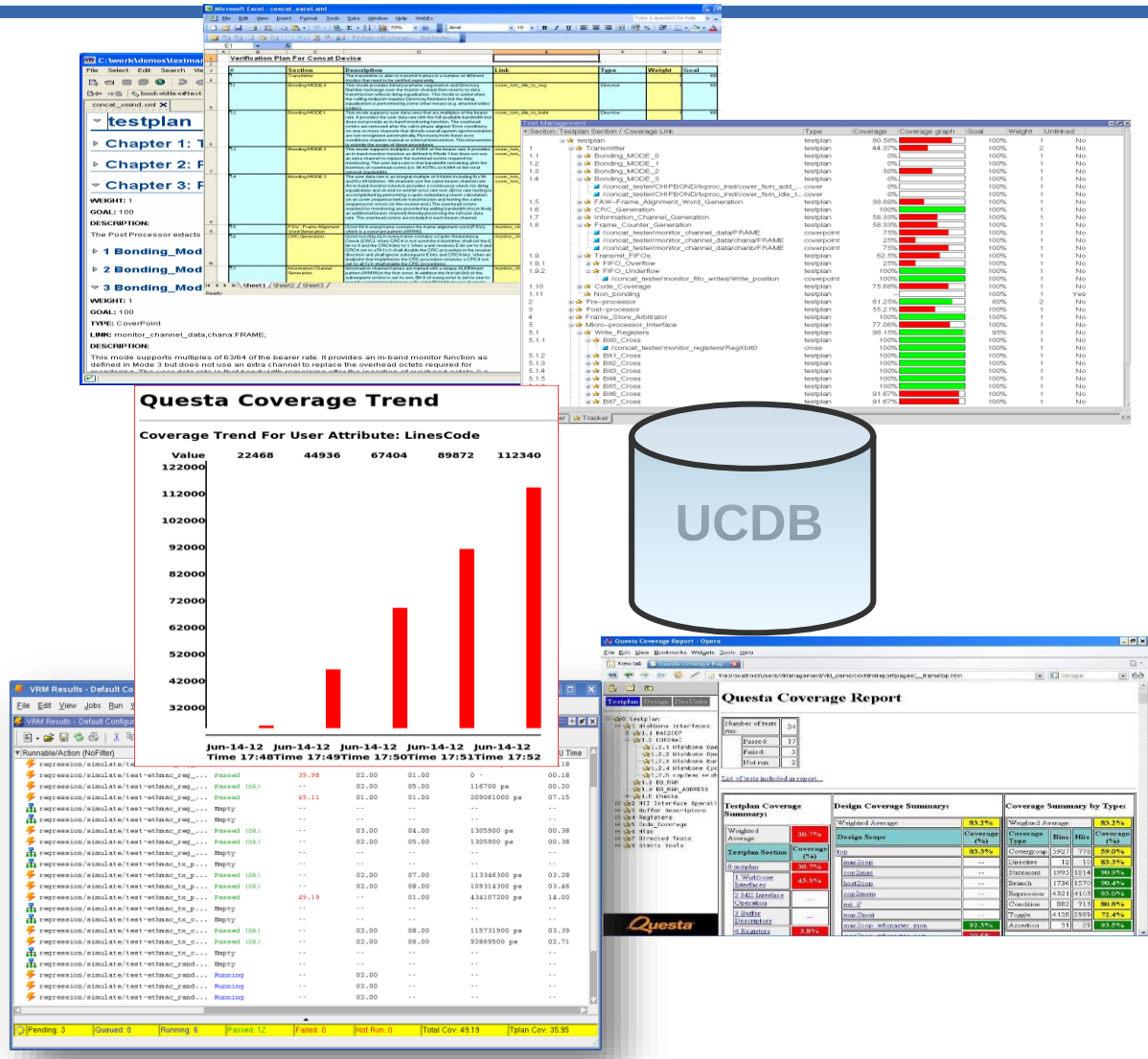
Questa Verification Management

Productivity in Tool Execution, Data Management, Analysis and Tracking

- Test Plan Tracking
  - Lifts the lid on simulation, formal, CDC
  - See progress day by day
  - Have I done enough testing?
  - Am I ready to freeze the RTL?
- Trend Metrics
  - Monitor progress throughout the project
  - Mitigate verification risks
  - Help improve future project timescale estimations
- Results Analysis
  - Quickly Identify and Organize Results
  - Improve debug turn-around time
- Verification Run Manager
  - Automate all regression tasks and reporting
  - One interface to control all



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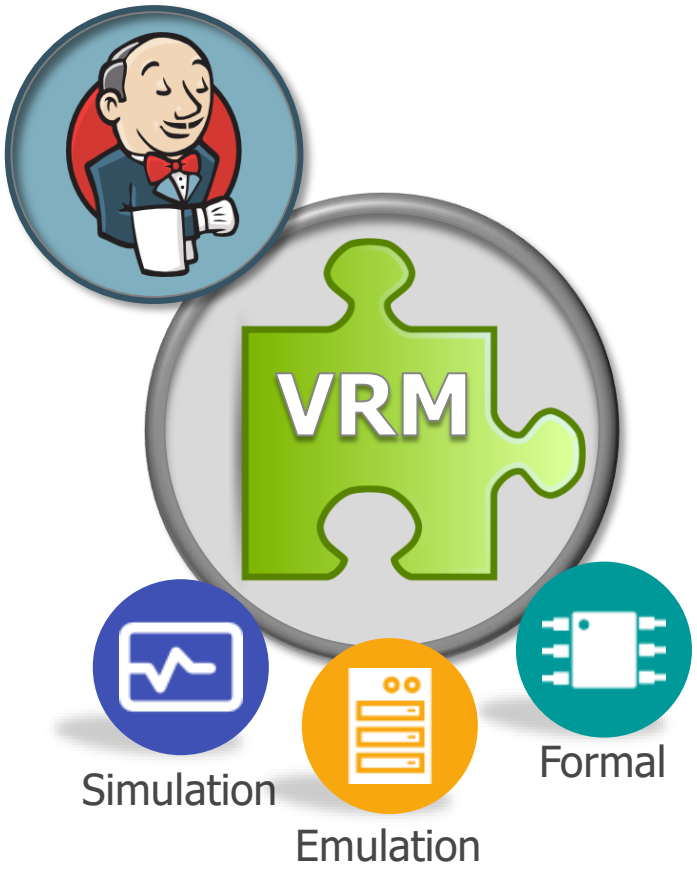
Jenkins & Questa Verification Run Management

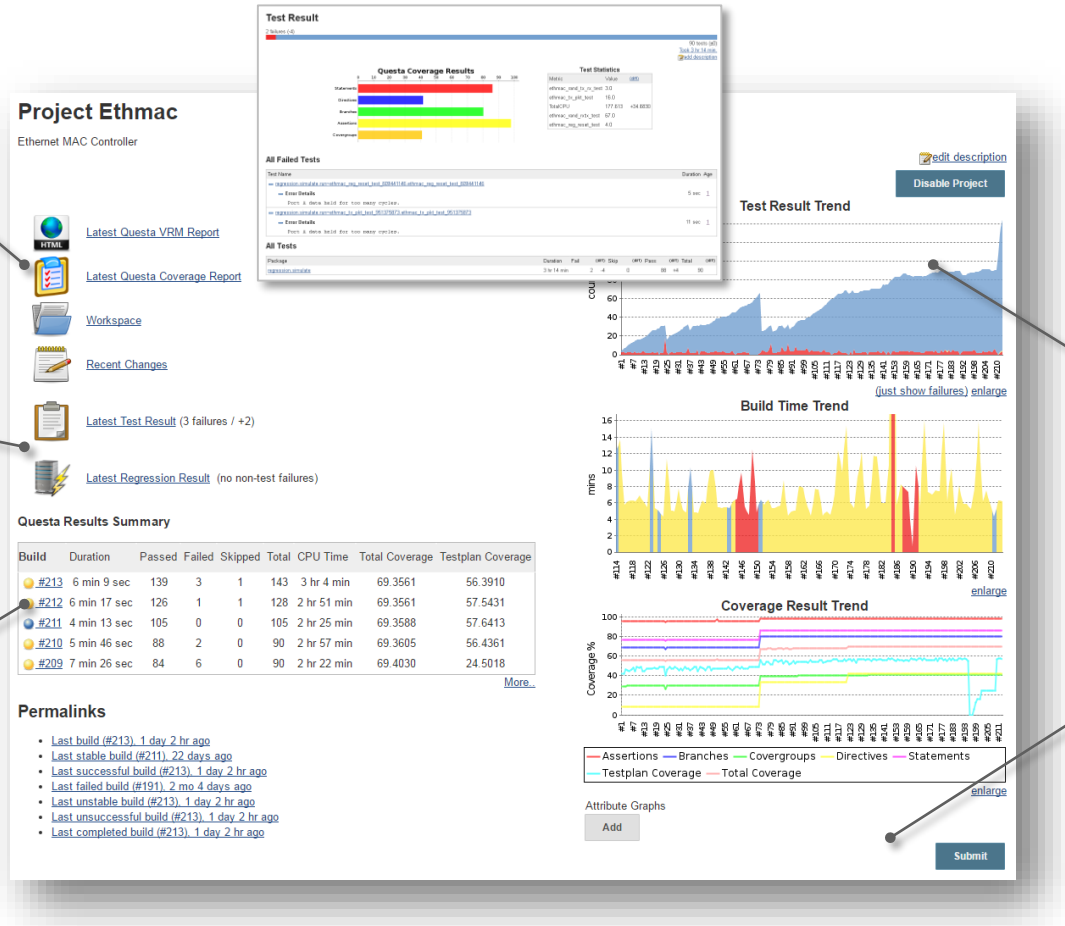
Continuous integration and reporting for advanced regressions management



HTML Reports
VRM & Coverage

Test Results
Native Jenkins
Full Questa VRM

Build Summary
Expandable



Trend Graphs
Test results
Build times
Coverage code/functional

Custom Trends
Any user attribute

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FINAL THOUGHTS

Proven Benefits from Advanced Verification

FPGA customers realize the benefits of evolving their verification methodologies

SystemVerilog UVM/UVMF

- Constrained random for better testing
- Functional coverage for better insight
- Consistent methodology
- Promotes Reuse

Verification IP

- Protocol expertise
- Reduces TB development effort
- Risk reduction

Formal

- Find bugs at design time
- Identify unreachable code
- Exhaustive testing

FPGA Customer Success Stories

- Increased business due to shorter design cycles
- 400% ROI after adopting UVM and VIP
- 5 straight FPGA's without a bug
- Zero bugs found in lab since moving to UVM
- 3x Speed up verification cycle with Formal Apps
- Higher quality code

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Where Can You Go To Learn More?

- Verification Academy
  - https://verificationacademy.com/
  - Most comprehensive verification resource in industry
  - Free online courses, verification cookbooks, discussion forums
  - More than 40,000 members

- Functional Verification at www.mentor.com
  - https://www.mentor.com/products/fv/
  - Learn more about tools to enable methodologies
  - Simulation, SV/UVM, Formal, Verification IP
  - Training catalog
  - Success Stories
    - https://www.mentor.com/products/fv/success/

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