SEFUW: SpacE FPGA Users Workshop, 4th Edition

Monday, 9 April 2018

Industrial Experiences - Newton 1 and 2 (10:30 - 11:30)

-Conveners: David Dangla

time	[id] title	presenter
10:30	[45] FPGA experience and SoC design methodology at Airbus Defence & Space.	Mr RIED, Ottmar
10:50	[28] Jena-Optronik Experience Summary on Microsemi RTG4 designs	BOTH, Johannes
11:10	[37] SpaceFibre, Spectrometer and Camera: Some applications on the RTG4 FPGA	Prof. PARKES, Steve

Tuesday, 10 April 2018

Industrial Experiences - Newton 1 and 2 (10:00 - 10:20)

-Conveners: Agustin Fernandez-Leon

time	[id] title	presenter
10:00	[11] First Design-In Experiences of Xilinx's, 20 nm, Kintex UltraScale KU060 for Space Applications and 16 nm UltraScale+ RFSoC for Ground Segment	Dr BEDI, Rajan

Industrial Experiences - Newton 1 and 2 (17:10 - 17:30)

-Conveners: David Merodio Codinachs

time	[id] title	presenter
17:10	[10] A Comparison of 65 nm Space-Grade and COTS FPGAs : RTG4 vs. V5QV vs. NG-MEDIUM vs. NG-LARGE vs. IGLOO2 vs. SmartFusion2	Dr BEDI, Rajan

Wednesday, 11 April 2018

Industrial Experiences - Newton 1 and 2 (14:00 - 16:00)

-Conveners: Silvia Moranti

time	[id] title	presenter
14:00	[34] Using Open-source Spacewire and RMAP IPs in the PLATO Router and Data compressor Unit (RDCU)	Dr TONFAT, Jorge
14:20	[35] Virtex5QV - Device & High Speed Interfaces Feedbacks	Mr LAMONACA, DANILO
14:40	[30] Use of FPGAs in a scientific instrument development process: processing, testbenchs, simulators	Mr RAMBAUD, Damien
15:00	[36] Evaluation of a New Mass Memory Controller Architecture on Space-Grade FPGAs	Mr JIA, Lei
15:20	[47] Comparison between Microsemi RTG4 and Xilinx SIRF	Mr VERMERSCH, Felix
15:40	[49] Radiation Testing and End User Validation of the BRAVE NG-Medium FPGA	Mr BERROJO, Luis