SEFUW: SpacE FPGA Users Workshop, 4th Edition

Monday, 9 April 2018

Design Flow - Newton 1 and 2 (11:30 - 12:10)

-Conveners: David Merodio Codinachs

time	[id] title	presenter
11:30	[8] UVVM - Universal VHDL Verification Methodology. Setting a standard for VHDL testbenches	Mr TALLAKSEN, Espen

Design Flow - Newton 1 and 2 (15:10 - 15:30)

-Conveners: Lucana Santos

time	[id] title	presenter
15:10	[15] Evaluation of MATLAB/Simulink and RTL VHDL HDL environment	Mr BRAVHAR, Klemen Mr VAN BEEK, Stephan

Wednesday, 11 April 2018

Design Flow - Newton 1 and 2 (10:00 - 11:10)

-Conveners: David Dangla

time	[id] title	presenter
10:00	[41] QUEENS-FPGA: Quality Evaluation of European New SW for the BRAVE FPGA	Mr GONZALEZ-ARJONA, David
10:25	[40] High-Performance Benchmarking of the European NG-MEDIUM FPGA	Dr LENTARIS, George
10:50	[25] An ECSS-Q-ST-60-02C compliant verification flow for scientific projects	Mr DARMETKO, Marcin