



Techniques for **Radiation Effects** Mitigation in ASICs and FPGAs

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Microelectronics Section, ESA/ESTEC

Techniques for radiation effects mitigation in ASICs and FPGAs handbook

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- ECSS-Q-ST-10-09C Rev.1 – Nonconformance control system (1 March 2018)
- ECSS-Q-ST-20C Rev.2 – Quality assurance (1 February 2018)
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- ECSS-E-ST-40-07C-DIR1: Public Review (24 September 2018 – 31 January 2019)
- ECSS-Q-ST-60-14C Rev.1 DIR1: Public Review (21 September – 19 November 2018)

Previous reviews:

- ECSS-E-HB-20-21A-DIR1: Electrical design and interface requirements for actuators handbook (Public Review: 3 July – 28 September 2018)
- ECSS-E-ST-20-21C-DIR1: Electrical design and interface requirements for actuators (Public Review: 3 July – 28 September 2018)

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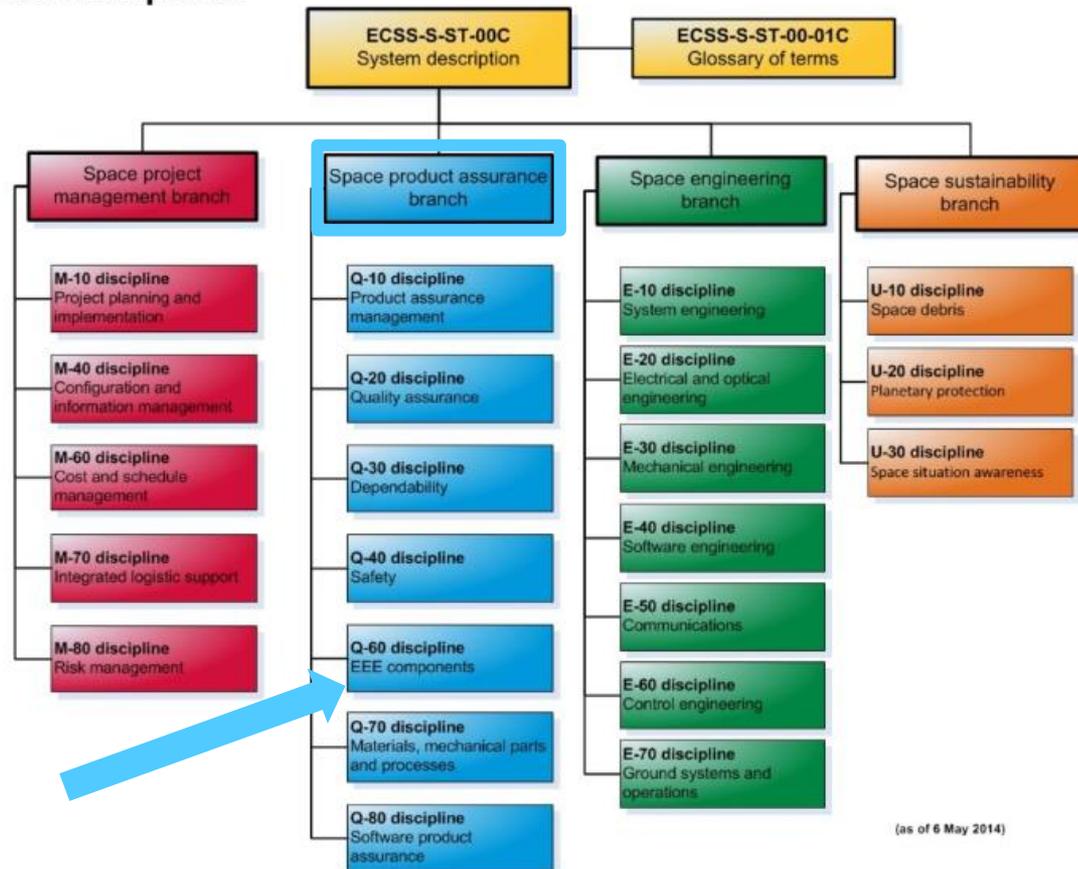
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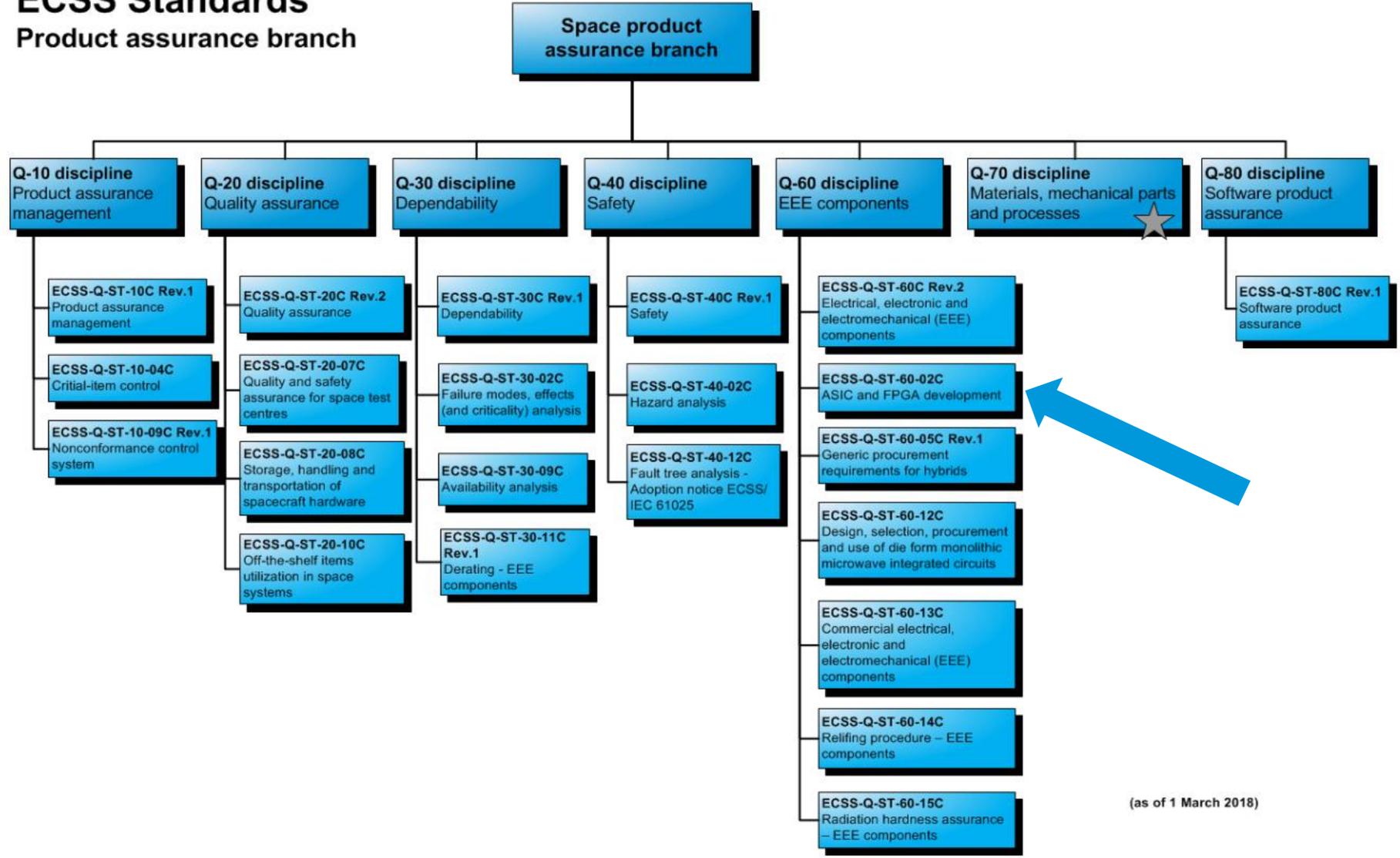
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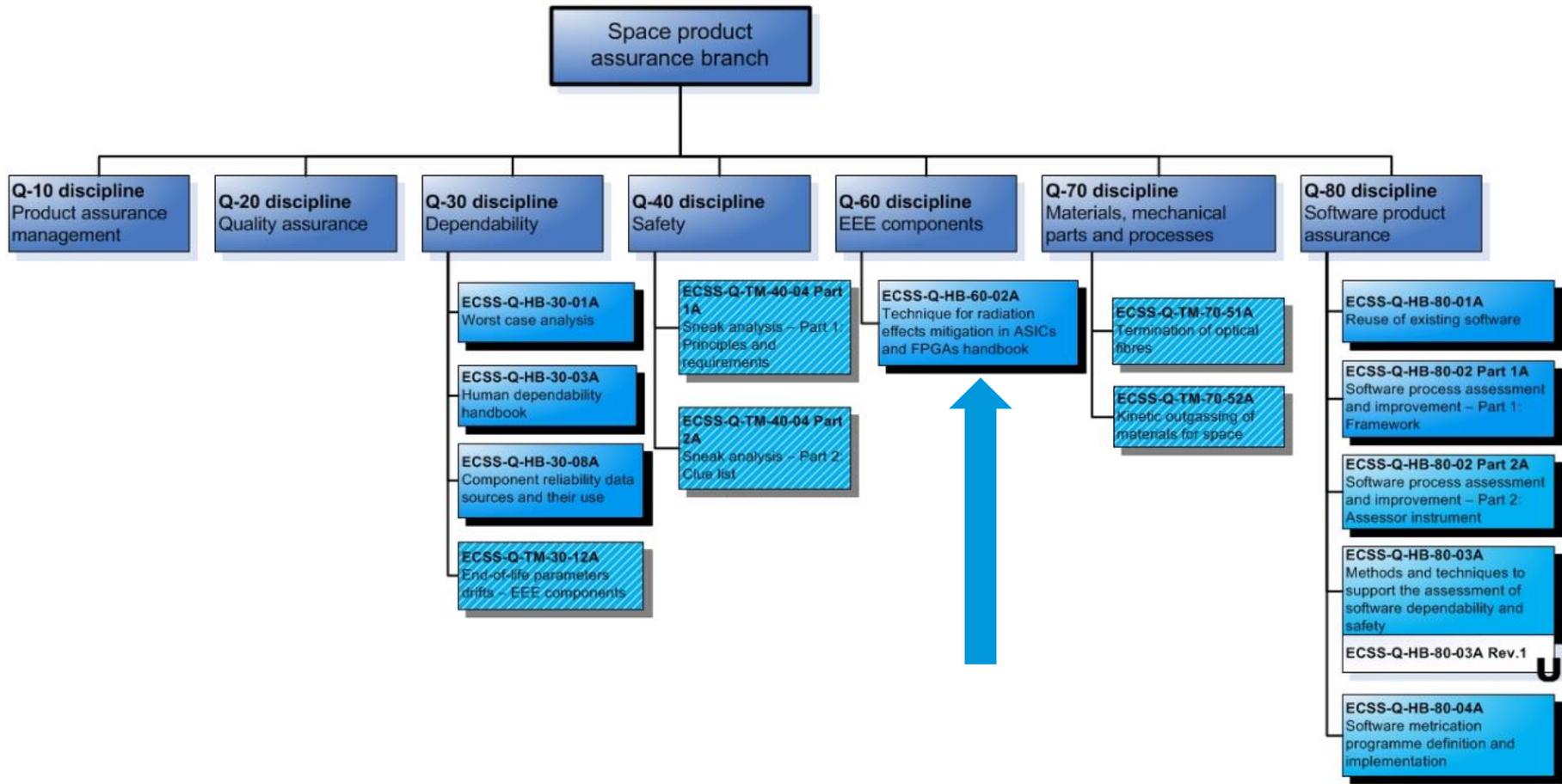
(as of 6 May 2014)

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(as of 1 September 2016)

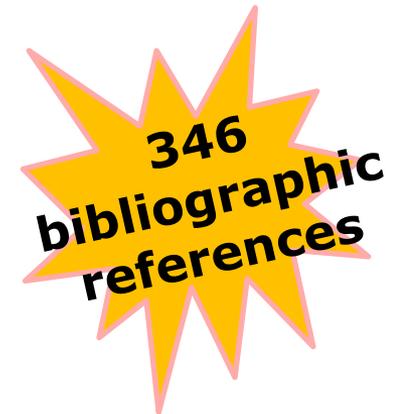
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78
mitigation
techniques



15 validation
techniques



346
bibliographic
references

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Complementing this Handbook, **two additional documents** available at the ESA Microelectronics website :

http://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/Microelectronics_Development_Methodology

1. [ECSS-Q-HB-60-02A Annex](#) (informative) Vendor- or institute-ready ASIC and FPGA technology solutions that include mitigation against radiation effects or that can help to introduce mitigation and/or to validate it
2. [ECSS-Q-HB-60-02A Acknowledgements](#)



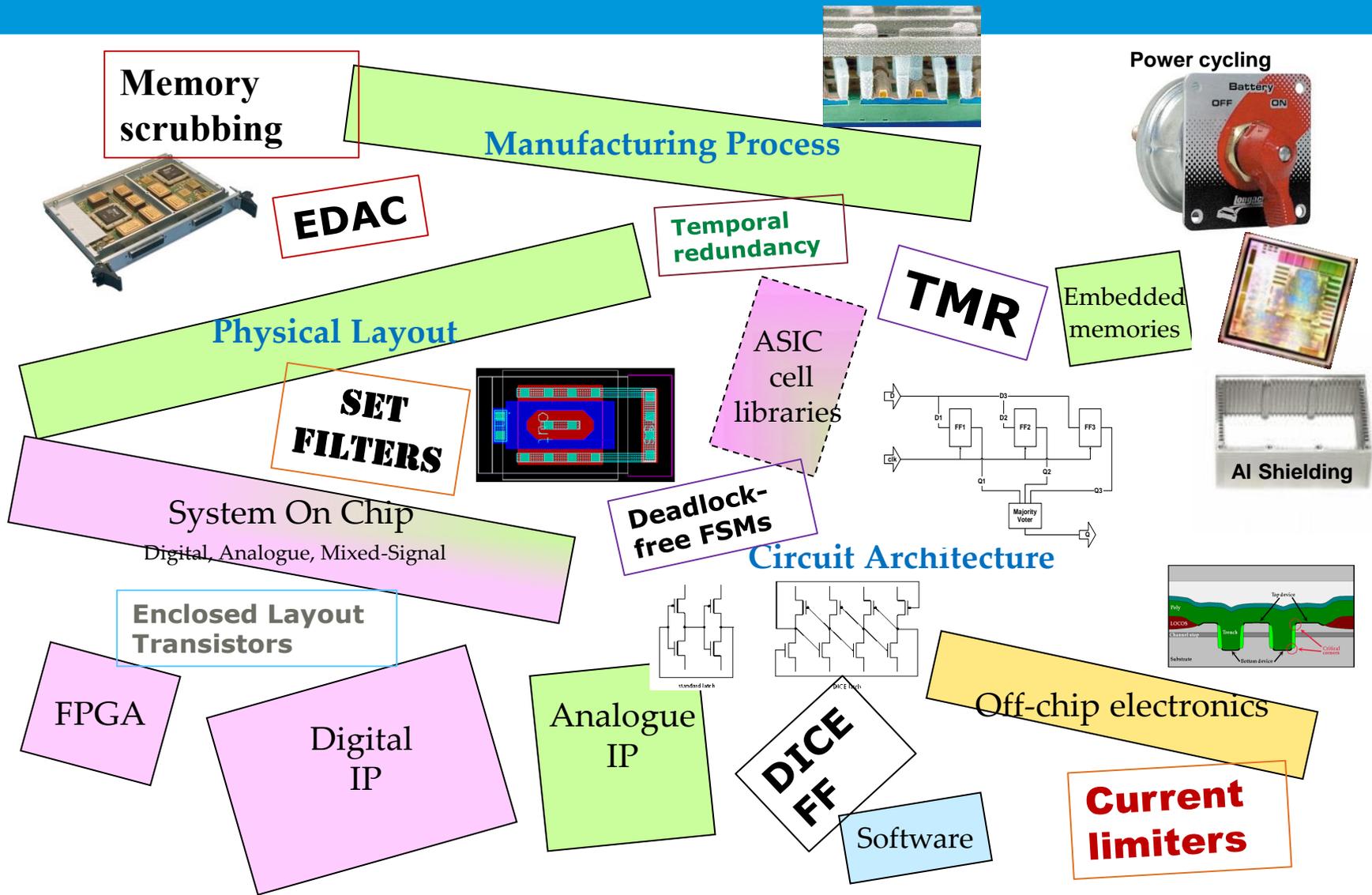
31 experts

from



**13 companies
& institutions**

Many techniques, applied at different stages of chip development, by different people

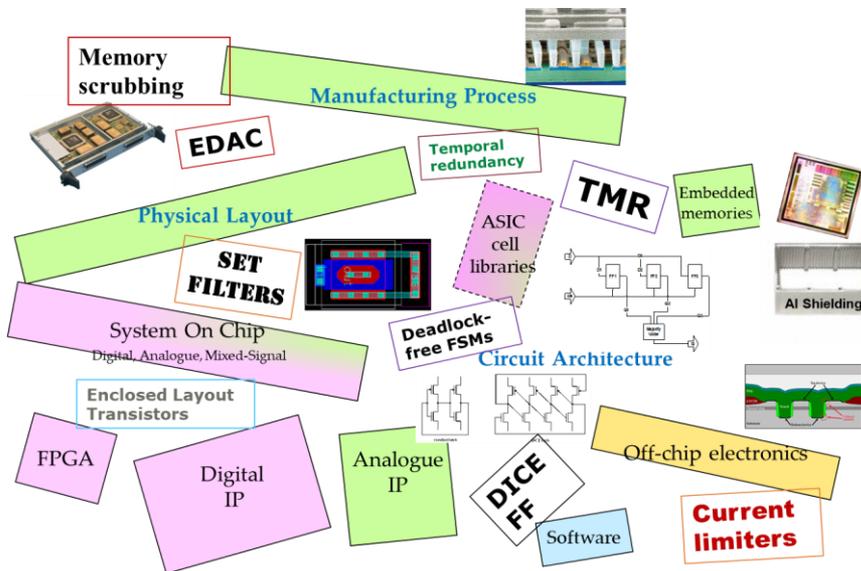


the Handbook Working Group classified all mitigation techniques in

10 GROUPS

belonging to

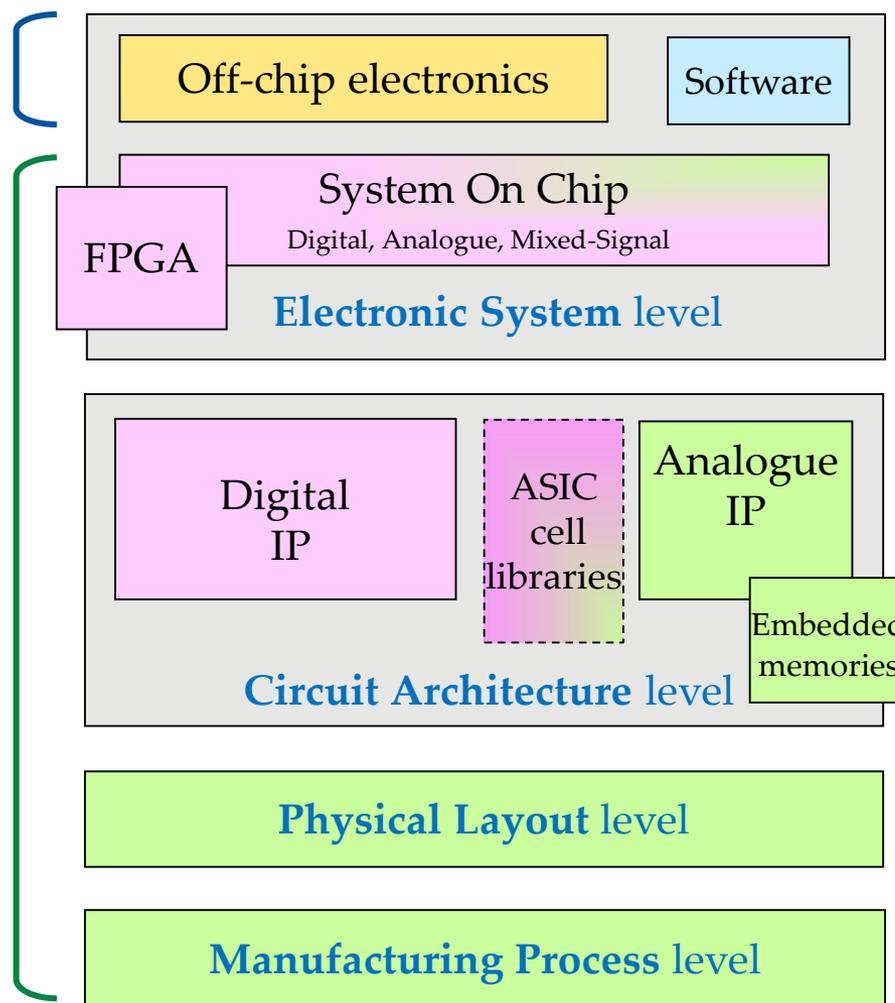
4 "levels"



classification of mitigation techniques, abstraction levels

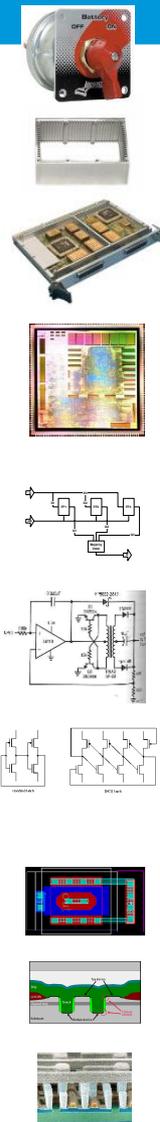
Outside
integrated circuit

Inside
integrated circuit

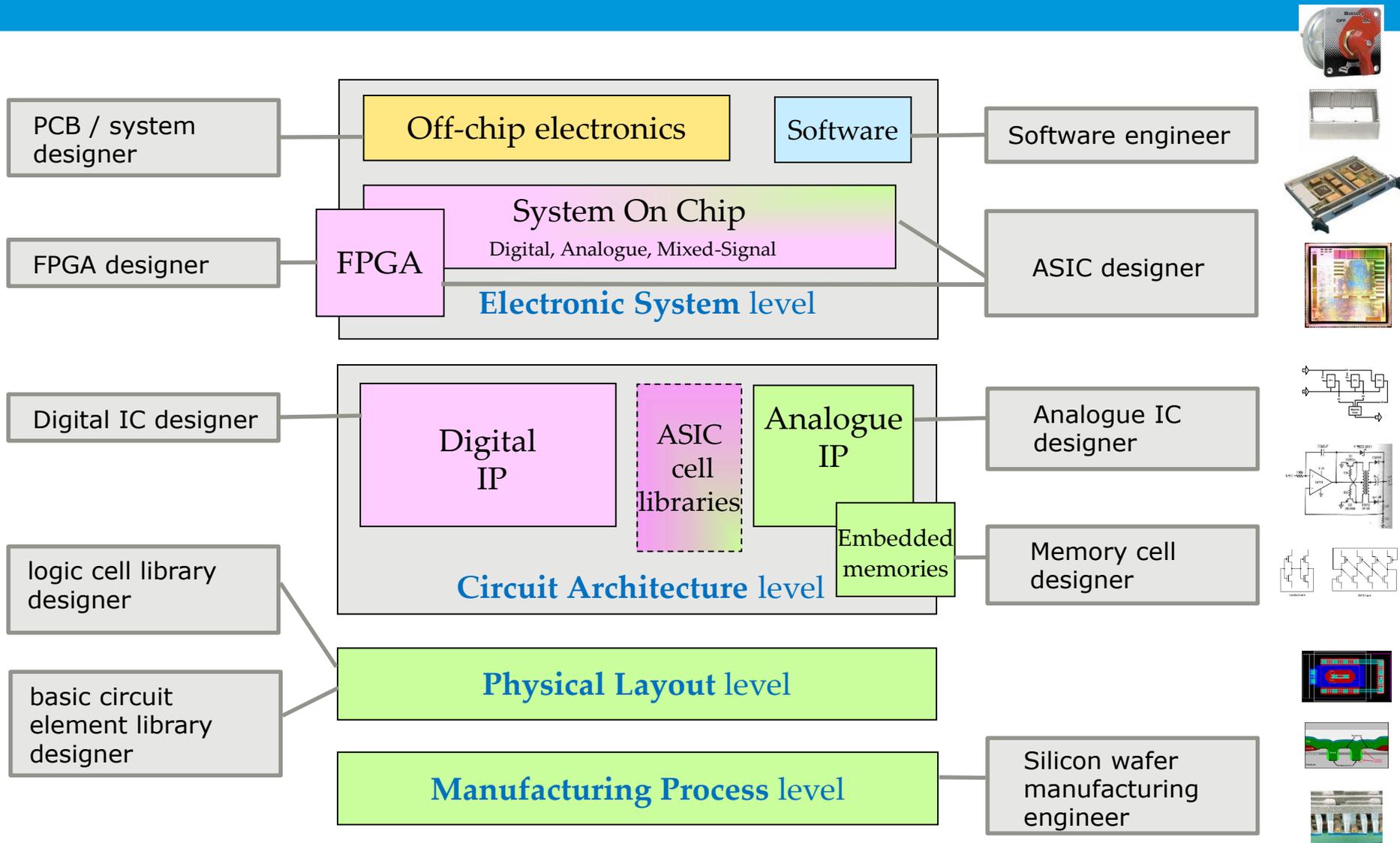


RHBD

RHBP



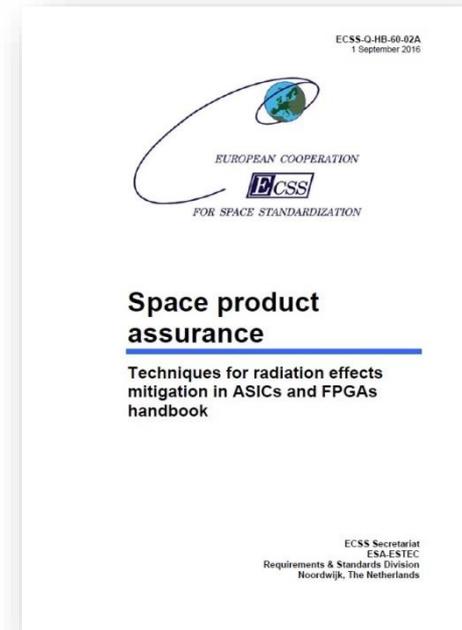
Who implements the mitigation technique ?



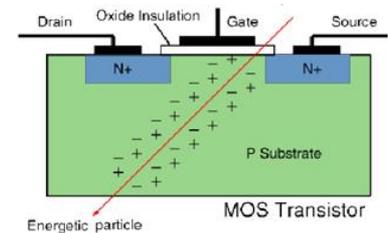
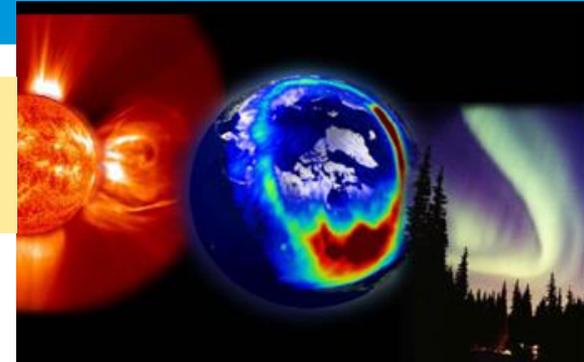
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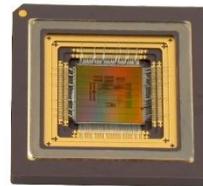
Chapter 5: simplified flow to select mitigation. Many variables: technical requirements, financial, development time and resources

1. What **radiation environment** will affect your IC (what radiation levels for my orbit, mission duration?).
2. Define the **reliability targets**, i.e. how many errors (of a given fault class) per time unit (e.g. year) can be tolerated by the user.
3. Identify candidate **IC technologies or existing parts** and collect data on **their sensitivity** to TID and SEE.
4. Identify and quantify all **the effects (pros and cons) of mitigation** techniques which can be introduced at the various levels.
5. **Choose the best compromise** of mitigation that allows to meet the reliability targets while also respecting the rest of the requirements. In doing this, the expected levels of final fault tolerance (e.g. error rates) are estimated by analysis, simulation or tests.

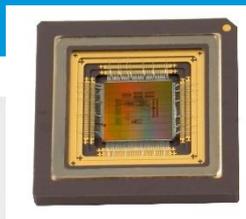
Once implemented, validate the selected approach by fault-injection and/or radiation testing.

... which ones were used in a few concrete examples ?

device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)



a "cocktail" of several techniques in each device



5 devices , 5 cocktails



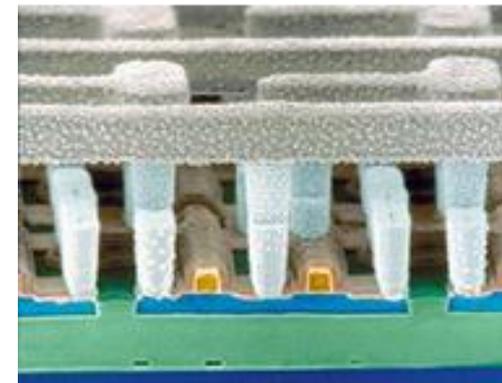
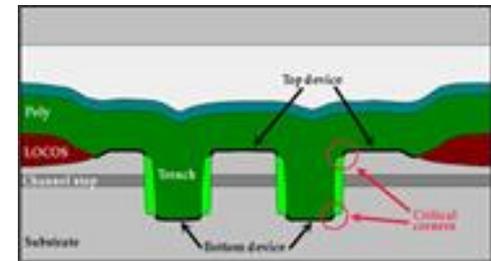
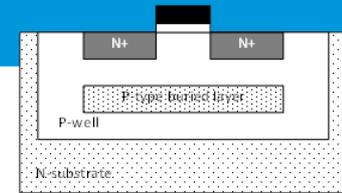
TOTAL number of techniques used

21 12 13 14 22

Device type	Multi-core microprocessor	Single-core microprocessor	Application SoC ASIC	Multi-core microprocessor	FPGA
Vendor or name	TALOS	Microchip Atmel (FPGA)	ASIC (FPGA)	Custom Gasket (ASIC)	Microchip (FPGA)
Microchip name	DPC	AT697F	SCOC3	GR740	BRAVE HD-LARGE NX1H140
Microchip technology	90nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS	28nm CMOS (BRAVE based config)
6 Technology selection and process level mitigation					
6.1.1 Software errors	?	X	X	X	X
6.1.2 Memory retention				X	X
6.1.3 Triple write				X	X
6.1.4 Burned fuses				deep N-well	deep N-well
6.1.5 On-chip memory					
6.1.6 High-impedance tri-state					
7 Layout					
7.1.1 Impact of Enclosed Layer Transition	X			X	?
7.1.2 Critical impedance range	X	X	X	X	X
7.1.3 Current vias					
7.1.4 Transition Edge Reflection (TER)	X	X	X	X	X
8 Analogous circuitry					
8.1.1 Node capacitance/charge separation	?				?
8.1.2 Analogous redundancy (overaging)	?				?
8.1.3 Memory overaging	?				?
8.1.4 Preaging	?				?
8.1.5 Modulation in bandwidth, gain, operating speed, and current drive	?				?
8.1.6 Redundant hardware redundancy	?				?
8.1.7 Redundant high impedance nodes	?				?
8.1.8 Memory overage	?				?
8.1.9 Non-persistent	?				?
9 Memory cells and Embedded memory blocks					
9.1.1.1 Memory cell	?				?
9.1.1.2 Capacitor loading	?				?
9.1.1.3 SRAM cell					
9.1.1.4 SRAM cell					
9.1.1.5 DRAM cell					
9.1.1.6 DRAM cell	X	X	X	X	X
9.1.1.7 DRAM cell					
9.1.1.8 DRAM cell					
9.1.2 DRAM cell	?	X	X	X	?
9.1.3 Data scrubbing					
10 Radiation hardened ASIC libraries					
10.1 MIC (ASIC) library	CMOS	ATC18000	ATC18000	CSDFACE	CSDFACE
10.2 CMOS 0.5µm radiation hardened library	X				
10.3 CMOS 0.5µm radiation hardened library					
10.4 CMOS 0.5µm radiation hardened library					
10.5 CMOS 0.5µm radiation hardened library					
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10.9 CMOS (FPGA) library					
10.10 CMOS (FPGA) library					
11 Digital circuits					
11.1.1 Data retention					
11.1.1.1 Data retention				X	at proc diffused FFs
11.1.2 Data retention					
11.1.2.1 Data retention			X		
11.1.2.2 Triple temporal redundancy combined with spatial redundancy		X	?		
11.1.2.3 Memory level redundancy					
11.1.2.4 Memory level redundancy					
11.1.2.5 Memory level redundancy					
11.1.2.6 Memory level redundancy					
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Process level, examples

device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

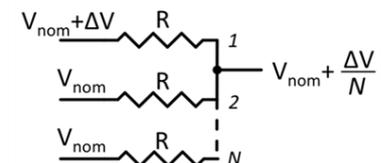
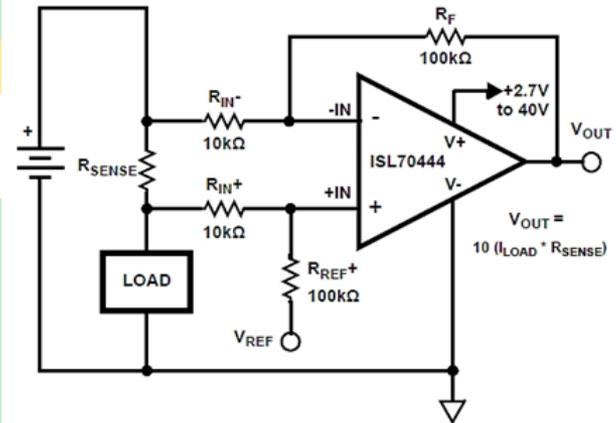
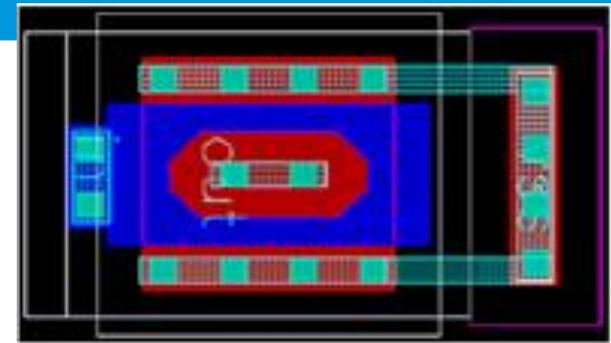
Mitigation Tech code in ECSS-Q-HB-60-02

6 Technology selection and process level mitigation

6.2.1	Epitaxial layers	?	x	x	x	x
6.2.2	Silicon On Insulator					
6.2.3	Triple wells				x	x
6.2.4	Buried layers				deep N-well	deep N-well
6.2.5	Dry thermal oxidation					
6.2.6	Implantation into oxides					

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Layout level, examples

device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
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microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

Mitigation Tech code in ECSS-Q-HB-60-02

7 Layout						
7.2.1	Ringed or Enclosed Layout Transistor	x				?
7.2.2	Contacts and guard rings	x	x	x	x	x
7.2.3	Dummy transistors					
7.2.4	Transistors Gate W/L ratio sizing	x	x	x	x	x

Analogue circuits level, examples

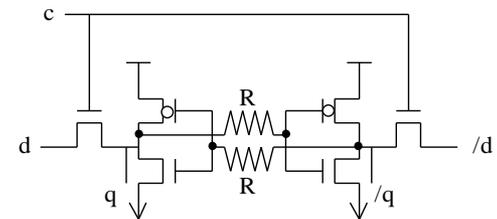
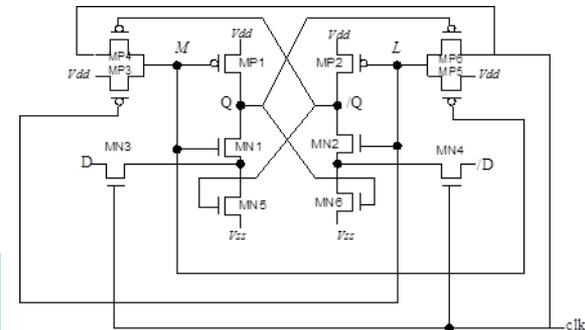


device type	ASIC				FPGA
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microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

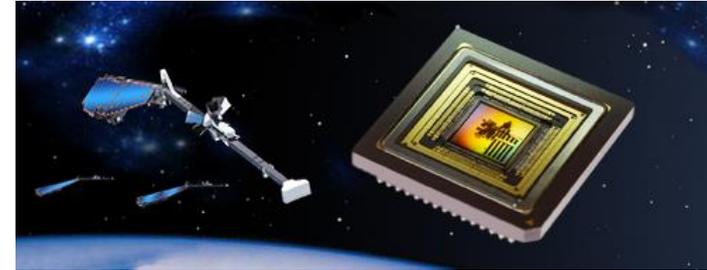
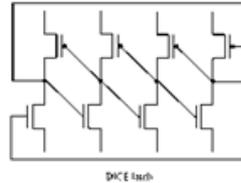
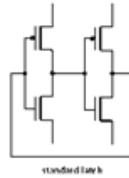
Mitigation
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8 Analogue circuits					
8.2.1	Node Separation and Inter-digitation	?			?
8.2.2	Analogue redundancy (averaging)	?			?
8.2.3	Resistive decoupling	?			?
8.2.4	Filtering	?			?
8.2.5	Modifications in bandwidth, gain, operating speed, and current drive	?			?
8.2.6	Reduction of window of vulnerability	?			?
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Memory cells, embedded memory blocks and rad-hard libraries level, examples



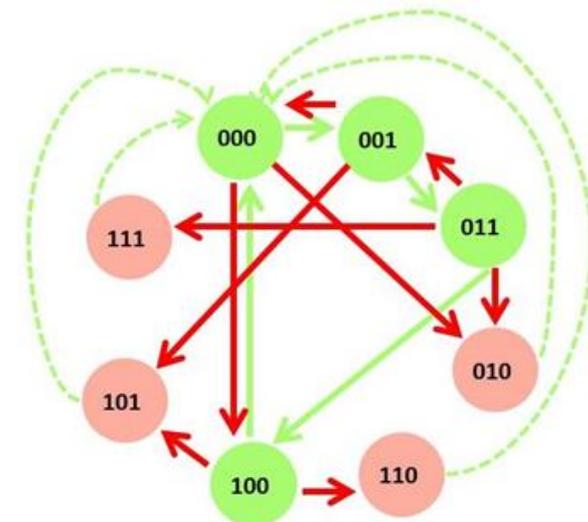
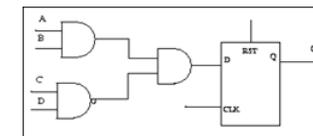
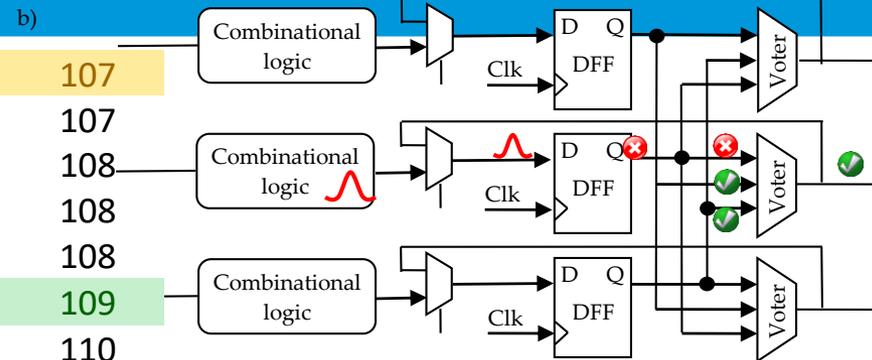
device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

Mitigation Tech code in ECSS-Q-HB-60-02

9	Memory cells and Embedded memory blocks				
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9.2.1.6	DICE hardened memory cell		x	x	x
9.2.1.7	NASA-Whitaker hardened memory cell				
9.2.1.8	NASA-Liu hardened memory cell				
9.2.2	Bit-interleaving in memory arrays	?	x	x	?
9.2.3	Data scrubbing				
10	Radiation-hardened ASIC libraries	DARE180	ATC18RHA-U	ATC18RHA-U	C65SPACE

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Digital circuits, examples

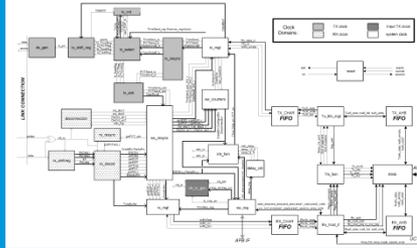


device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
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microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

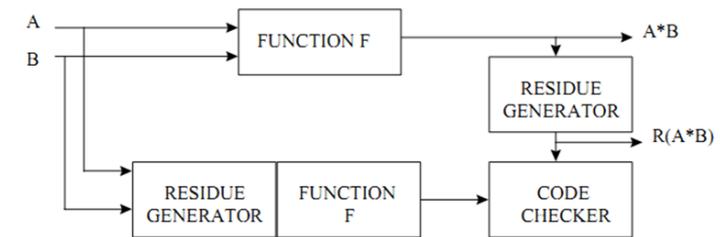
Mitigation Tech code in ECSS-Q-HB-60-02

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11.2.2.1.3	Minimal level sensitive latch				
11.2.3	Fail-safe, deadlock-free finite state machines	?		?	
11.2.4	Selective use of logic cells, clock and reset lines hardening	x	x	x	x x

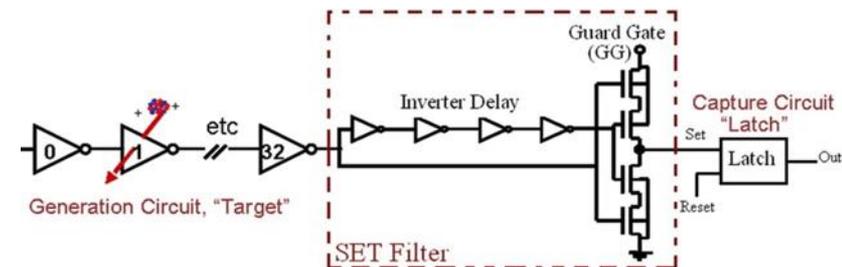
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7 bits of data	Number of "1"	8-bits including parity bit	
		even	odd
000 0000	0	<u>0</u> 000 0000	<u>1</u> 000 0000
101 0001	3	<u>1</u> 101 0001	<u>0</u> 101 0001
110 1001	4	<u>0</u> 110 1001	<u>1</u> 110 1001
111 1111	7	<u>1</u> 111 1111	<u>0</u> 111 1111



System-on-a-Chip level, examples

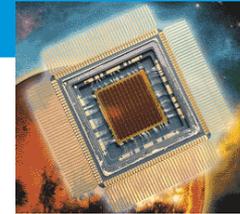


device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

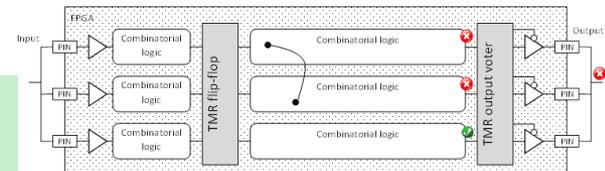
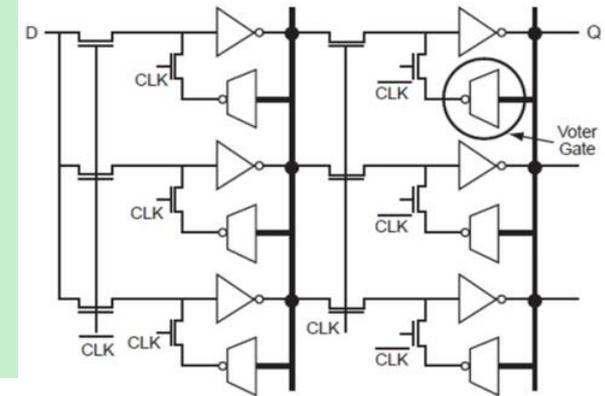
Mitigation Tech code in ECSS-Q-HB-60-02

12 System on a chip					
12.2.1.1.3	Cyclic Redundancy Check	?			
12.2.1.1.4	BCH codes				
12.2.1.1.5	Hamming codes				
12.2.1.1.6	SEC-DED codes		x	x	x
12.2.1.1.7	Reed-Solomon codes			x	x
12.2.1.1.8	Arithmetic codes				
12.2.1.1.9	Low Density Parity Codes				
12.2.2	Mitigation for Memory Blocks				
12.2.3	Filtering SET pulses in data paths				
12.2.4	Watchdog timers		x	x	x
12.2.5	TMR in mixed-signal circuits	?			

13 Field Programmable Gate Arrays



of the Virtex-52V FPGA has been qualified for high-radiation, deep-space applications.



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FPGA level, examples



device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

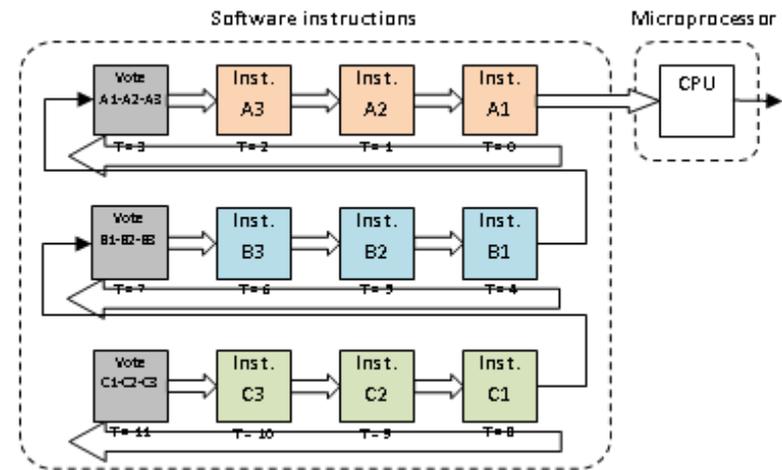
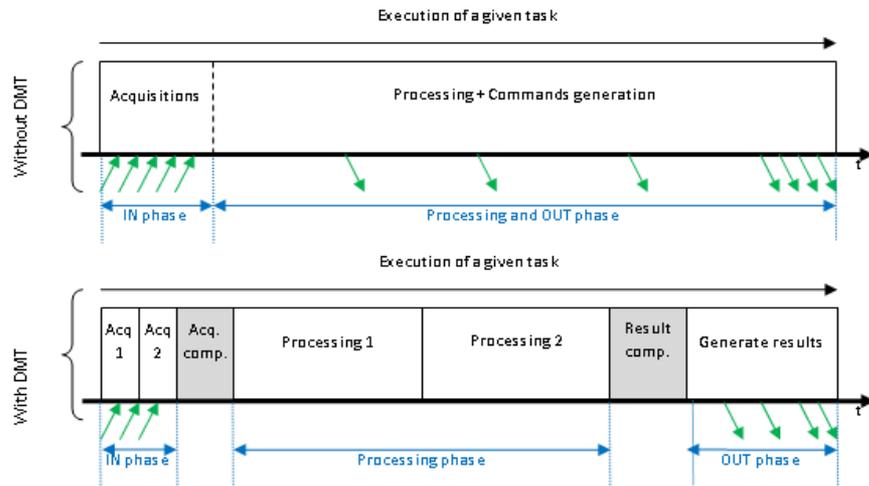
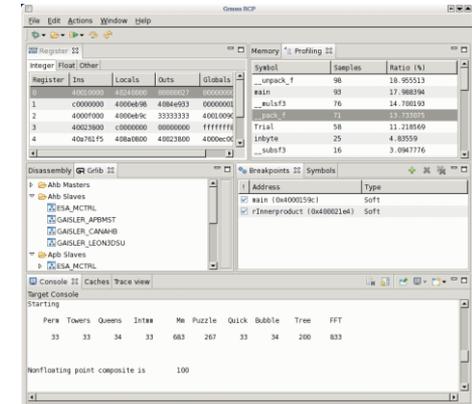
Mitigation Tech code in ECSS-Q-HB-60-02

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13.2.5	Additional voters in TMR data-paths to minimise DCE				
13.2.6	Reliability-oriented place and Route Algorithm (RoRA)				
13.2.7	Embedded processor protection				
13.2.8.1.2	Full scrubbing				CMIC
13.2.8.1.3	Partial scrubbing				
13.2.8.1.4	Partial reconfiguration				

14 Software-implemented hardware fault tolerance

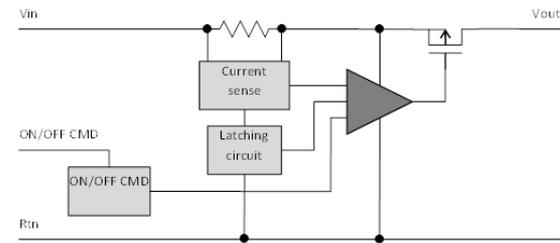
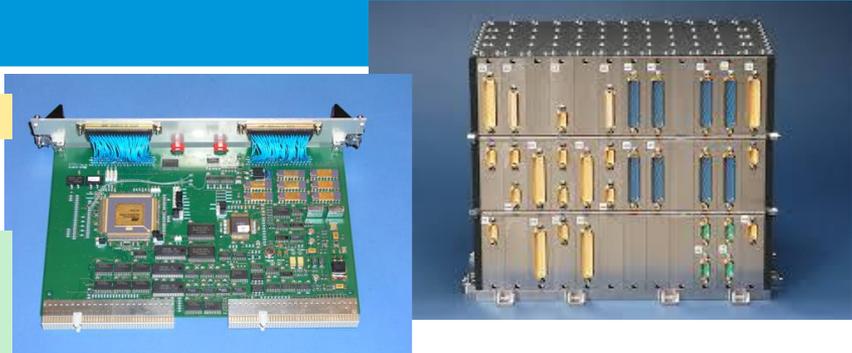
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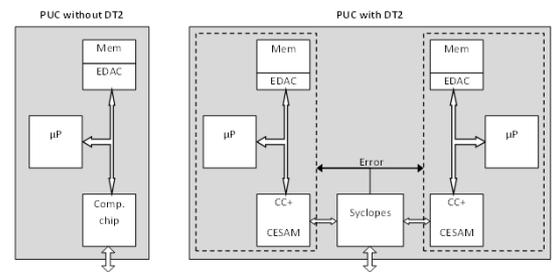
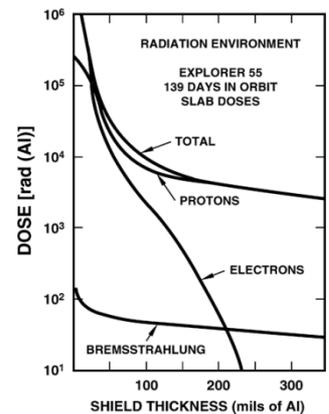


15 System architecture (off-chip)

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Power cycling



SW and system (off-chip) level, examples



device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

Mitigation Tech code in ECSS-Q-HB-60-02

14 Software-implemented hardware fault tolerance

- 14.2.1 Redundancy at instruction level
- 14.2.2 Redundancy at task level
- 14.2.3 Redundancy at application level: using a hypervisor

15 System architecture

- 15.2.1 Shielding
- 15.2.2 Watchdog timers
- 15.2.3 Power cycling and reset
- 15.2.4 Latching current limiters
- 15.2.5.2.2 Lockstep
- 15.2.5.2.3 Double duplex
- 15.2.5.2.4 Double Duplex Tolerant to Transients
- 15.2.5.3 Triple Modular Redundant system
- 15.2.6 Error Correcting Codes
- 15.2.7 Off-chip SET filters

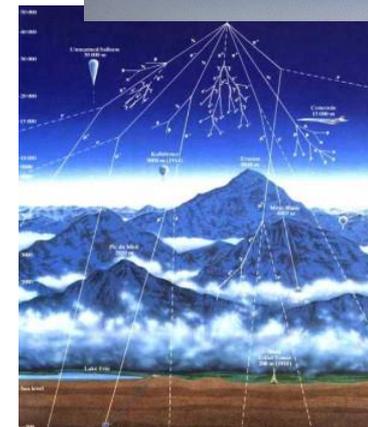
TMR variants in this Handbook



Type of TMR	11 - Digital Circuits	12 - SoC	13 - FPGA	15 - Off-chip		3x Flip flops	3x combinatorial logic	3x voter	Extra voters in data paths	Triplets physical layout separated	3x memory blocks	comparing analog signals	3x chip	Synchronizing logic	3x outputs
Basic TMR	x					x									
Full TMR	x					x	x	x							
Local TMR			x			x									
Global TMR			x			x	x	x							x
Large grain TMR			x			x	x	x		x					x
Embedded memory TMR			x								x				
TMR with voters against DCE			x			x	x	x	x						
Mixed-signal TMR		x										x			
Chip-level TMR				x									x	x	

16 Validation methods (1/2)

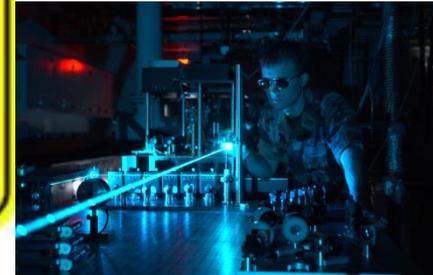
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- ◆ **Radiation Facilities in use by ESA** <https://escies.org/ReadArticle?docId=230>
 - ▲ Co-60 at ESA/ESTEC, Netherlands (total dose)
 - ▲ Californium-252 at ESA/ESTEC, Netherlands
 - ▲ Paul Scherrer Institut (PSI), Switzerland: proton irradiation
 - ▲ Louvain la Neuve (UCL), Belgium: heavy ions and protons
 - ▲ Jyväskylä University, Finland: heavy ions and protons



The ECSS-Q-HB-60-02 WG chose to group and name 78 techniques in 10 “LEVELS”, mainly according to WHO maybe applying or choosing the techniques, depending on role of the person involved in the chip selection or design or manufacturing or programming or integration on system phases

but

There are of course many other ways to classify and present this information

Unfortunately, there is **no universal recipe** nor cookbook (flowchart) to guide you to decide which mitigation cocktail is best for your ASIC or FPGA.

many variables: radiation environment expected, what radiation sensitivity is tolerable by the system using the chip, costs of applying mitigation, experience applying mitigation, project costs and timing constraints...



Sometimes **LESS can be BETTER**: Every technique has a cost associated (power, speed, area, time and manpower resources to apply and test it...) . Too many overlapping techniques can raise overall chip sensitivity: more logic elements can introduce more radiation sensitive areas or parasitic devices, which can cause additional or new unwanted radiation effects

