Techniques for Radiation Effects Mitigation in ASICs and FPGAs

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ECSS-Q-HB-60-02

Techniques for radiation effects mitigation in ASICs and FPGAs handbook

since September 2016 publicly available from www.ecss.nl

ECSS : European Cooperation for Space Standardization

The European Cooperation for Space Standardization is an initiative established to develop a coherent, single set of user-friendly standards for use in all European space activities.

4 disciplines (or branches)

- Space Project Management
- Space Product Assurance
- Space Engineering
- Space Sustainability

3 types of documents

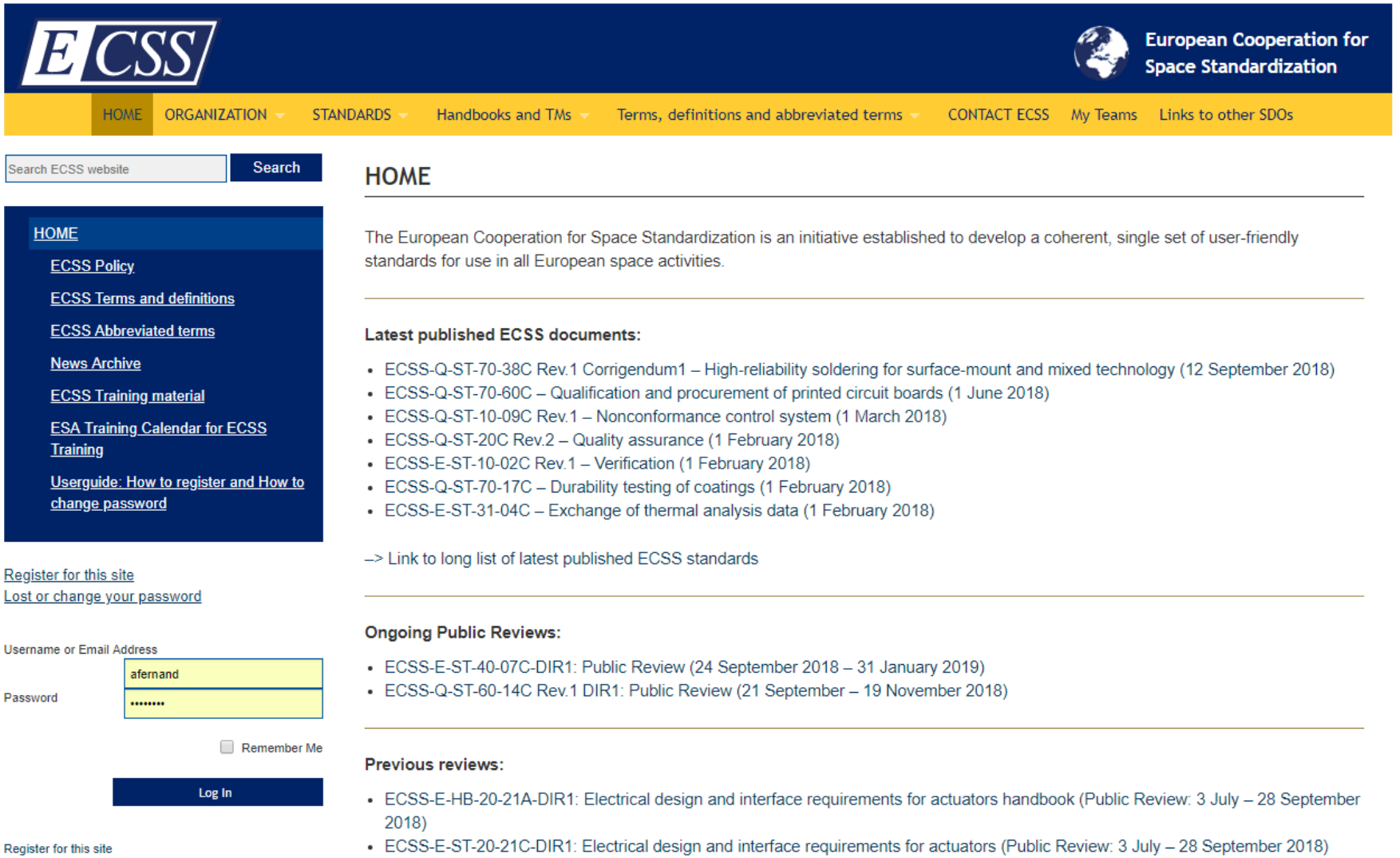
- Standards (normative)
- Handbooks (non-normative)
- Technical Memoranda (non-normative)

What is an ECSS Handbook ?

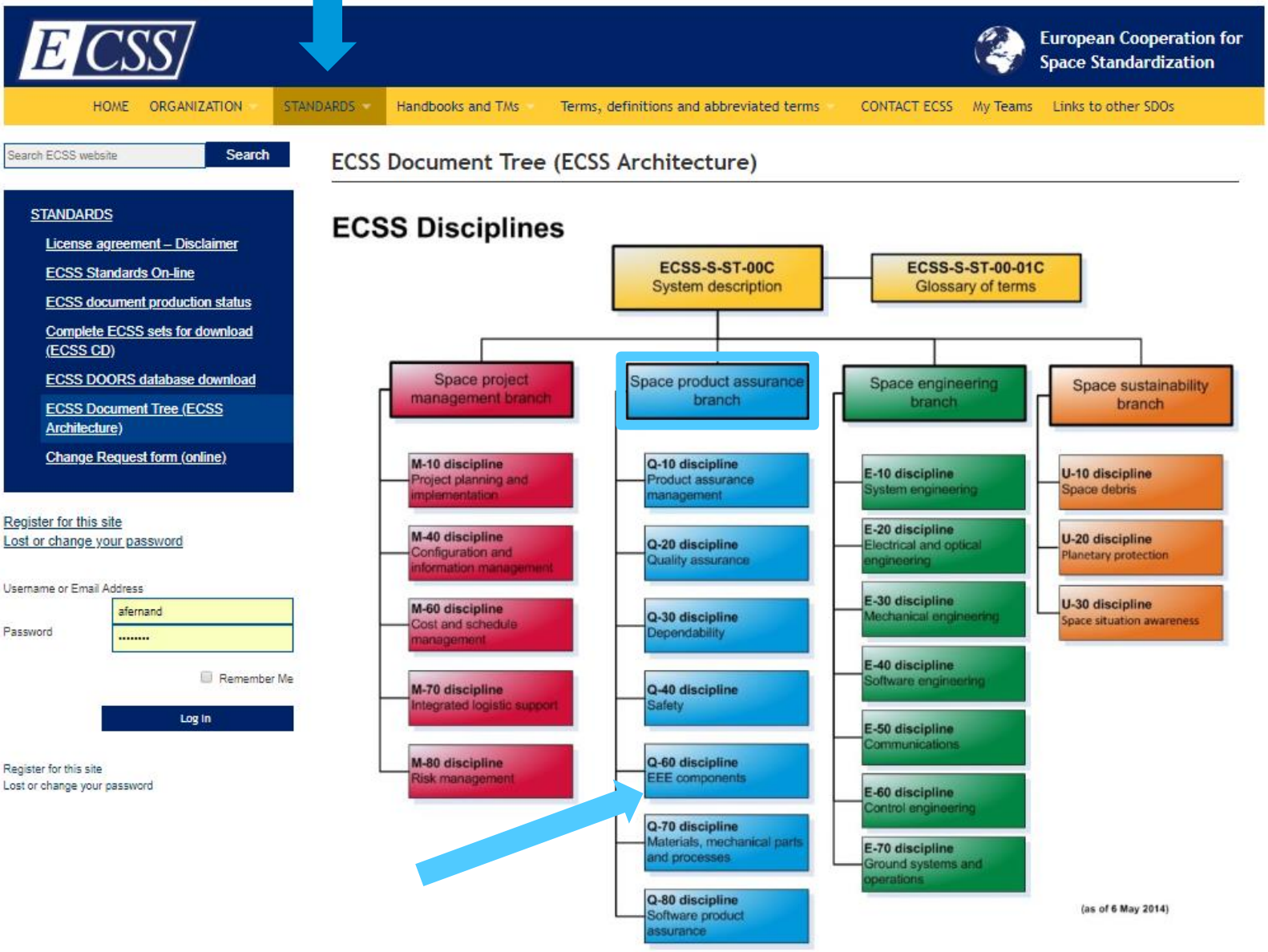
non-normative document providing background information, orientation, advice or recommendations related to one specific discipline or to a specific technique, technology, process or activity

European Cooperation for Space Standardization

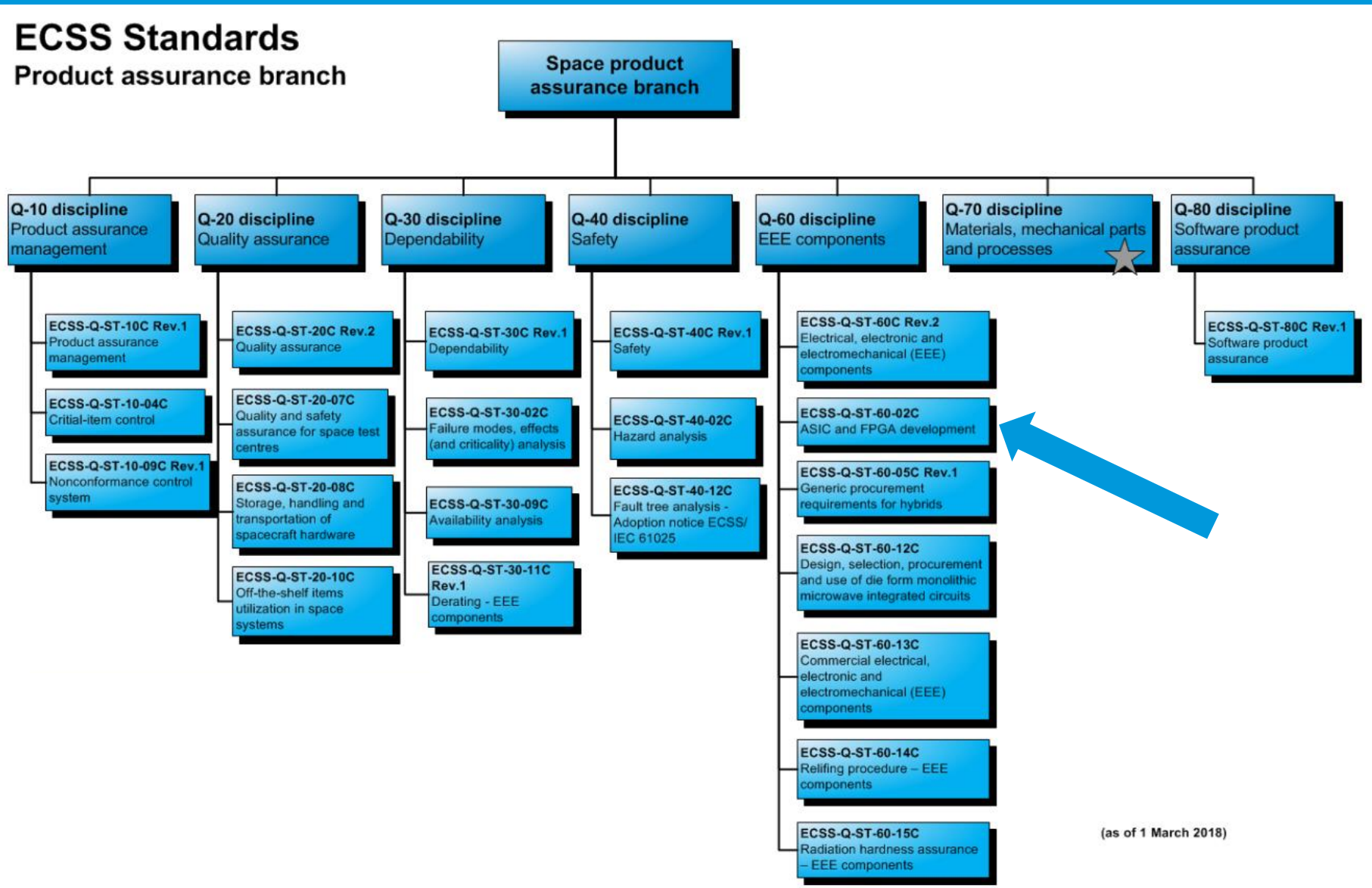
ecss.nl



ECSS Disciplines



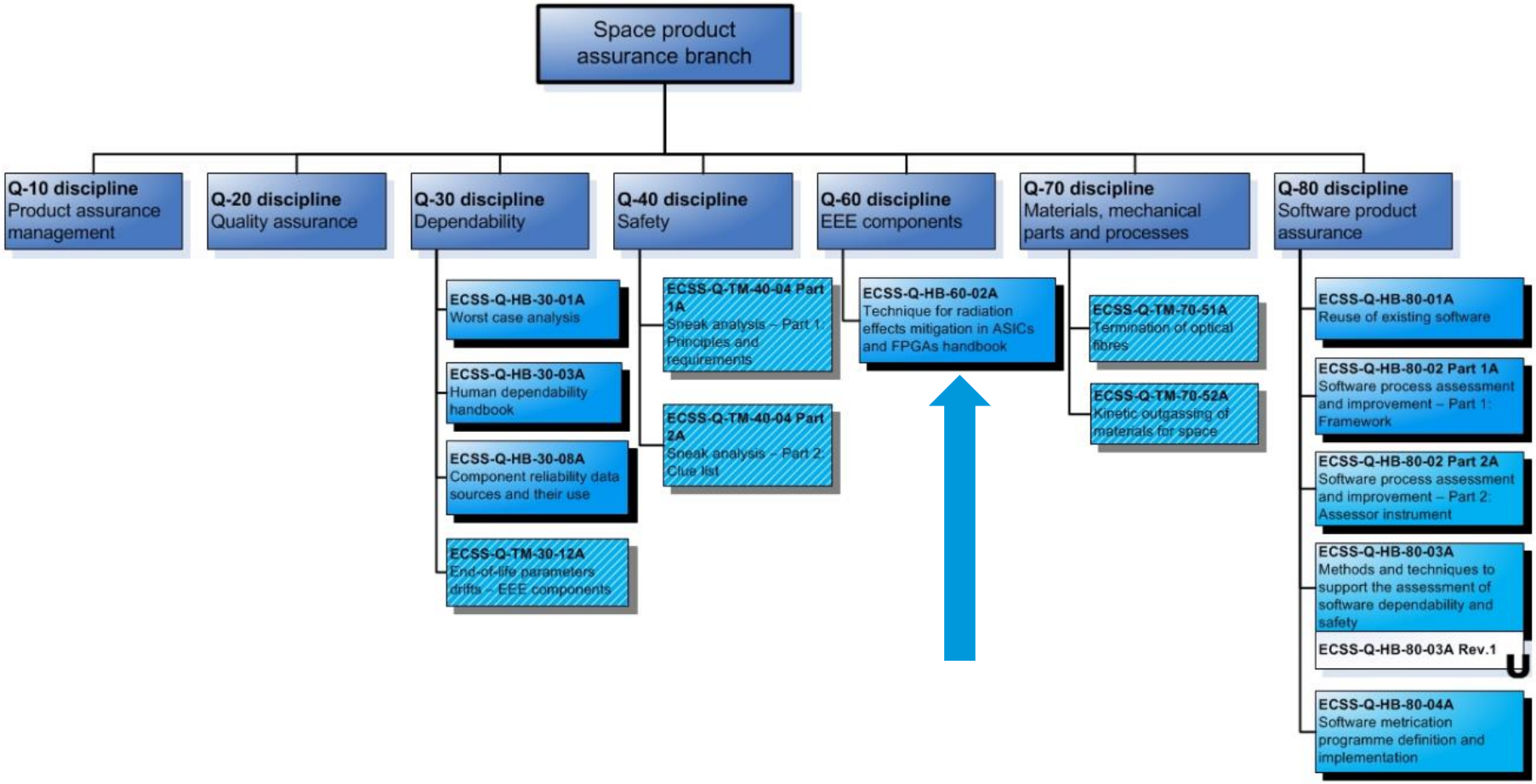
Standards, product assurance, EEE components



HB and TM, product assurance, EEE components

ECSS Handbooks and Technical memoranda

PA branch HBs and TMs



(as of 1 September 2016)

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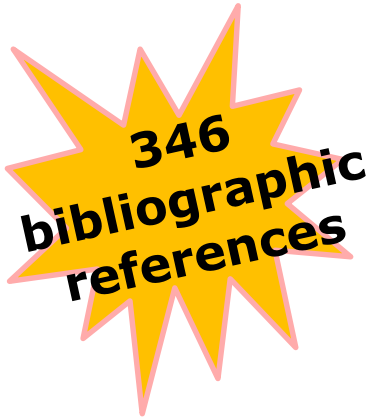

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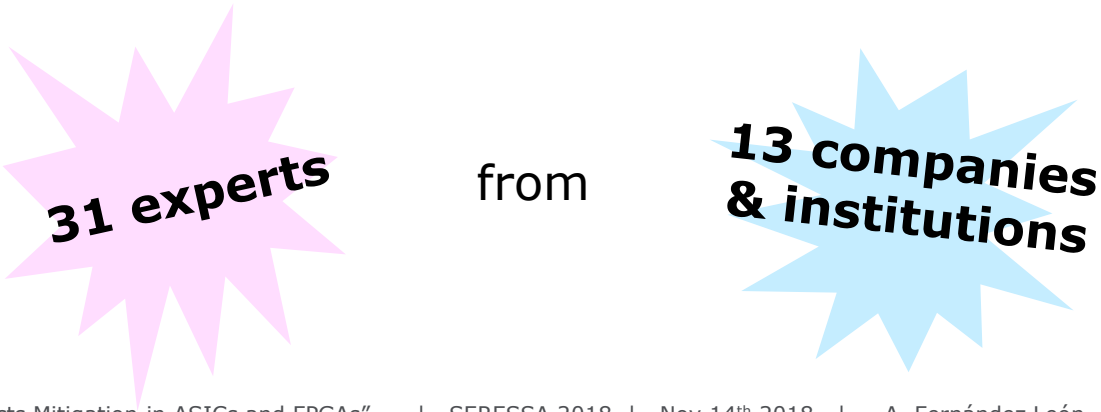
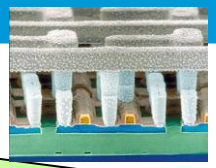
Techniques for radiation effects mitigation in ASICs and FPGAs handbook

Complementing this Handbook, **two additional documents** available at the ESA Microelectronics website :
http://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/Microelectronics_Development_Methodology

1. **ECSS-Q-HB-60-02A Annex** (informative) Vendor- or institute-ready ASIC and FPGA technology solutions that include mitigation against radiation effects or that can help to introduce mitigation and/or to validate it
2. **ECSS-Q-HB-60-02A Acknowledgements**



Many techniques, applied at different stages of chip development, by different people



Power cycling

Memory scrubbing

Manufacturing Process

EDAC

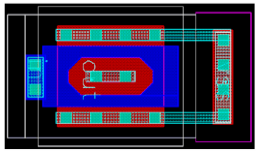
Temporal redundancy

TMR

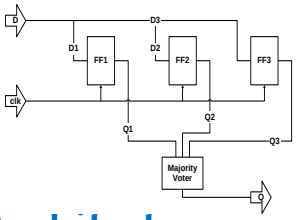
Embedded memories

Physical Layout

SET FILTERS



ASIC cell libraries

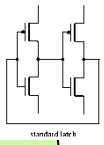


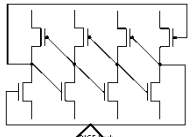
System On Chip

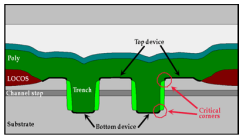
Digital, Analogue, Mixed-Signal

Deadlock-free FSMs

Circuit Architecture







Enclosed Layout Transistors

FPGA

Digital IP

Analogue IP

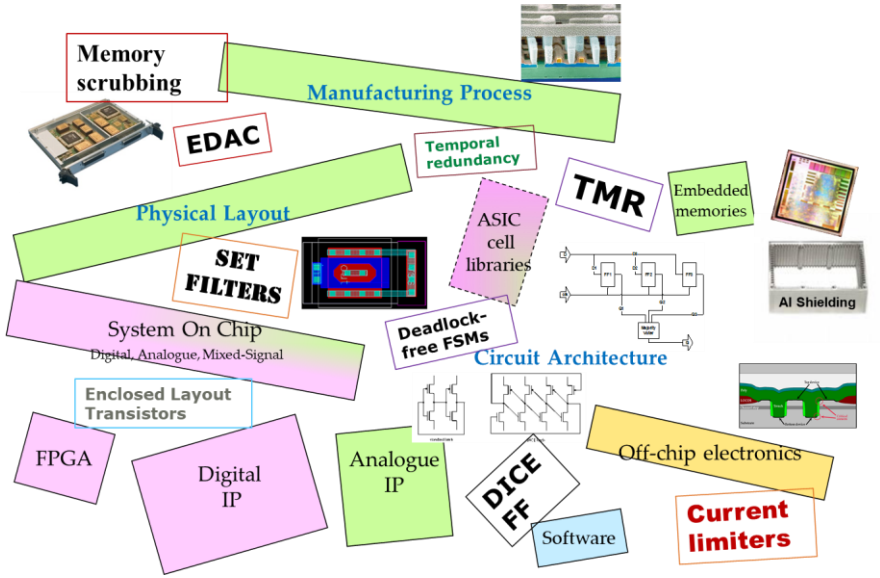
DICE FF

Off-chip electronics

Software

Current limiters

How to classify and present the information …



the Handbook Working Group classified all mitigation techniques in

10 GROUPS

belonging to

4 "levels"

classification of mitigation techniques, abstraction levels

Outside
integrated circuit

Inside
integrated circuit

Off-chip electronics

Software

System On Chip
Digital, Analogue, Mixed-Signal

FPGA

Electronic System level

Digital IP

ASIC cell libraries

Analogue IP

Embedded memories

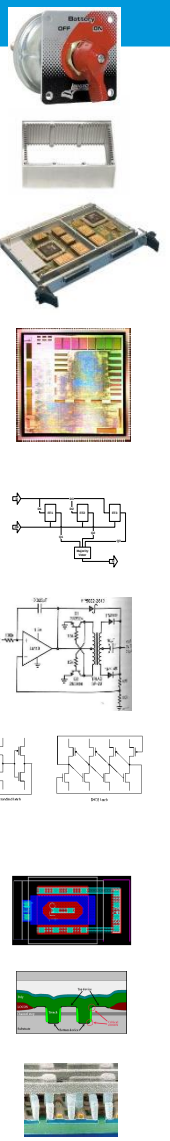
Circuit Architecture level

Physical Layout level

Manufacturing Process level

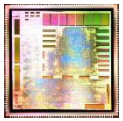
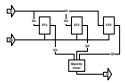
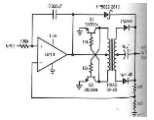
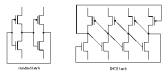
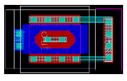
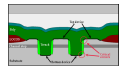
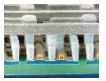
RHBD

RHBP



Who implements the mitigation technique ?



PCB / system designer

FPGA designer

Off-chip electronics

Software

System On Chip

Digital, Analogue, Mixed-Signal

FPGA

Electronic System level

Software engineer

ASIC designer

Digital IC designer

logic cell library designer

basic circuit element library designer

Digital IP

ASIC cell libraries

Analogue IP

Embedded memories

Circuit Architecture level

Analogue IC designer

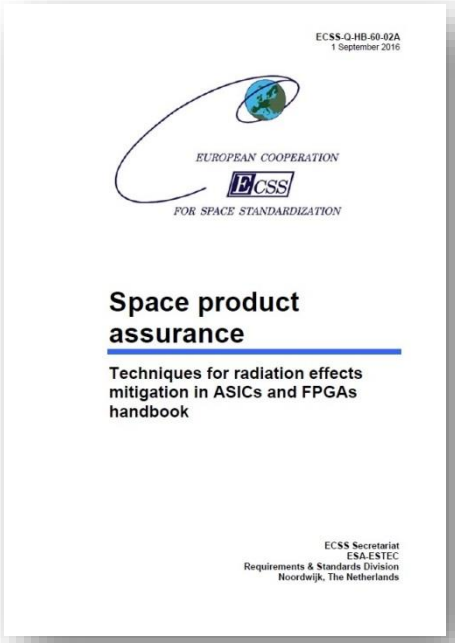
Memory cell designer

Physical Layout level

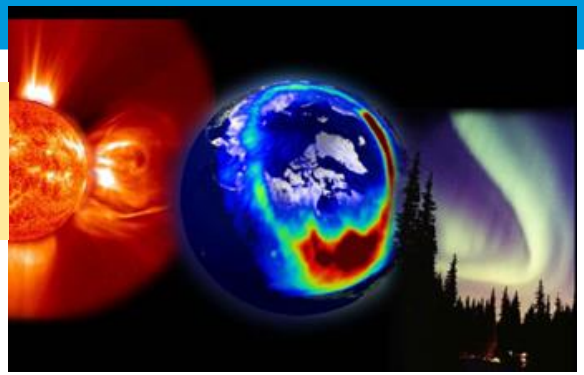
Manufacturing Process level

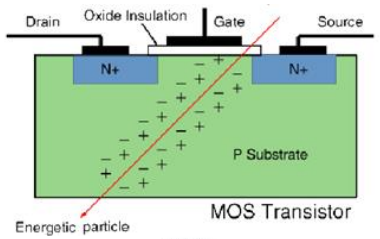
Silicon wafer manufacturing engineer

Techniques for radiation effects mitigation in ASICs and FPGAs handbook



ECSS-Q-HB-60-02: the first chapters





Choosing a device hardening strategy

Chapter 5: simplified flow to select mitigation. Many variables: technical requirements, financial, development time and resources

1. What **radiation environment** will affect your IC (what radiation levels for my orbit, mission duration?).
2. Define the **reliability targets**, i.e. how many errors (of a given fault class) per time unit (e.g. year) can be tolerated by the user.
3. Identify candidate **IC technologies or existing parts** and collect data on **their sensitivity** to TID and SEE.
4. Identify and quantify all **the effects (pros and cons) of mitigation** techniques which can be introduced at the various levels.
5. **Choose the best compromise** of mitigation that allows to meet the reliability targets while also respecting the rest of the requirements. In doing this, the expected levels of final fault tolerance (e.g. error rates) are estimated by analysis, simulation or tests.

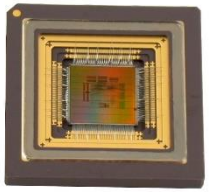
Once implemented, validate the selected approach by fault-injection and/or radiation testing.

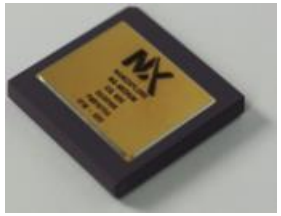
78 mitigation techniques listed in the HB…

6	Technology selection and process level mitigation
6.2.1	Epitaxial layers
6.2.2	Silicon On insulator
6.2.3	Triple wells
6.2.4	Buried layers
6.2.5	Dry thermal oxidation
6.2.6	Implantation into oxides
7	Layout
7.2.1	Ringed or Enclosed Layout Transistor
7.2.2	Contacts and guard rings
7.2.3	Dummy transistors
7.2.4	Transistors Gate W/L ratio sizing
8	Analogue circuits
8.2.1	Node Separation and time-digitation
8.2.2	Analogue redundancy (averaging)
8.2.3	Resistive decoupling
8.2.4	Filtering
8.2.5	Modifications in bandwidth, gain, operating speed, and current drive
8.2.6	Reduction of window of vulnerability
8.2.7	Reduction of high-impedance nodes
8.2.8	Differential design
8.2.9	Dual path hardening
9	Memory cells and Embedded memory blocks
9.2.1.2	Resistive hardening
9.2.1.3	Capacitive hardening
9.2.1.4	IBM hardened memory cell
9.2.1.5	SIT hardened memory cell
9.2.1.6	DICE hardened memory cell
9.2.1.7	NASA-Whitaker hardened memory cell
9.2.1.8	NASA-Liu hardened memory cell
9.2.2	Bit-interleaving in memory arrays
9.2.3	Data scrubbing
10	Radiation-hardened ASIC libraries
10.2	RHBC Design Against Radiation Effects (DARE) library
10.3	CERN 0,25 µm radiation hardened library
10.4	BAE 0,15 µm radiation hardened library
10.5	Ramon Chips 0,18 µm and 0,13 µm radiation hardened libraries
10.6	Cobham (former Aeroflex) 600, 250, 130 and 90 nm radiation hardened libraries
10.7	Microchip Atmel MH1RT 0,35 µm and ATC18RHA 0,18 µm CMOS and ATMX150RHA 0,15 µm SOI CMOS radiation hardened libraries
10.8	ATK 0,25 µm radiation hardened cell library
10.9	ST Microelectronics CEDFPACE 65 nm radiation hardened library
10.10	RedCat Devices radiation hardened libraries
11	Digital circuits
11.2.1.2	Duplex architectures
11.2.1.3.2	Basic TMR
11.2.1.3.3	Full TMR
11.2.2.1.2	Triple Temporal Redundancy combined with spatial redundancy
11.2.2.1.3	Minimal level sensitive latch
11.2.3	Fail-safe, deadlock-free finite-state machines
11.2.4	Selective use of logic cells, clock and reset lines hardening
12	System on a chip
12.2.1.1.3	Cyclic Redundancy Check
12.2.1.1.4	BCH codes
12.2.1.1.5	Hamming codes
12.2.1.1.6	SEC-DED codes
12.2.1.1.7	Reed-Solomon codes
12.2.1.1.8	Arithmetic codes
12.2.1.1.9	Low Density Parity Codes
12.2.2	Mitigation for Memory Blocks
12.2.3	Filtering SET pulses in data paths
12.2.4	Watchdog timers
12.2.5	TMR in mixed-signal circuits
13	Field programmable gate arrays
13.2.1	Local Triple Modular Redundancy
13.2.2	Global Triple Modular Redundancy
13.2.3	Large grain Triple Modular Redundancy
13.2.4	Embedded user memory Triple Modular Redundancy
13.2.5	Additional voters in TMR data-paths to minimize DCE
13.2.6	Reliability-oriented place and Route Algorithm (RoRA)
13.2.7	Embedded processor protection
13.2.8.1.2	Full scrubbing
13.2.8.1.3	Partial scrubbing
13.2.8.1.4	Partial reconfiguration
14	Software-implemented hardware fault tolerance
14.2.1	Redundancy at instruction level
14.2.2	Redundancy at task level
14.2.3	Redundancy at application level: using a hypervisor
15	System architecture
15.2.1	Shielding
15.2.2	Watchdog timers
15.2.3	Power cycling and reset
15.2.4	Latching current limiters
15.2.5.2.2	Lockstep
15.2.5.2.3	Double-duplex
15.2.5.2.4	Double-Duplex Tolerant to Transients
15.2.5.3	Triple Modular Redundant system
15.2.6	Error Correcting Codes
15.2.7	Off-chip SET filters

… which ones were used in a few concrete examples ?

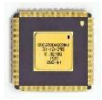
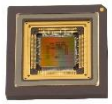
device type	ASIC				FPGA
	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)

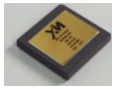


a "cocktail" of several techniques in each device

5 devices , 5 cocktails

TOTAL number of techniques used

21	12	13	14	22

	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (I&I)	Microchip Atmel (FR)	AD5 (FR)	Cobham Gaisler (SE)	Nanoxplore (FR)
	microchip name	DPC	AT697F	SCOC3	GR740	BRAVE NG-LARGE NX1H140
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech. code in ECSS-Q-HB-60-02						
6	**Technology selection and process level mitigation**					
6.2.1	Epitaxial layers	?	x	x	x	x
6.2.2	Silicon On Insulator					
6.2.3	Triple wells				x	x
6.2.4	Buried layers				deep N-well	deep N-well
6.2.5	Dry thermal oxidation					
6.2.6	Implantation into oxides					
7	**Layout**					
7.2.1	Hagen or Enclosed layout Transistor	x				?
7.2.2	Contacts and guard rings	x	x	x	x	x
7.2.3	Dummy transistors					
7.2.4	Transistors Gate W/L ratio sizing	x	x	x	x	x
8	**Analogue circuits**					
8.2.1	Node degradation and trim-digitation	?				?
8.2.2	Analogue redundancy (averaging)	?				?
8.2.3	Resistive decoupling	?				?
8.2.4	Filtering	?				?
8.2.5	Modifications in bandwidth, gain, operating speed, and current drive	?				?
8.2.6	Reduction of window of vulnerability	?				?
8.2.7	Reduction of high impedance nodes	?				?
8.2.8	Differential design	?				?
8.2.9	Dual path hardening	?				?
9	**Memory cells and Embedded memory blocks**					
9.2.1.2	Resistive hardening					
9.2.1.3	Capacitive hardening					
9.2.1.4	SRAM hardened memory cell					
9.2.1.5	HIT hardened memory cell	x				
9.2.1.6	DICE hardened memory cell		x	x	x	x
9.2.1.7	NASA Whitaker hardened memory cell					
9.2.1.8	NASA Calhardened memory cell					
9.2.2	Bit interleaving in memory arrays	?	x	x	x	?
9.2.3	Data scrubbing					
10	**Radiation-hardened ASIC libraries**	DARE180	ATC18RHA-U	ATC18RHA-U	GS65PACE	GS55PACE
10.2	IMEC Design Against Radiation Effects (DARE) library	x				
10.3	CERN 0,25 µm radiation hardened library					
10.4	BAE 0,15 µm radiation hardened library					
10.5	Ramon Chips 0,18 µm and 0,13 µm radiation hardened libraries					
10.6	Cobham (former Aeroflex) 600, 250, 130 and 90 nm radiation hardened libraries					
10.7	Microchip Atmel M-HLF 0,35 µm and ATC18RHA 0,18 µm CMOS and ATMTC65RHA 0,15 µm SOI CMOS radiation hardened libraries		x	x		
10.8	ATK 0,35 µm radiation hardened cell library					
10.9	ST Microelectronics CS55PACE 65 nm radiation hardened library				x	x
10.10	RedCat Devices radiation hardened libraries					
11	**Digital circuits**					
11.2.1.2	Duplex architectures					
11.2.1.2.2	Basic TMR				x	at pre-diffused FFs
11.2.1.3.3	Full TMR		x			
11.2.2.1.2	Triple Temporal Redundancy combined with spatial redundancy		x	?		
11.2.2.1.3	Minimal level sensitive latch					
11.2.3	Fail-safe, deadlock-free finite state machines	?		?		
11.2.4	Selective use of logic cells, clock and reset lines hardening	x	x	x	x	x
12	**System on a chip**					
12.2.1.1.3	Cyclic Redundancy Check	?				
12.2.1.1.4	BCH codes					
12.2.1.1.5	Hamming codes					
12.2.1.1.6	SEC-DED codes		x	x	x	
12.2.1.1.7	Reed-Solomon codes			x	x	
12.2.1.1.8	Arithmetic codes					
12.2.1.1.9	Low Density Parity Codes					
12.2.2	Mitigation for Memory Blocks					
12.2.3	Filtering SET pulses in data paths					
12.2.4	Watchdog timers		x	x	x	
12.2.5	TMR in mixed-signal circuits	?				
13	**Field programmable gate arrays**					
13.2.1	Local Triple Modular Redundancy					
13.2.2	Global Triple Modular Redundancy					
13.2.3	Large grain Triple Modular Redundancy					
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13.2.5	Additional voters in TMR data-paths to minimise DCE					
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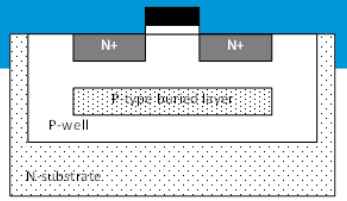
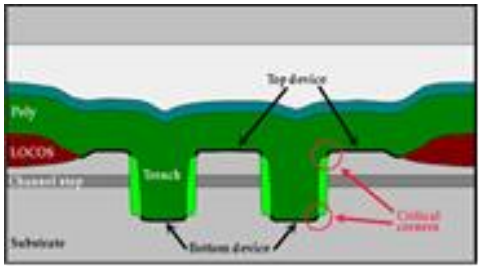
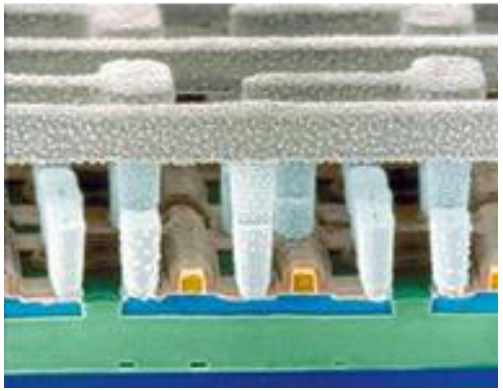
13.2.8.1.2	Full scrubbing					CMIC
13.2.8.1.3	Partial scrubbing					
13.2.8.1.4	Partial reconfiguration					

6 Technology selection and process level mitigation



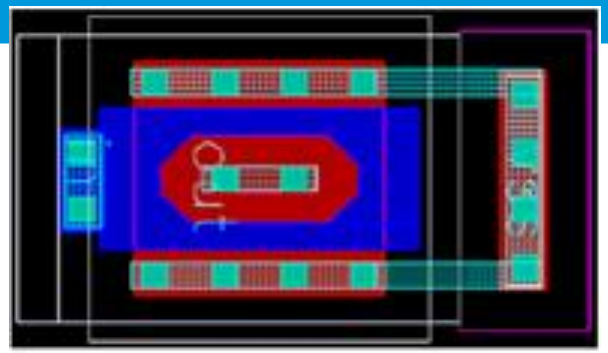


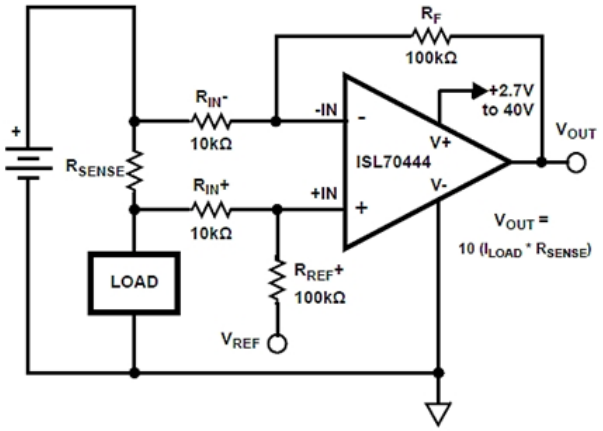


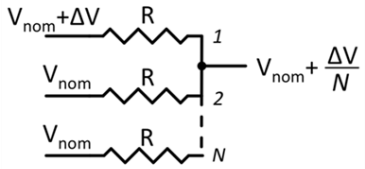
Process level, examples

	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
6	**Technology selection and process level mitigation**					
6.2.1	Epitaxial layers	**?**	**x**	**x**	**x**	**x**
6.2.2	Silicon On Insulator					
6.2.3	Triple wells				**x**	**x**
6.2.4	Buried layers				**deep N-well**	**deep N-well**
6.2.5	Dry thermal oxidation					
6.2.6	Implantation into oxides					

7 Layout, 8 Analogue circuits







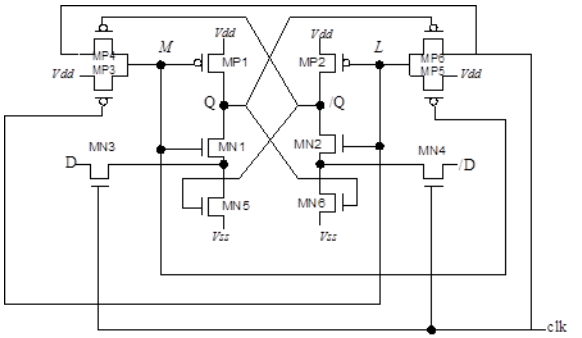
Layout level, examples

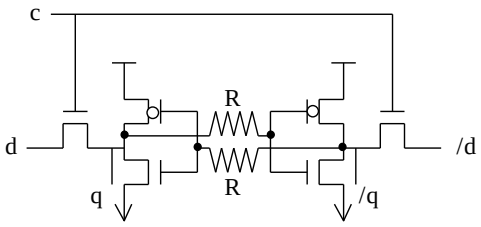
	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
7	**Layout**					
7.2.1	Ringed or Enclosed Layout Transistor	x				?
7.2.2	Contacts and guard rings	x	x	x	x	x
7.2.3	Dummy transistors					
7.2.4	Transistors Gate W/L ratio sizing	x	x	x	x	x

Analogue circuits level, examples

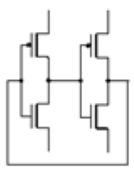
		ASIC				FPGA
	device type	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
8	**Analogue circuits**					
8.2.1	Node Separation and Inter-digitation	?				?
8.2.2	Analogue redundancy (averaging)	?				?
8.2.3	Resistive decoupling	?				?
8.2.4	Filtering	?				?
8.2.5	Modifications in bandwidth, gain, operating speed, and current drive	?				?
8.2.6	Reduction of window of vulnerability	?				?
8.2.7	Reduction of high impedance nodes	?				?
8.2.8	Differential design	?				?
8.2.9	Dual path hardening	?				?

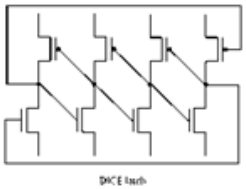
9 Embedded memories

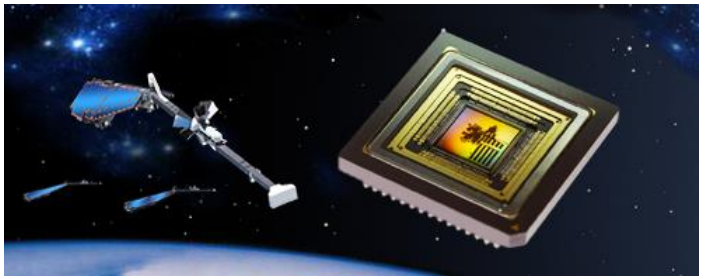




10 Radiation-hardened ASIC libraries





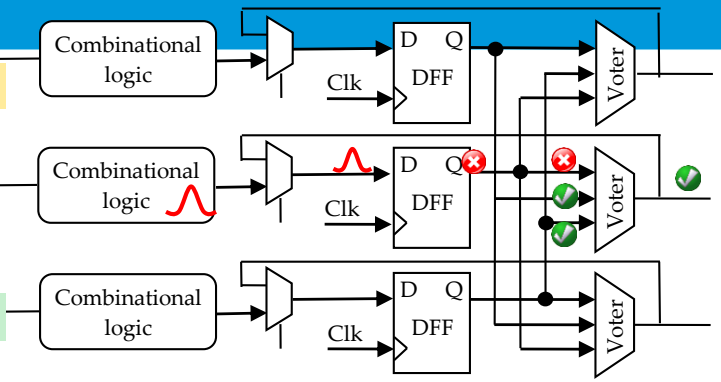


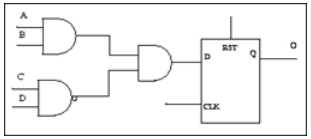
Memory cells, embedded memory blocks and rad-hard libraries level, examples

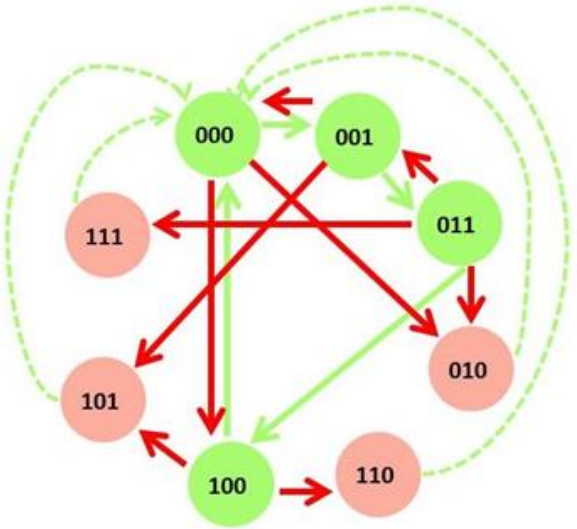
	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
9	**Memory cells and Embedded memory blocks**					
9.2.1.2	Resistive hardening					
9.2.1.3	Capacitive hardening					
9.2.1.4	IBM hardened memory cell					
9.2.1.5	HIT hardened memory cell	x				
9.2.1.6	DICE hardened memory cell		x	x	x	x
9.2.1.7	NASA-Whitaker hardened memory cell					
9.2.1.8	NASA-Liu hardened memory cell					
9.2.2	Bit-interleaving in memory arrays	?	x	x	x	?
9.2.3	Data scrubbing					
10	**Radiation-hardened ASIC libraries**	**DARE180**	**ATC18RHA-U**	**ATC18RHA-U**	**C65SPACE**	**C65SPACE**

11 Digital Circuits

b)



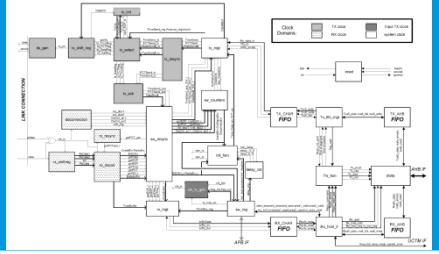


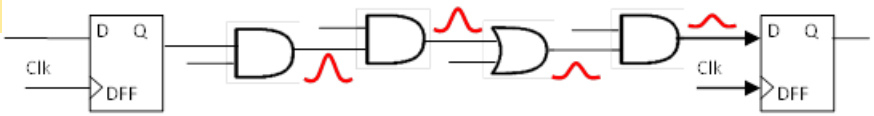


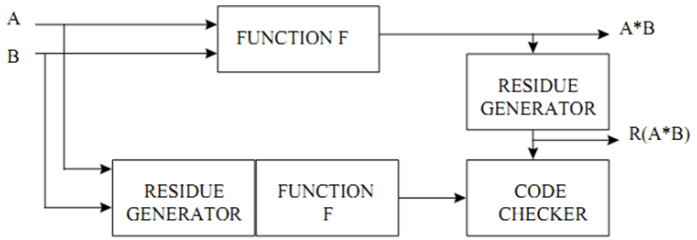
Digital circuits, examples

		ASIC				FPGA
	device type	multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
11	**Digital circuits**					
11.2.1.2	Duplex architectures					
11.2.1.3.2	Basic TMR				x	at pre-diffused FFs
11.2.1.3.3	Full TMR		x			
11.2.2.1.2	Triple Temporal Redundancy combined with spatial redundancy		x	?		
11.2.2.1.3	Minimal level sensitive latch					
11.2.3	Fail-safe, deadlock-free finite state machines	?		?		
11.2.4	Selective use of logic cells, clock and reset lines hardening	x	x	x	x	x

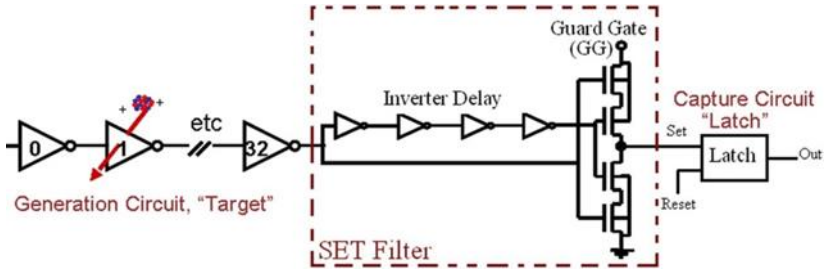
12 System on a Chip







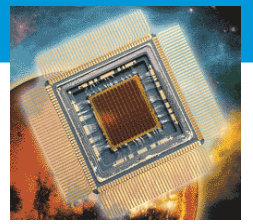
7 bits of data	Number of "1"	8-bits including parity bit	
		even	odd
000 0000	0	**0**000 0000	**1**000 0000
101 0001	3	**1**101 0001	**0**101 0001
110 1001	4	**0**110 1001	**1**110 1001
111 1111	7	**1**111 1111	**0**111 1111

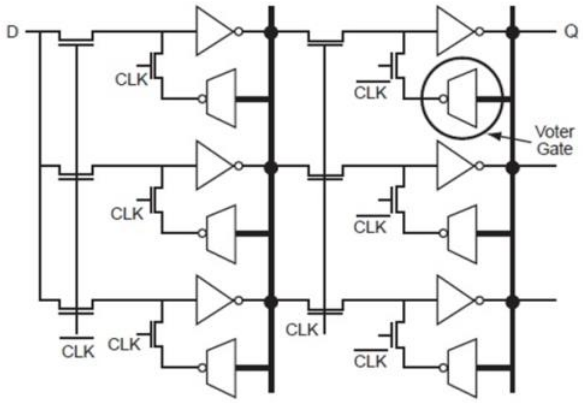


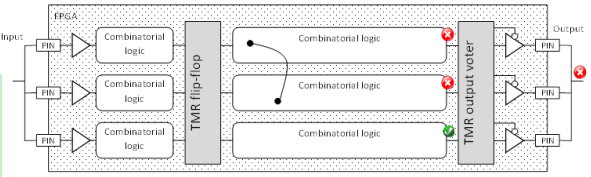
System-on-a-Chip level, examples

	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
12	**System on a chip**					
12.2.1.1.3	Cyclic Redundancy Check	?				
12.2.1.1.4	BCH codes					
12.2.1.1.5	Hamming codes					
12.2.1.1.6	SEC-DED codes		x	x	x	
12.2.1.1.7	Reed-Solomon codes			x	x	
12.2.1.1.8	Arithmetic codes					
12.2.1.1.9	Low Density Parity Codes					
12.2.2	Mitigation for Memory Blocks					
12.2.3	Filtering SET pulses in data paths					
12.2.4	Watchdog timers		x	x	x	
12.2.5	TMR in mixed-signal circuits	?				

13 Field Programmable Gate Arrays



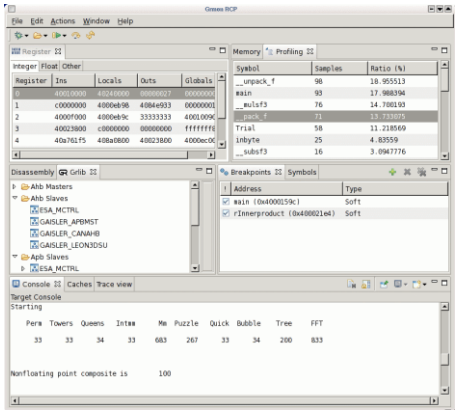


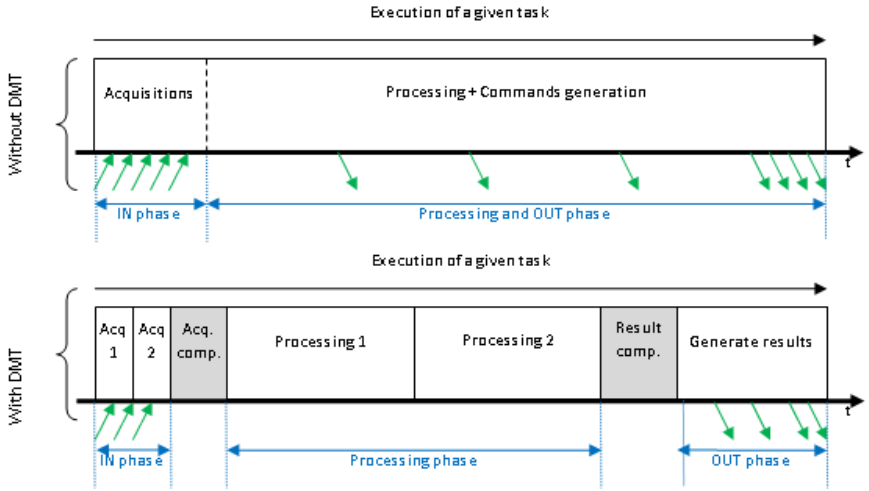


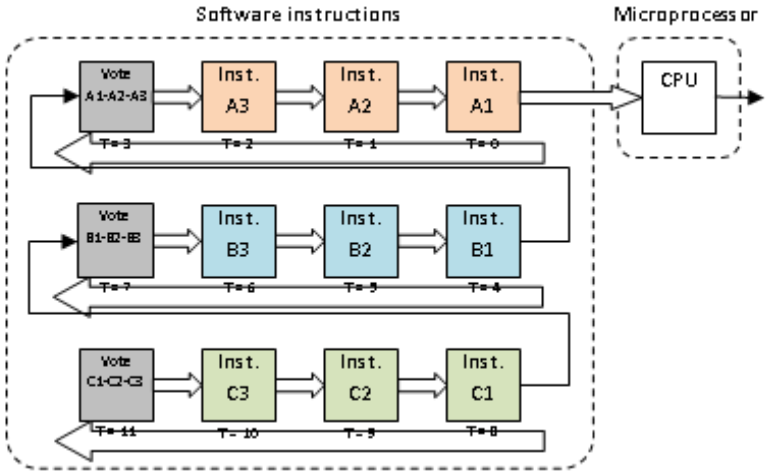
FPGA level, examples

	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
13	**Field programmable gate arrays**					
13.2.1	Local Triple Modular Redundancy					
13.2.2	Global Triple Modular Redundancy					
13.2.3	Large grain Triple Modular Redundancy					
13.2.4	Embedded user memory Triple Modular Redundancy					
13.2.5	Additional voters in TMR data-paths to minimise DCE					
13.2.6	Reliability-oriented place and Route Algorithm (RoRA)					
13.2.7	Embedded processor protection					
13.2.8.1.2	Full scrubbing					**CMIC**
13.2.8.1.3	Partial scrubbing					
13.2.8.1.4	Partial reconfiguration					

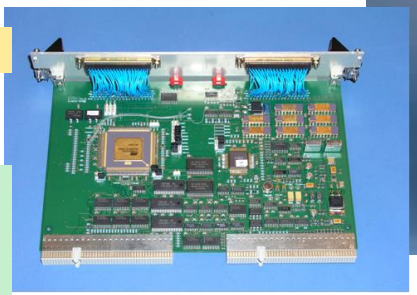
14 Software-implemented hardware fault tolerance

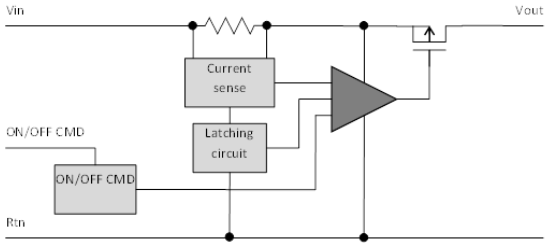


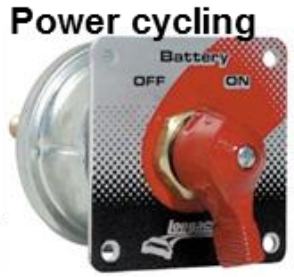


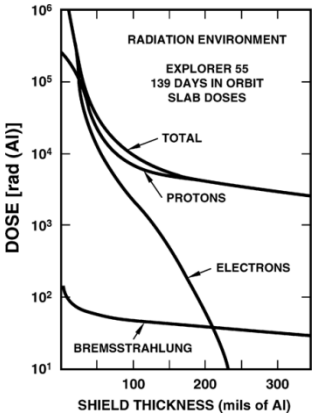


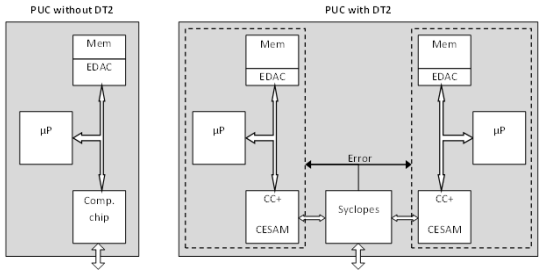
15 System architecture (off-chip)











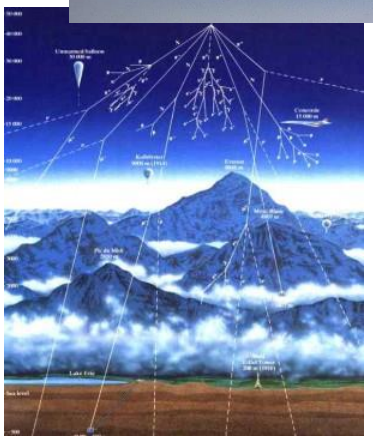
SW and system (off-chip) level, examples

	device type	ASIC				FPGA
		multi-core microcontroller	mono-core microprocessor	multi-core SoC ASIC	multi-core microprocessor	blank FPGA
	vendor or owner	TAS (BE)	Microchip Atmel (FR)	ADS (FR)	Cobham Gaisler (SE)	NanoXplore (FR)
	microchip name	**DPC**	**AT697F**	**SCOC3**	**GR740**	**BRAVE NG-LARGE NX1H140**
	microchip technology	UMC 180nm	Atmel 180nm	Atmel 180nm	ST 65nm	ST 65nm (SRAM-based config)
Mitigation Tech code in ECSS-Q-HB-60-02						
14	**Software-implemented hardware fault tolerance**					
14.2.1	Redundancy at instruction level					
14.2.2	Redundancy at task level					
14.2.3	Redundancy at application level: using a hypervisor					
15	**System architecture**					
15.2.1	Shielding					
15.2.2	Watchdog timers					
15.2.3	Power cycling and reset					
15.2.4	Latching current limiters					
15.2.5.2.2	Lockstep					
15.2.5.2.3	Double duplex					
15.2.5.2.4	Double Duplex Tolerant to Transients					
15.2.5.3	Triple Modular Redundant system					
15.2.6	Error Correcting Codes					
15.2.7	Off-chip SET filters					

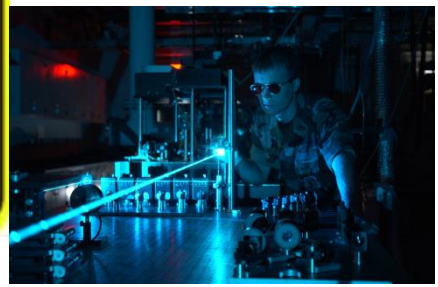
TMR variants in this Handbook

Type of TMR	11 – Digital Circuits	12 - SoC	13 - FPGA	15 – Off-chip		3x flip flops	3x combinatorial logic	3x voter	Extra voters in data paths	Triplets physical layout separated	3x memory blocks	comparing analog signals	3x chip	Synchronizing logic	3x outputs
Basic TMR	x					x									
Full TMR	x					x	x	x							
Local TMR			x			x									
Global TMR			x			x	x	x							x
Large grain TMR			x			x	x	x		x					x
Embedded memory TMR			x								x				
TMR with **voters against DCE**			x			x	x	x	x						
Mixed-signal TMR		x										x			
Chip-level TMR				x									x	x	

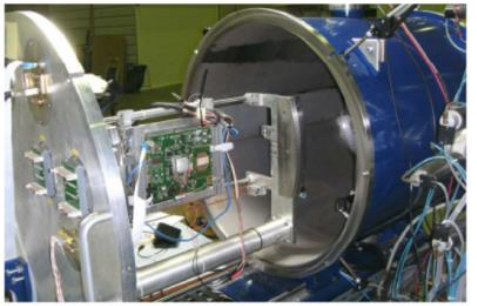
16 Validation methods (1/2)



16 Validation methods (2/2)



- ***Radiation Facilities in use by ESA*** https://escies.org/ReadArticle?docId=230
  - Co-60 at ESA/ESTEC, Netherlands (total dose)
  - Californium-252 at ESA/ESTEC, Netherlands
  - Paul Scherrer Institut (PSI), Switzerland: proton irradiation
  - Louvain la Neuve (UCL), Belgium: heavy ions and protons
  - Jyväskylä University, Finland: heavy ions and protons



A few remarks and reminders

The ECSS-Q-HB-60-02 WG chose to group and name 78 techniques in 10 "LEVELS" , mainly according to WHO maybe applying or choosing the techniques, depending on role of the person involved in the chip selection or design or manufacturing or programming or integration on system phases

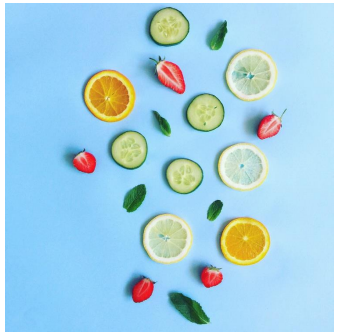
but

There are of course many other ways to classify and present this information

A few remarks and reminders

Unfortunately, there is **no universal recipe** nor cookbook (flowchart) to guide you to decide which mitigation cocktail is best for your ASIC or FPGA.

many variables: radiation environment expected, what radiation sensitivity is tolerable by the system using the chip, costs of applying mitigation, experience applying mitigation, project costs and timing constraints…



A few conclusions and reminders

Sometimes **LESS can be BETTER**: Every technique has a cost associated (power, speed, area, time and manpower resources to apply and test it…) . Too many overlapping techniques can raise overall chip sensitivity: more logic elements can introduce more radiation sensitive areas or parasitic devices, which can cause additional or new unwanted radiation effects