Modeling of SET Generation in Standard CMOS Logic Gates

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Single Event Transients (SETs), originating in combinational logic as a result of the passage of energetic particles, represent nowadays a serious reliability issue for electronics operating under radiation exposure. In that regard, analysis of the SET generation and propagation effects in combinational logic is an important step in the rad-hard design flow. To facilitate accurate and fast SET evaluation, the SET generation and propagation models based on analytical formulations or look-up tables are used. In this work, the modeling of the SET generation effects in standard combinational logic gates designed in 130 nm CMOS process is addressed. The models for the two main parameters of SET generation (critical charge and SET pulse width) are introduced. The proposed models are derived through the conventional current-injection approach in SPICE simulations, and they provide advancement over the state-of-the-art models by considering important aspects that have been neglected in existing models.

The critical charge models are used to predict the minimum induced charge required to cause the SET glitch at the output of a logic gate. A number of critical charge models have been proposed in literature [1 – 3]. However, existing models have some important shortcomings such as: (a) some models do not consider all relevant parameters (e.g. load and temperature), (b) some models depend on technology-related parameters which are often not readily available to designers. As alternative to existing models, we introduce a model based on the linear superposition principle, i.e. the critical charge Q_{CRIT} is expressed as a sum of contributing components. The proposed model was derived from SPICE simulations with the double-exponential current source, and considers the dependence of Q_{CRIT} on 6 parameters: size factor of target gate S_T, size factor of load gate S_L, interconnection capacitance C_W, supply voltage V_{DD}, temperature T_{EMP} and width of the injected current pulse T_{PULSE}. A general form of the model is,

$$Q_{CRIT} = f(S_T, S_L, C_W, V_{DD}, T_{EMP}, T_{PULSE}) = Q_{NOMINAL} + \sum_{i=1}^{6} Q_i \tag{1}$$

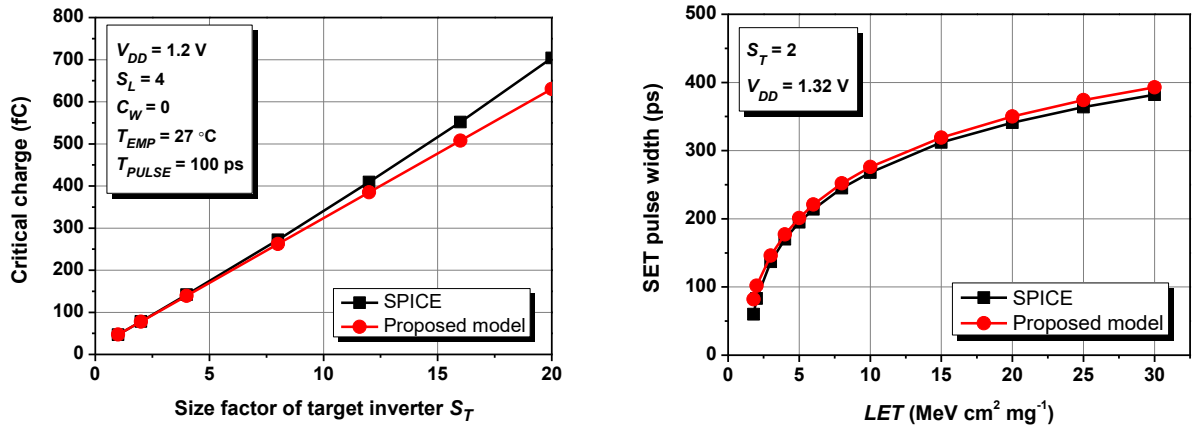
In (1), $Q_{NOMINAL}$ denotes the critical charge value for nominal values of model parameters (S_T, S_L, C_W, V_{DD}, T_{EMP} and T_{PULSE}). The terms Q_i are linear functions representing the contribution of 6 considered parameters when their values increase or decrease beyond the nominal values.

As the critical charge gives only the information on the circuit node's robustness to direct particle strikes, the knowledge of the SET pulse width is required to estimate the probability that a generated SET pulse will propagate through the circuit and eventually cause a soft error. Most available SET pulse width models have been derived using the double-exponential current source as a SET current model [4 – 7]. Although the double-exponential current model may be sufficient for initial estimation of Q_{CRIT}, its inherent limitations lead to inaccurate prediction of the SET pulse width. Recently, a SET pulse width model considering the bias-dependence of the induced current pulse has been proposed [8], but this model requires extensive TCAD simulations before it can be applied to a given circuit. In contrast to existing models, we propose a simple SET pulse width model derived from the current injection in SPICE using the bias-dependent current source proposed by Kaupilla *et al.* [9]. The model expresses the SET pulse width in terms of particle's *LET*, drive strength of target gate S_T and supply voltage V_{DD},

$$T_{SET} = f(LET, S_T, V_{DD}) = \begin{cases} f_a(LET) \pm f_b(V_{DD}), & S_T = 1 \\ f_a\left(\frac{LET}{n}\right) \pm f_b(V_{DD}), & S_T = n > 1 \end{cases} \tag{2}$$

Extensive evaluation of the proposed models' accuracy with respect to SPICE results has been conducted, and a representative sample of results obtained for inverter designed in IHP's 130 nm CMOS technology is illustrated in

Figure 1. The proposed critical charge model provides very good accuracy (better than 90 %) for lower driving strengths of the target gate but the accuracy is lower for higher driving strengths. To resolve this issue, we intend to implement an error function for compensating the relative error. On the other side, the proposed SET pulse width model provides very good accuracy (better than 90 %) for higher values of LET but the relative error compared to SPICE results is higher for low LETs (LET < 2 MeV cm^2 mg^{-1}). This can be attributed to the linear modeling applied in (2), and this issue is currently under investigation. Overall, the proposed models can be very useful for initial estimation of the SET generation effects in standard combinational gates. With improved accuracy, the models can be integrated into a design flow for automated estimation of the soft error rate (SER) of complex logic gates.



(a) (b)

Figure 1: Comparison of proposed models with SPICE: (a) critical charge model vs. SPICE, (b) SET pulse width model vs. SPICE

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