Modeling of SET Generation in Standard CMOS Logic Gates

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MOTIVATION

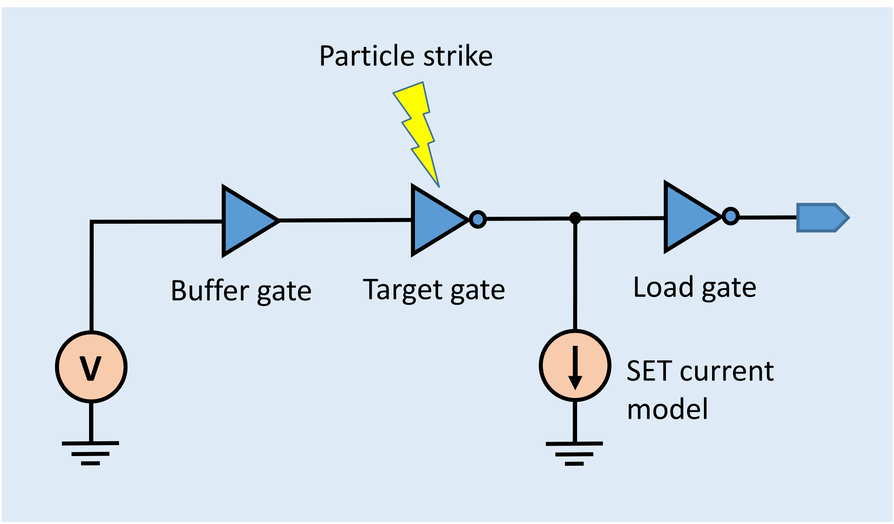
- With the technological downscaling, the Single Event Transients (SETs) are becoming a major reliability issue in modern CMOS technologies employed in space applications
- For rad-hard design automation, accurate models for SET generation effects are required
- Existing models for SET generation have crucial shortcomings:
  - *Critical charge models do not consider all relevant parameters (e.g. load and temperature) or require the knowledge of some process parameters*
  - *Most SET pulse width models are based on double-exponential current source which is inaccurate for SET pulse width estimation*
- **It is required to establish more accurate models for analysis of SET generation in standard combinational cells**

GOALS

- To address the limitations of existing models by establishing more accurate circuit-level SET generation models for:
  - ***Critical charge (minimum charge causing a SET)***
  - ***SET pulse width (width of generated SET voltage pulse)***
- To consider the combined impact of all relevant parameters:
  - *Drive strength of target gate (S_T)*
  - *Drive strength of load gate (S_L)*
  - *Capacitance of interconnections (C_W)*
  - *Supply voltage (V_{DD})*
  - *Temperature (T_{EMP})*
  - *SET current pulse width (T_{PULSE})*
  - *Input logic levels*
- The proposed models have been derived from SPICE simulations

APPROACH

- Analysis based on current injection in SPICE simulations, using Cadence Virtuoso
- SET was modeled with a current source connected at the output of target gate
- Dependence of critical charge and SET pulse width on design and operating parameters was investigated
- Standard logic gates in IHP's 130 nm CMOS technology were analyzed
- Critical charge analysis:
  - **Double-exponential current source** was used as SET current model
- SET pulse width analysis:
  - **Bias-dependent current source** was used as SET current model (*J. Kauppila et al., IEEE TNS, 2009*)

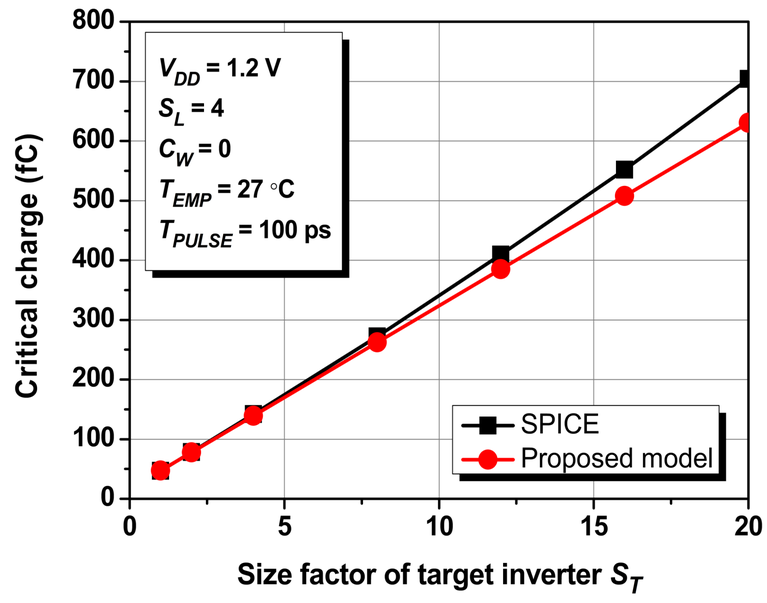


CRITICAL CHARGE MODEL

- A critical charge (Q_{CRIT}) model based on linear superposition principle is proposed
- Q_{CRIT} in terms of S_T, S_L, C_W, V_{DD}, T_{EMP}, and T_{PULSE}
- Relative error compared to SPICE is below 10 %
- Model has been verified for common standard logic gates (INV, BUF, AND, NAND, OR, NOR, XOR, XNOR)
- Open issues:
  - Nonlinearities for high driving strengths of target gate, resulting in high relative error
- Proposed critical charge model:

$$Q_{CRIT} = Q_{NOMINAL} + \sum_{i=1}^{6} Q_i$$

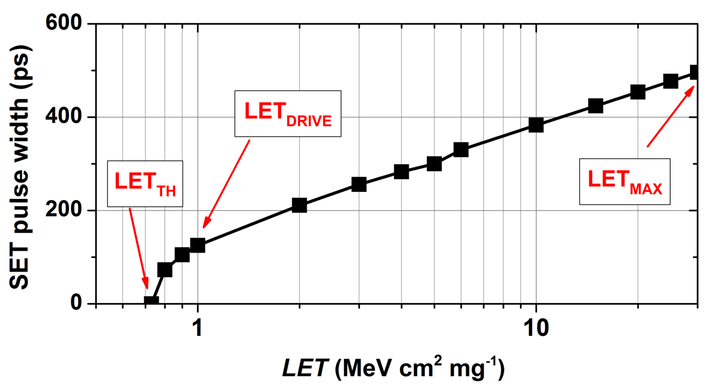
- $Q_{NOMINAL}$ is the value of Q_{CRIT} when all parameters are at nominal values
- Q_i defines the increase or decrease of Q_{CRIT} due to the variation of *i-th* parameter

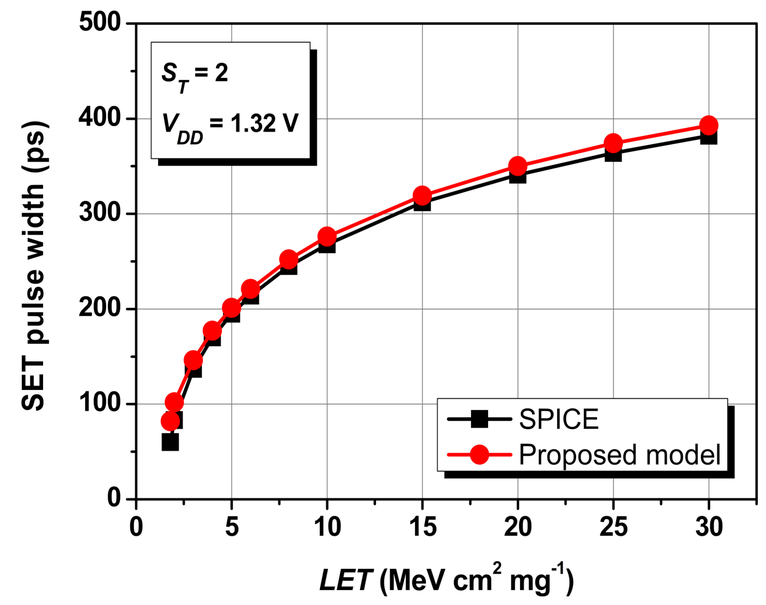


SET PULSE WIDTH MODEL

- A SET pulse width model considering the bias-dependence of the SET current pulse is proposed
- T_{SET} in terms of S_T, V_{DD} and LET
- Relative error with respect to SPICE is below 8 % for LET > 2 MeV cm^2 mg^{-1}
- Model has been verified for inverter
- Open issues:
  - Extension of model to include the impact of other relevant parameters
  - Verification of proposed model with other standard logic gates
- Proposed SET pulse width model:

$$T_{SET} = f_a\left(\frac{LET}{S_T}\right) + f_b(V_{DD})$$





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DFG Deutsche Forschungsgemeinschaft

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