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ESA/ESTEC

Book of Abstracts

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ADC12DJ3200QML-SP SEE Radiation Testing Results

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The ADC12DJ3200QML is an RF-sampling giga-sample ADC that can directly sample input frequencies from DC to above 10 GHz. In dual channel mode, ADC12DJ3200 can sample up to 3200-MSPS and in single channel mode up to 6400-MSPS. Programmable tradeoffs in channel count (dual channel mode) and Nyquist bandwidth (single channel mode) allow development of flexible hardware that meets the needs of both high channel count and wide instantaneous signal bandwidth applications. Full power input bandwidth (-3 dB) of 7.0 GHz, with usable frequencies exceeding the -3 dB point in both dual and single channel modes, allows direct RF sampling of L-band, S-band, C-band and X-band for frequency agile systems.

ADC12DJ3200 uses a high speed JESD204B output interface with up to 16 serialized lanes and subclass-1 compliance for deterministic latency and multi-device synchronization. The serial output lanes support up to 12.8 Gbps and can be configured to trade-off bit rate and number of lanes. Innovative synchronization features, including noiseless aperture delay (TAD) adjustment and SYSREF windowing, simplify system design for phased array radar and MIMO communications. Optional digital down converters (DDCs) in dual channel mode allow for reduction in interface rate (real and complex decimation modes) and digital mixing of the signal (complex decimation modes only).

The ADC12DJ3200QML was put through heavy ion testing using the TAMU 15 MeV K500 Cyclotron. The device was monitored for Single Event Latch-up (SEL), Single Event Functional Interrupt (SEFI) and Single Event Upset (SEU).

A summary of the testing is as follows:
• The ADC's JESD204B link always self-recovers from radiation events and without user intervention.
• The ADC exhibits no functional interrupts (SEFI) or performance degradations under the beam.
• No user-programmable or fuse-backed device registers are corrupted under the beam.
• Calibration vectors are not corrupted under the beam while running in either foreground or background calibration modes.
• The ADC12DJ3200 does not exhibit SEL beyond an LET of 120 MeV cm^2 / mg using datasheet maximum supply voltages and Tj = 125C.
• The total ionizing dose (TID) rating of the ADC12DJ3200 is 300 krad(Si).

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Accurate Abstraction and High Level Modeling and Validation of SEE in Electronic Systems

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In this talk, we will be discussed the practical use of formal based techniques, such as SAT, SMT and probabilistic model checker to analyze SEEs at logical and higher abstraction levels. Through examples, we will illustrate each approach and its benefits.

COTS / **46**

Analysis and Design Techniques for Reconfigurable System Reliability in Harsh Environments

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ABSTRACT - SRAM-based Field Programmable Gate Arrays (FPGAs) in Aerospace Applications are increasingly attractive for their high integration and reprogrammability but their configuration memory still suffers of and high radiation sensitivity and still requires long time to be reconfigured in-flight. Thus, dependability and performability of such systems are major concerns in safety-critical and mission-critical applications. The in-depth knowledge of low-level resources implementation is a key point to develop more reliable and efficient systems.

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Atmospheric radiation

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Automotive safety challenges based on AEC Q100 / ISO 26262 requirement

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COTS / **31**

COTS in Space: Constraints, Limitations and Disruptive Capability

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This talk describes one application of CNES methodology for allowing using commercial (COTS) digital electronic components in large spacecrafts. The required steps the components have to successfully pass before to be authorized to fly are presented. Then, the limitation concerning COTS

usable performance is outlined. Even if these specificities reduce the attractiveness of commercial components, several project configurations are highlighted where COTS components are feasibility factor for the space mission due to their contribution to system performance.

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COTS in Space: Experience and lessons learned at ESA

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COTS / 32

COTS in Space: Qualified commercial components for space

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Commercial electronics compared to their space qualified counterparts are increasingly proving to be fit for use in space. High performance and reliability together with reduction of qualification costs and less testing time play an important role in the development of the space market. Space-COTS are commercial components qualified for small satellite missions, which support the NewSpace technology development.

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COTS on ground: Ultra-High energies radiation test facilities

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Coffee and posters

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Concluding remarks

Authors: Raoul Velazco[1]; Gregoire Deprez[2]; Christian POIVEY[2]; Veronique Ferlet-Cavrois[2]; Agustin Fernandez-Leon[2]; Ali Zadeh[2]; Jaime Estela[3]

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Mitigation and Hardening / 28

Development of a Hardened 150nm Standard Cell library

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The effects produced by radiation on integrated circuits can be classified into Single Event Effects (SEE) related to transient problems and Total Ionization Dose (TID) effects that arise due to the long exposure time ionizing radiation. The mitigation of these effects on integrated circuits can be done in three ways: Manufacturing Process Level, Architectural Level (redundancy) and Layout Level. The work presented here deals with the third way of mitigation, that is, the cell library design of radiation tolerant integrated circuits. Designed and manufactured in silicon on 150nm technology, the SMDH-RH library is based on the use of guard rings and the application of closed geometry techniques (ELT – Enclosed Layout Transistor). The library includes simple and complex digital logic gates. It was tested in space as payload of a nanosatellite (NanosatC-Br1), launched in space in 2014 and still in activity, being approved its operation and functionality.

Radiation effects (SEE, TID, TNID) / 42

Development of device for testing electronics in radiation harsh environment using Timepix detectors

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Single Event Effects (SEE), caused generally by single energetic particles, pose an important issue when implementing electronics in a harsh radiation environment. In this work, we present an electronic system for measuring SEEs timely and spatially correlated with Timepix detectors. The Timepix detector is a semiconductor pixel detector, which contains 256 x 256 pixels. It provides energy or time information for each hit pixel. Our experimental setup consists of FPGA based board synchronized with Timepix readout (Timepix and spectrometer readout interface) and a replaceable Device Under Test (DUT), which can consists of various type of circuits, including D flip-flops, Random Access Memory (RAMs), or Field Programmable Gate Arrays (FPGAs).

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Development of read-out interfaces for pixel particle detector Timepix

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Development of read-out interfaces dedicated for the advanced hybrid radiation pixel detector Timepix will be presented. A basic concept and importance of a read-out interface as an absolutely necessary supporting electronics for proper operation and exploitation of the radiation detector Timepix and its advanced features will be explained. Then several application specific variants of read-out interfaces will be demonstrated (e.g. small size portable device, stand alone remotely controlled device, harsh radiation environment operated device, vacuum operated device, educational kit or space environment radiation monitor…) and fulfillment of diverse requirements on the design of each variant will be discussed.

Space and atmospheric environments / 40

Development of the MIRAM radiation monitor

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Concept, purpose and functionality of the highly miniaturized radiation monitor (MIRAM) will be presented. The monitor is a specialized device with purpose of radiation field monitoring-characterization and online composition recognition with purpose to be deployed and operated on the earth orbit satellites. The device is currently being developed for ESA-ESTEC institution. Design has to meet a set of strict requirements on low power consumption, small weight, low-particle recognition, long term stability and precision of measurements and also radiation hardness. The device is based on hybrid semiconductor pixel detector Timepix3 (256x256 pixels with TOT and TOA information) with single particle recognition capability accompanied with single pad diodes of different materials to optimize energy range resolution.

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EEE Parts in the New Space Paradigm

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As the space business rapidly evolves to accommodate a lower cost model of development and operation via concepts such as commercial space and small spacecraft (aka, CubeSats and swarms), traditional EEE parts screening and qualification methods are being scrutinized under a risk reward trade space. In this presentation, two basic concepts will be discussed: The movement from complete risk aversion EEE parts methods to managing and/or accepting risk
via alternate approaches; and discussion of emerging assurance methods to reduce overdesign as well emerging model based mission assurance (MBMA) concepts. Example scenarios will be described as well as consideration for trading traditional versus alternate methods.

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ESTEC High Bay and test rooms visit

Tests and simulations / **21**

Error-rate Prediction for Programmable Circuits: Methodology, Tools and Studied Cases

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This presentation describes a method devoted to SEU error-rate prediction for processor-based architectures. The proposed method combines results issued from fault-injection, performed at circuit by means of CEU (Code Emulated Upsets), to those issued from radiation ground tests. It allows predicting error rates without requiring radiation ground-tests for future applications. The approach was successfully applied to processors and FPGAs and is illustrated by three representative case-studies.

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Fault Injection Methodologies

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Fault injection is a widely used method to evaluate fault effects and error mitigation in a design. While not a replacement for standard Radiation- Hardness Assurance methodologies, it can provide valuable information in a quick and inexpensive manner. Moreover, recent developments have improved performance by several orders of magnitude, thus enabling the realization of extremely large fault injection campaigns. Today, fault injection can be used to forecast the expected circuit behaviour in the occurrence of SEUs and SETs, validate error mitigation approaches and detect weak areas that require error mitigation. This talk will review the most relevant fault injection methods, covering software-based techniques, simulation techniques and FPGA-based emulation techniques. Recent advances for SET and MCU emulation will also be presented.

Tests and simulations / **27**

Laser Testing: Laser Simulation Test Possibilities and Facilities

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Carrier generation induced by pulsed-laser excitation has become an essential tool for the investigation of single-event effects (SEEs) of micro- and nano-electronic structures. The qualitative capabilities of this approach include, among others, sensitive node identification, radiation hardened circuit verification, basic mechanisms investigations, model validation and calibration, screening devices for space missions, and fault injection to understand error propagation in complex circuits. Recent effort has built upon the success enabled by these qualitative benefits, and has focused on putting the laser SEE approaches on a more quantitative basis. This presentation will present the basic physics associated with the single-photon and two-photon excitation processes, as well as numerous case studies.

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Measurements using novel monolithic pixel radiation detectors

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The presented radiation detection device X-CHIP-03 is a monolithic silicon detection chip based on 180 nm SoI technology. The chip consists of square pixel cells with a 60 μm pitch forming an array of 64 x 64 pixels covering an active surface of 3.84 x 3.84 mm^2. X-CHIP-03 has two operation modes – hit counting mode and ADC mode dedicated to the measurement of deposited energy in pixels.

Among other applications, X-CHIP-03 serves as a technology demonstrator for the SpacePix ASIC, which will be a key component of SpacePix Radiation Monitor (SXRM) - a new detector designed for space dosimetry with wide dynamic range and logarithmic amplifier.

One of the requirements to meet such a challenging task is a disponibility of sufficient SEU tolerance. For the evaluation of SEU cross-section of X-CHIP03, data from irradiation by protons and various ions (helium, carbon, xenon, argon, neon) were used.

Besides SEU measurement, a response to radionuclide sources of ^{55}Fe and ^{238}Pu was evaluated to demonstrate the universality of X-CHIP-03 usage.

Tests and simulations / **22**

Microprocessor testing: characterization tests, mitigation

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Most satellites use radiation-hardened microprocessors, as many organizations are concerned that a microprocessor failure could be catastrophic to the mission. Most radiation hardened microprocessors are not as capable as commercial microprocessors, and the instrument's performance might

be affected by the microprocessor's capability. Commercial microprocessors can be useful for secondary, non-mission computations so that the radiation-hardened microprocessor has more capacity for mission critical processing. Qualifying a commercial microprocessor for space usage can be quite complicated, though. This talk will highlight methods for characterizing microprocessors for SEE failures, methods for mitigating microprocessors, and open questions regarding microprocessor resilience. The talk includes a short introduction to computer architecture for several types of microprocessors.

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Mitigation in ASICs and FPGAs

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Radiation effects (SEE, TID, TNID) / 41

Modeling of SET Generation in Standard CMOS Logic Gates

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Single Event Transients (SETs), originating in combinational logic as a result of the passage of energetic particles, represent nowadays a serious reliability issue for electronics operating under radiation exposure. In that regard, analysis of the SET generation and propagation effects in combinational logic is an important step in the rad-hard design. To enable efficient SET evaluation, the SET generation and propagation models based on analytical formulations or look-up tables are used. In this work, the modeling of the SET generation effects in standard combinational logic gates designed in 130 nm CMOS process from IHP is addressed. The models for the two main parameters of SET generation (critical charge and SET pulse width) are introduced. The proposed models are derived through the conventional current-injection approach in SPICE simulations, and they provide advancement over the state-of-the-art models by considering important aspects that have been neglected in existing models.

The critical charge models are used to predict the minimum induced charge required to cause the SET voltage glitch at the output of a logic gate. A number of critical charge models have been proposed in literature. However, existing models have some important shortcomings such as: (a) some models do not consider all relevant parameters (e.g. load and temperature), (b) some models depend on technology-related parameters which are often not readily available to designers. As alternative to existing models, we introduce a model based on the linear superposition principle, i.e. the critical charge QCRIT is expressed as a sum of contributing components. The proposed model was derived from SPICE simulations with the double-exponential current source, and considers the dependence of QCRIT on 6 parameters: size factor of target gate ST, size factor of load gate SL, interconnection capacitance CW, supply voltage VDD, temperature TEMP and width of the injected current pulse TPULSE.

As the critical charge gives only the information on the circuit node's robustness to direct particle strikes, the knowledge of the SET voltage pulse width is required to estimate the probability that a generated SET voltage pulse will eventually cause a soft error. Most available SET pulse width models have been derived using the double-exponential current source as a SET current model. Although the double-exponential current model is useful for initial estimation of QCRIT, its inherent limitations lead to inaccurate prediction of the SET pulse width. Recently, a SET pulse width model considering the bias-dependence of the induced current pulse has been proposed by T. R. Assis et al. (IEEE IRPS, 2016), but this model requires extensive calibration with TCAD simulations. In contrast

to existing models, we propose a simple SET pulse width model derived from the current injection in SPICE using the bias-dependent current source proposed by J. S. Kauppila et al. (IEEE TNS, 2009). The proposed model expresses the SET pulse width in terms of particle's LET, drive strength of target gate ST and supply voltage VDD.
Extensive evaluation of the proposed models' accuracy with respect to SPICE results has been conducted. The proposed critical charge model provides very good accuracy (better than 90 %) for lower driving strengths of the target gate but the accuracy is lower for higher driving strengths. To resolve this issue, we intend to implement an error function for compensating the relative error. On the other side, the proposed SET pulse width model provides very good accuracy (better than 90 %) for higher values of LET but the relative error is higher for low LETs (LET < 2 MeV cm2 mg-1). This issue is currently under investigation. Overall, the proposed models can be very useful for initial estimation of the SET generation effects in standard combinational gates. With improved accuracy, the models can be integrated into a design flow for automated estimation of the soft error rate (SER) of complex logic circuits.

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Multi and Many core Processors: Fault tolerance and Radiation tests

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This work evaluates the SEE static and dynamic sensitivity of a single-chip many-core processor having implemented 16 compute clusters, each one with 16 processing cores. A comparison of the dynamic tests when processing-cores cache memories are enabled and disabled is presented. The experiments were validated through radiation ground testing performed with 14 MeV neutrons on the MPPA-256 many-core processor manufactured in TSMC CMOS 28HP technology.

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New Developments in FPGA: SEUs and Fail-Safe Strategies

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Technology is changing at a fast pace. Transistor geometries are getting smaller, voltage thresholds are getting lower, design complexity is exponentially increasing, and user options are expanding. Consequently, reliable insertion of error detection and correction (EDAC) circuitry has become relatively challenging. As a response, a variety of mitigation techniques are being implemented. They range from weaker EDAC circuits that save area and power to strong mitigation strategies that come as a great expense to the system. Regarding FPGA and ASIC EDAC insertion, there is no "one-solution-fits-all." The user must be aware of plethora of concerns. As an example, each FPGA device-type requires a different mitigation strategy for various reasons. This presentation will focus on the susceptibilities of a variety of FPGA types and ASICs in the avionics and space environment. In addition, the user will be provided information on what are the optimal mitigation strategies per FPGA and ASIC. Internal device component mitigation versus system level mitigation will also be discussed.

Mitigation and Hardening / 20

New Paradigm of error correction used for reliable embedded memories in aerospace applications

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On-membrane PD SOI MOSFET with micro-heater for TID in-situ annealing: experiments versus Eldo and Atlas simulations.

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Abstract: Silicon On Insulator (SOI) technology has already improved immunity to Single Event Effects (SEE) thanks to the presence of the Buried Oxide (BOX). However, this technology remain very sensitive to the Total Ionizing Dose (TID) [1]. In recent works, we have integrated micro-heaters in the close vicinity of Partially-Depleted (PD) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), in order to study the possibility of in-situ thermal annealing to recover from TID-induced degradations [2]. A complete recovery by in-situ thermal annealing was demonstrated, after the exposure to high doses of gamma and proton radiations[1, 3]. The bulk etching technique used to perform the membrane, possibly alters the typical MOSEFET's behaviour. In this paper, we use 2D Atlas simulations as well as Mentor Graphics ELDO simulations of the xfab XI10 1µm technology in order to confirm the experimentally observed trends. The simulated I-V characteristics were compared to the experimental measurements of the suspended PD SOI MOSFET.

[1] Amor S, André N, Kilchytska V, Tounsi F, Mezghani B, Gérard P, et al. In-situ thermal annealing of on-membrane silicon-on-insulator semiconductor-based devices after high gamma dose irradiation. Nanotechnology. 28(18):184001; 2017.
[2] Amor S, André N, Gérard P, Ali S, Udrea F, Tounsi F, et al. Reliable characteristics and stabilization of on-membrane SOI MOSFET-based components heated up to 335 C. Semiconductor Science and Technology. 32(1):014001; 2016.
[3] Francis LA, Sedki A, André N, Kilchytska V, Gérard P, Ali Z, et al., editors. A Low-Power and In Situ Annealing Technique for the Recovery of Active Devices After Proton Irradiation. EPJ Web of Conferences; 2018: EDP Sciences; 170.

Organization / 12

Opening speeches and program overview

Authors: Raoul Velazco[1]; Gregoire Deprez[2]; Christian POIVEY[2]; Veronique Ferlet-Cavrois[2]; Agustin Fernandez-Leon[3]; Ali Zadeh[2]; Jaime Estela[4]

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Radiation Effects Hardness Assurance for space mission

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The approach used to ensure that parts will meet performance requirements for a mission operating in a radiation environment will be discussed. First part
will mostly focus on Single Event Effect Hardness Assurance. A particular mission will be used to illustrate the method. Second part will develop total ionizing dose (TID) and displacement damage (DD) hardness assurance.
Rationale for defining Radiation Design Margin (RDM) requirements will be presented. Systematic errors and uncertainties on the different inputs needed to define the TID and DD RDM will be discussed.

Tests and simulations / **23**

Radiation tests of advanced SRAM memories

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Radiation-Hardening-By-Design for the Warm Front-End Electronics of the X-IFU/ATHENA Space Observatory

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The ATHENA mission is an on-going X-Ray spacing observatory project of ESA, dedicated to the scientific theme « The Hot and Energetic Universe ». The 12-meter telescope will work in a halo orbit around the second Lagrangian point (L2 Sun-Earth) during its 5 year lifetime at the end of the next decade. The X-Ray spectral imager on board, X-IFU, based on 3840 superconducting microcalorimeters cooled to 50 mK, will provide a spectral resolution 10 times better than the best X-ray telescope nowadays.

The Warm Front-End Electronics (WFEE) subsystem is the first, non-cooled readout stage in the X-IFU detection chain. It is a mixed electronic system, including analog devices, such as the low noise amplifiers (LNA) and current sources for amplifying and biasing cryogenic stages. It also integrates digital devices: serial decoders RS485/I2C for configuring the current sources (current DAC). In the frame of the assessment phase (Phase A) of the mission, a first ASIC dedicated to the subsystem has been designed and tested. The ASIC is based on the 350 nm SiGe BiCMOS AMS technology, and integrates all the main functions needed for the WFEE.

In order to prevent the ASIC from the radiation space environment effects, RHBD (Radiation-Hardening-By-Design) techniques have been used to improve the radiation tolerance of the WFEE electronics. Their tolerances to the radiation effects TID and SEL have been tested and compared. The evolution of the main parameters of the LNA (gain and noise) and of the current source (output current and noise) with respect to different dose levels has also been measured. The measurements after irradiation show that the RHBD techniques are very effective for improving the radiation-hardened ability of the electronics circuits based on this technology. With the RHBD-enhanced design, the ASIC could fulfil the requirements of the ATHENA space mission.

Our poster will present the RHBD techniques used for the WFEE subsystem of X-IFU and the dose and latch-up tests done on the ASIC.

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Recent studies at the three irradiation facilities from the CNA and the coming upgrade.

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In this work we summarize some recent experiments carried out at the three different irradiation facilities from the Centro Nacional de Aceleradores (CNA), using either gamma radiation from a Co-60 source, or protons and neutrons from the particle accelerators. In addition, the main characteristics of a new chamber which will be available at CNA in the near future and specially designed to irradiate at elevated and cryogenic temperatures will be shown.

Radiation effects (SEE, TID, TNID) / 9

SEE effects on VLSI devices (ASIC and FPGA)

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Radiation effects on VLSI technology are provoked when radiation particles such as neutrons, protons or heavy ions hit a sensitive region of the integrated circuits. Due to the progressive technology scaling, VLSI devices are becoming, more and more vulnerable to Single Event Effects (SEEs) and are subject to cumulative ionizing damage known as Total Ionization Dose (TID). This talk will firstly describe the state-of-the-art methodologies used for analysing the impact of radiation effects on modern FPGAs and ASICs by means of Computer Aided Design (CAD) tools and secondly, it will describe the state-of-the-art CAD design techniques for their mitigation.

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SEU screening using an Am-Be neutron source

Authors: Matteo Cecchetto[1]; Ruben Garcia Alia[1]; Fabio Pozzi[1]; Slawosz Uznanski[1]; Frédéric WROBEL[2]

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I. ABSTRACT

The Single Event Upset (SEU) characterization of electronic components, requiring characteristics of radiation-hardness and employed in high-energy accelerators, relies on the knowledge of high-energy hadron cross sections typically measured with high-energy protons. Preliminary irradiation tests performed with an Americium-Beryllium (Am-Be) neutron source at CERN, demonstrated that this radiation environment can be used to induce SEUs in commercial SRAM memories. The source provides a spectrum with a peak around 3 MeV and reaches a maximum energy of about 10 MeV as shown in Fig. 1. This is a simulated spectrum thought the Monte Carlo FLUKA tool [1], [2]. The source employed for the tests presents an omnidirectional flux of 5.03×107 [s-1] and the activity of 888 GBq [3].

The ESA SEU Reference Monitor [4] (0.25 μm CMOS technology) and a Cypress 90 nm commercial SRAM were qualified with the aforementioned Am-Be source. The former is an SRAM-based detector calibrated in a broad set of facilities and used by the R2E group at CERN to cross validate the facility flux. In addition, it shows the beam homogeneity over its 20x20mm2 of active surface. The Cypress memory is the one embedded in the RadMon system [5], the radiation monitor used to measure the High Energy Hadrons (HEH) flux along the LHC accelerator.

The source and irradiation room were modelled thought FLUKA in order to estimate the flux of the source at the desired distance. Tests with the ESA Monitor were performed in different positions along the three axis with respect to the source, with the aim of evaluating in a qualitative way the flux attenuation and in comparison with the simulations [6] (see Fig. 2).

By weighting the neutron flux (derived through FLUKA simulations) impinging the active area of the device with the respective Weibull response, the agreement on the retrieved cross section with that obtained from high-energy protons (200 MeV) is within the experimental uncertainty. The same agreement applies in terms of expected upsets by convoluting the neutron flux and calibrated SEU response, both as a function of energy. Indirectly, experimental observations have shown that the cross section calculated with the specific Weibull fit is applicable to different particle energy spectra. The Am-Be source can therefore induce a statistically significant amount of SEUs in a relatively reduced timeframe (~hours). Its employment can therefore be aimed at screening the SEU sensitivity of SRAM memories in a more accessible and cost efficient way compared to high-energy cyclotron proton testing.

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Tests and simulations / 52

Simulating radiation effects of imaging detectors using Pyxel simulation framework

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Pyxel [1] is a novel, end-to-end Python framework designed to host and pipeline analytical, numerical and statistical models simulating detector effects such as cosmic rays, noise sources, Charge Transfer Inefficiency, persistence, dark current and other radiation effects on images produced by CCD or CMOS-based imaging detectors. It is currently under development at the European Space Agency with the goal of releasing it as an open-source software for the detector scientist and astronomer community.

http://sci.esa.int/pyxel

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Single Event Effect Tester for SmartFusion2 FPGAs

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Single Event Effects (SEE) are the main type of electronics failures when a device operates under extreme harsh conditions, i. e. particle accelerators or space environment. SmartFusion2 FPGA is produced as a radiation-tolerant device with some operability under such conditions. In this work, a test device for checking the reliability and aging of the FPGA is presented. The tester is based on parallel shift register structures, which are sequentially filled with the set of different test vectors in order to detect errors caused by SEE. Redundant memory circuits are dedicated to store error count, timestamps and in-chain error position securely. As the latch-up effect may appear, the additional power reset circuitry is added. Therefore the SEE tester is prepared for long-term autonomous testing in laboratory (radon decay) and even for application oriented tests (Large Hadron Collider in CERN).

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Single Event Effects (SEE): Mechanisms and Classifications

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The fundamental mechanisms responsible for non-destructive and destructive Single-Event Effects in ICs will be described in detail. This will include the interactions of ions with the constituent materials of the IC, the response of individual transistors to the disturbance, and the effect on the operation of the IC. The evolution of the threat with device scaling will be addressed.

Radiation effects (SEE, TID, TNID) / **44**

Single Event Effects Induced by Heavy Ion and Single Photon Pulsed Laser Irradiation on Atom Switch based Field Programmable Gate Array

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Single event effects (SEEs) of atom switches (ASs) embedded on 40-nm complementary metal oxide semiconductor (CMOS) were investigated with both heavy ion and pulsed laser irradiation. In the evaluation of atom switch-based field programmable Gate Array (AS-FPGA), ASs showed immunity against the irradiation and there was no change of the state of ASs both in a cross-bar switch and memory in look up tables (LUTs). It is supposed that ASs do not make any single event transients (SETs) noise when the ions hit. However, n-type metal oxide semiconductor field effect transistors (nMOSFETs) to program the ASs in the CMOS layer showed prolonged SETs against heavy ions hit. New approaches to solve the SET in CMOS are proposed in this paper, especially for AS-FPGA application.

Radiation effects (SEE, TID, TNID) / **8**

Single Event Effects Test Methods

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The lecture presents an overview of main types of single event effects (SEE), basic characteristics of sensitivity of devices and integrated circuits to SEE and existing standards and guidelines for testing with the use of heavy ion and proton accelerators. Basic requirements for both heavy ion and proton testing will be considered in detail including requirements for the energy of ions, their linear energy transfer (LET) and the range in semiconductor, recommendations for choosing the flux and fluency of ions, requirements for beam control during testing. Also, the lecture gives information about the specifics of testing for different types of SEE, such as: an impact of temperature and electrical bias conditions on the test results; recommendations for choosing test patterns during testing; advantages and disadvantages of static and dynamic testing; an impact of total ionizing dose effects on test results; specifics of testing for destructive types of SEEs and others. In addition, the lecture presents some recommendations for choosing the SEE test algorithms depending on the purpose and required result of testing.

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Solar Cells

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Space and atmospheric environments / **5**

Space Environments

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This talk presents the various radiation environments encountered by any spacecraft wandering in space, from LEO to interplanetary. For each of these environments, the potentially harmful phenomena - mainly trapped radiation, galactic cosmic rays and solar particle events - are presented as well as their degrading effects on spacecraft electronic systems.

Mitigation and Hardening / **17**

System Hardening and Real Applications

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This talk describes the suitable protections at architecture and system level against the effects of radiation on electronic components and digital systems. After the description of the general architecture of a space avionics system, the potential solutions for each type of units constituting an on-board computer are presented through the example of real space applications: avionics bus, links, memory units, and – the main part – processing units i.e. fault-tolerant architectures. The main fault-tolerant mechanisms are overviewed, as time replication either at instruction or task level, duplex, triplex (TMR), lock-step, and a trade-off between these different solutions. Then, real case studies are analyzed.

Radiation effects (SEE, TID, TNID) / **7**

TID and TNID

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Organization / **13**

Technical training

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The SpacePix radiation monitor (SXRM)

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The SXRM is a concept of a multilayer cosmic radiation detector currently being developed at the FNSPE, CTU in Prague.
Its main objective is a determination of the incoming particles species, estimation of their energy using pattern recognition techniques and trajectories reconstruction.
The geometric layout is designed to be compact with dimensions of \mbox{$5 \times 5 \times 4.2$ cm^3} and mass less than 50 g. The setup power consumption is estimated to be less than 1.2 W.

The SpacePix ASIC, a radiation tolerant monolithic pixel detector, is used as an active element. It is designed in a 180 nm SoI technology with a 60 μm pixel pitch.

The pixels contain a logarithmic amplifier, which provides a wide dynamic range of deposited charge from 2 ke$^-$ up to 10 Me$^-$.
In order to sample the energy deposition curve, several layers of the SpacePix ASIC are used in a telescope configuration, interleaved with absorber layers.

The presented work primarily concerns the simulations performed during the research and development phase. For these purposes, models of both SpacePix ASIC and SXRM were created in Geant4 and AllpixSquared packages, focusing on simulation of radiation-through-matter passage. Obtained results are being used for further development of the detection system.

The primary deployment area of the SXRM is intended to be the low Earth orbit. After successful testing and design improvements, it could be used beyond the aforementioned orbit in the Solar System.