

Tools for fast simulation of very complex System-on-Chip

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Incorporation of executable virtual prototype platforms is quickly gaining traction to aid early hardware architectural validation as well as providing software developers with an early test platform long before silicon becomes ready. One of these platforms is ESA's SoCRocket, a full-system prototype implemented in SystemC based on standardized transaction-level modelling techniques. For this work, SoCRocket's scope was extended from conventional multi-core bus-based SoC towards many-cores arranged in a tiled topology supporting the side-by-side execution of mixed-criticality applications. To deal with the simulation performance degradation caused by the increased complexity, a parallel simulation model was developed based on in-depth run-time analysis. By separating sub-systems on communication links of reduced transaction frequency into concurrent simulation processes, it achieves significant speedups while introducing only a limited timing error.