Enabling concepts: Packaging Technologies

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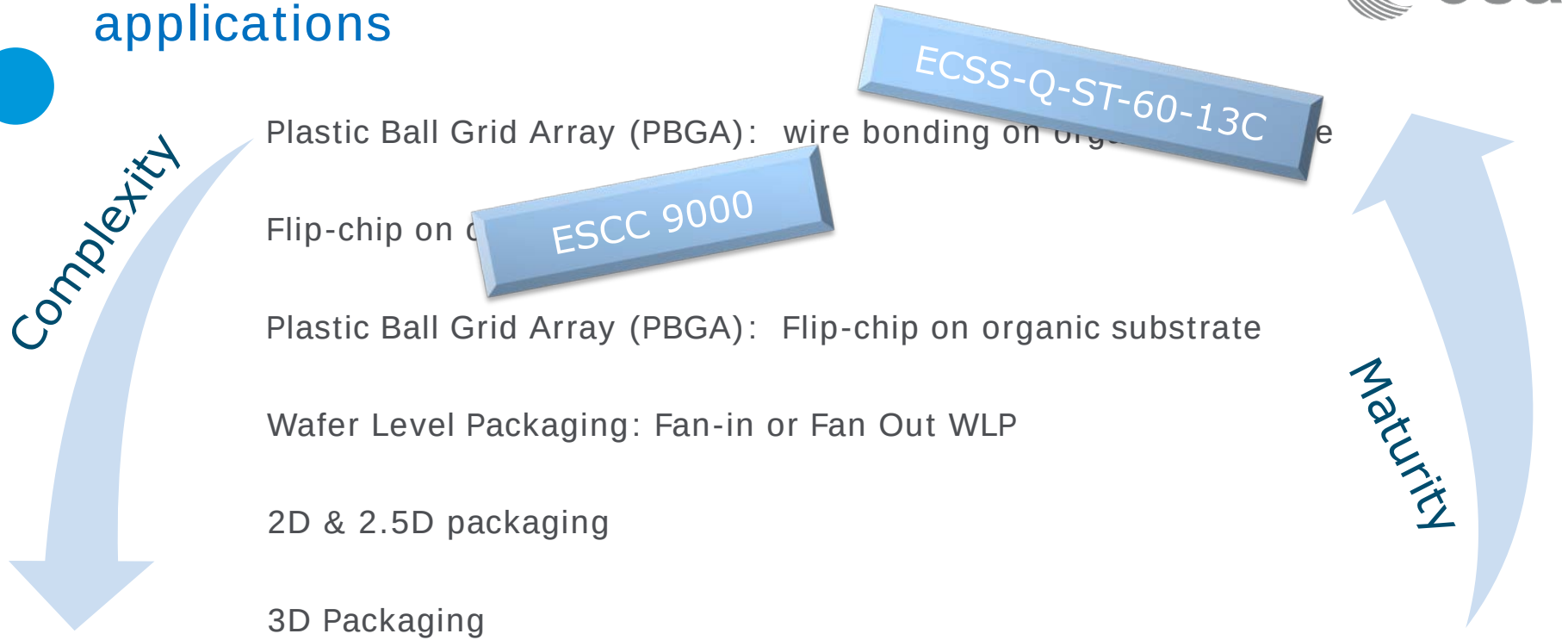
Enabling concepts: Packaging Technologies

Drivers for the future:

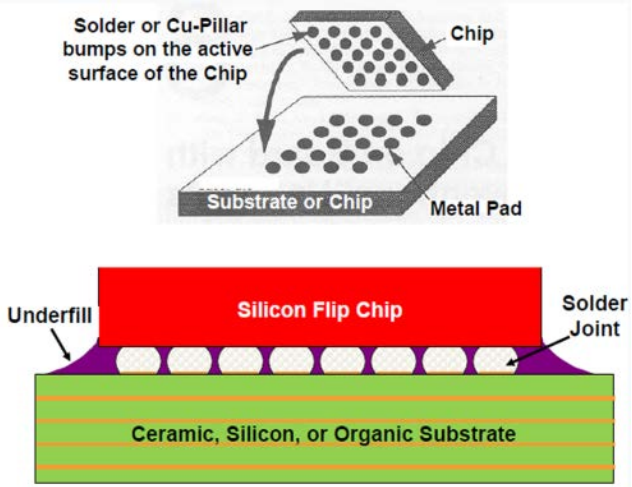
- Higher speed (>Gbps serial link)
- Higher integration between different active parts technologies
- Higher power dissipation
- Parts availability and market trends (e.g. Plastic parts, copper wire)
- Environmental regulation requirements (Lead free components)

Emerging Packaging Technologies for Space applications



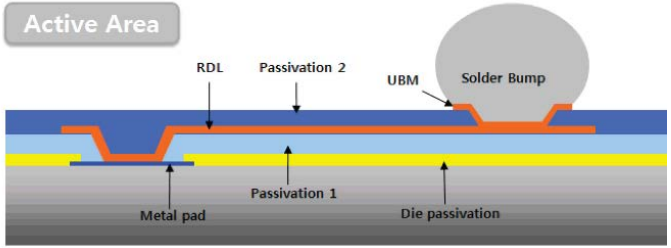
Enabling concepts: Flip chip packaging

- Concept description:
  - Could be done onto ceramic or organic substrate (e.g.PBGA)
  - Different bumping solutions (SAC alloys, Cu pillar)
- Technology Benefits:
  - Lower inductance than wire bonding
  - Better bandwidth performance
  - Lead free bumping (REACH compliant)
- Technology Drawbacks:
  - Non-hermetic packages
  - Little proven flight heritage
- Space acceptability:
  - Extensive reliability testing related to Lead Free bumping and plastic packaging
  - Establishment of procedures and requirements for manufacturing and test



Enabling concepts: Wafer Level Packaging

- Concept description:
  - FI-WLP: Fan-in redistribution
  - FO-WLP: Fan out redistribution with final molding



- Technology Benefits:
  - Suitable for new sub-micron technologies (e.g. <28nm)
  - Small Form Factor / Lower cost => High Drive from Mobile and IoT markets
- Technology Drawbacks:
  - Dielectric strength /reliability of Redistribution Layers.
  - Final encapsulation method is molded plastic (thermal management issues)
- Space acceptability:
  - Lack of definition for testing of BEOL manufacturing
  - Qualification approach similar to the silicon qualification

Enabling concepts: 2D / 2.5D Packaging

- **Concept description:**
  - 2D / 2.5D Packaging (TSV).
  - Silicon interposer, with or without TSVs. Different options/configurations possible
- **Technology Benefits:**
  - Integration of different technologies (e.g. RF/ Digital)
- **Technology Drawbacks:**
  - Use of Copper pillars with tin content > 97%
  - Micro-copper pillars technology still evolving
  - Complex testing procedures
- **Space acceptability:**
  - High diversity of technologies and unknown reliability level (for Flight applications)

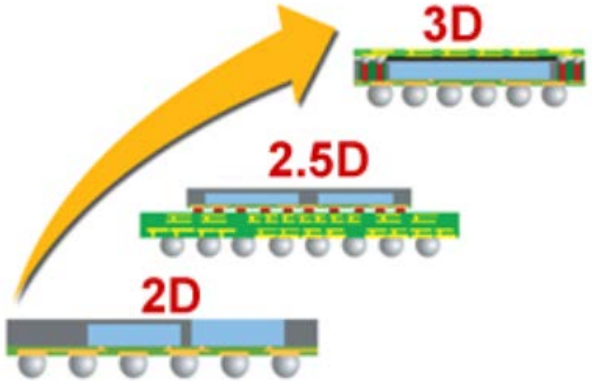
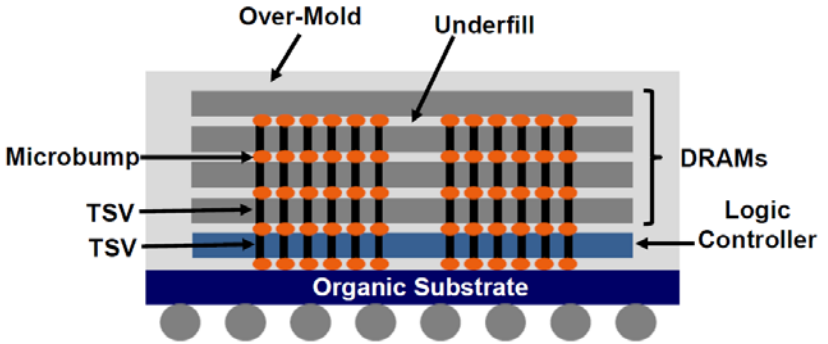


Fig. 1: Packaging solutions. Source STATS ChipPAC

Enabling concepts: 3D Packaging

- **Concept description:**
  - Proven Tech: Stacked dies and Package-on-Package (PoP)
  - Emerging Tech: 3D Wafer Stacking with TSV interconnects
- **Technology Benefits:**
  - Shorter-faster interconnections
  - Solution for Memory on Logic
- **Technology Drawbacks:**
  - Thermal management issues
  - Micro-copper pillar & TSV technologies
  - Limited shelf life (Moisture and solderability issues)
- **Space acceptability:**
  - Complex Supply Chain. Qualification of both MEOL and BEOL processes



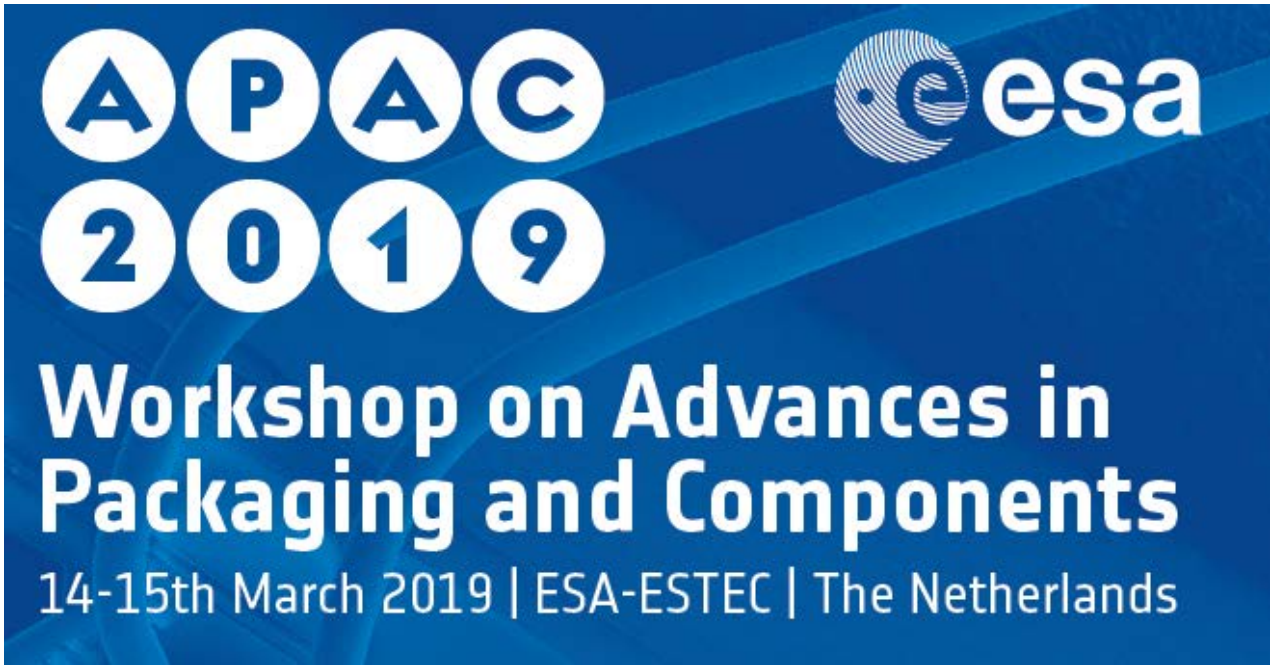
Conclusions

From the packaging perspective:

- Advanced packaging is perceived as a big variety of possible options in different maturity levels.
- Requirements flow down from components performance requirements/needs
- Reduced data available on space testing performed of Advanced Packaging
- Complex supply chain adds difficulty to the qualification of the product
- Advanced Packaging suppliers mainly in Far East
- Upcoming packaging materials restrictions (RoHs, REACH)

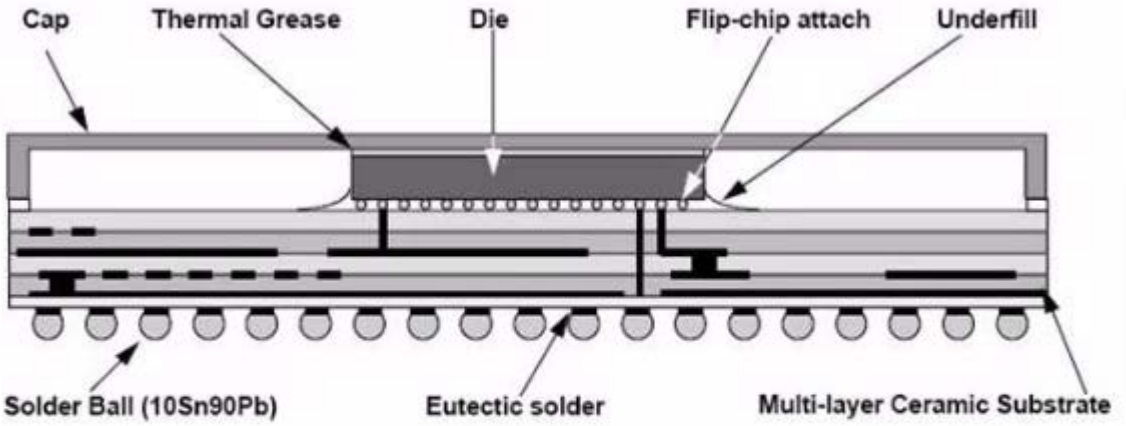
=> Could ESA use/qualify any of these technologies in the future?

Advanced Packaging Conference



Back–up slides

CBGA:



CBGA (Ceramic Ball Grid Array)

Image Cited from Test and Measurement World

Back–up slides

Organic BGA:

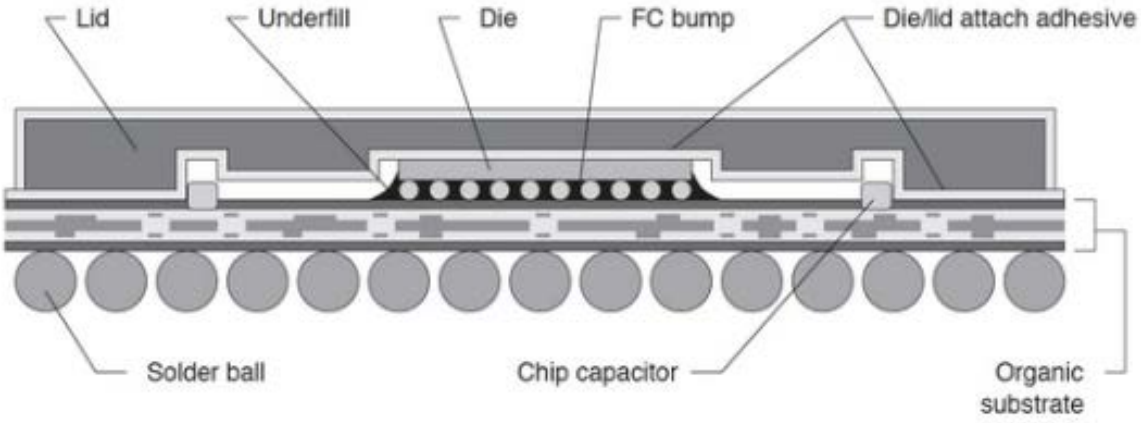


Image Cited from Shipco Circuits

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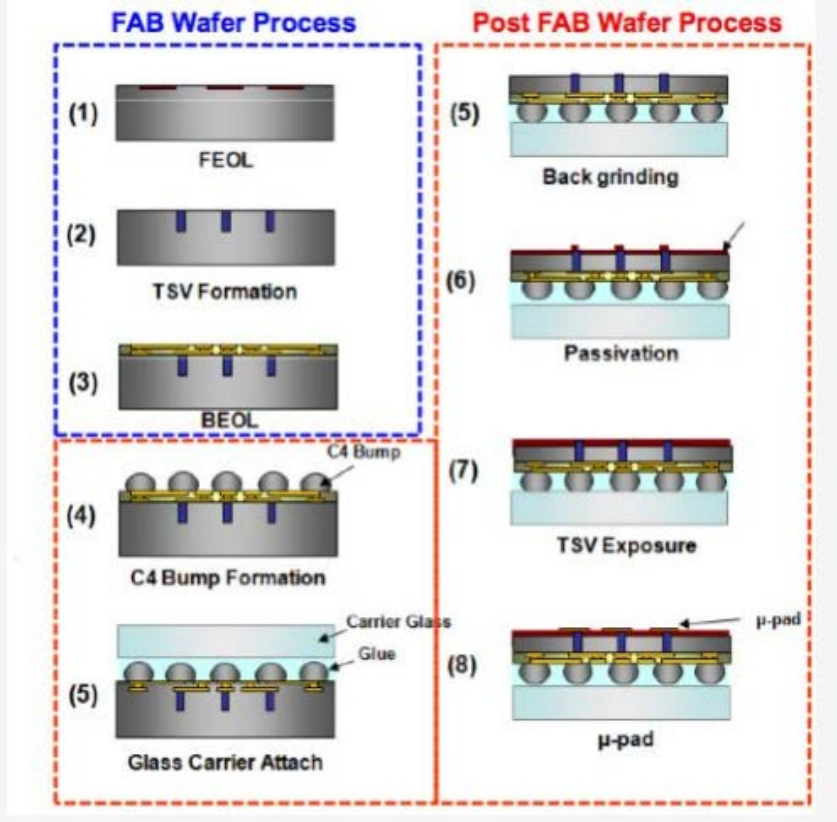
TSV Formation:



Back–up slides

Xilinx Virtex-7 2000T