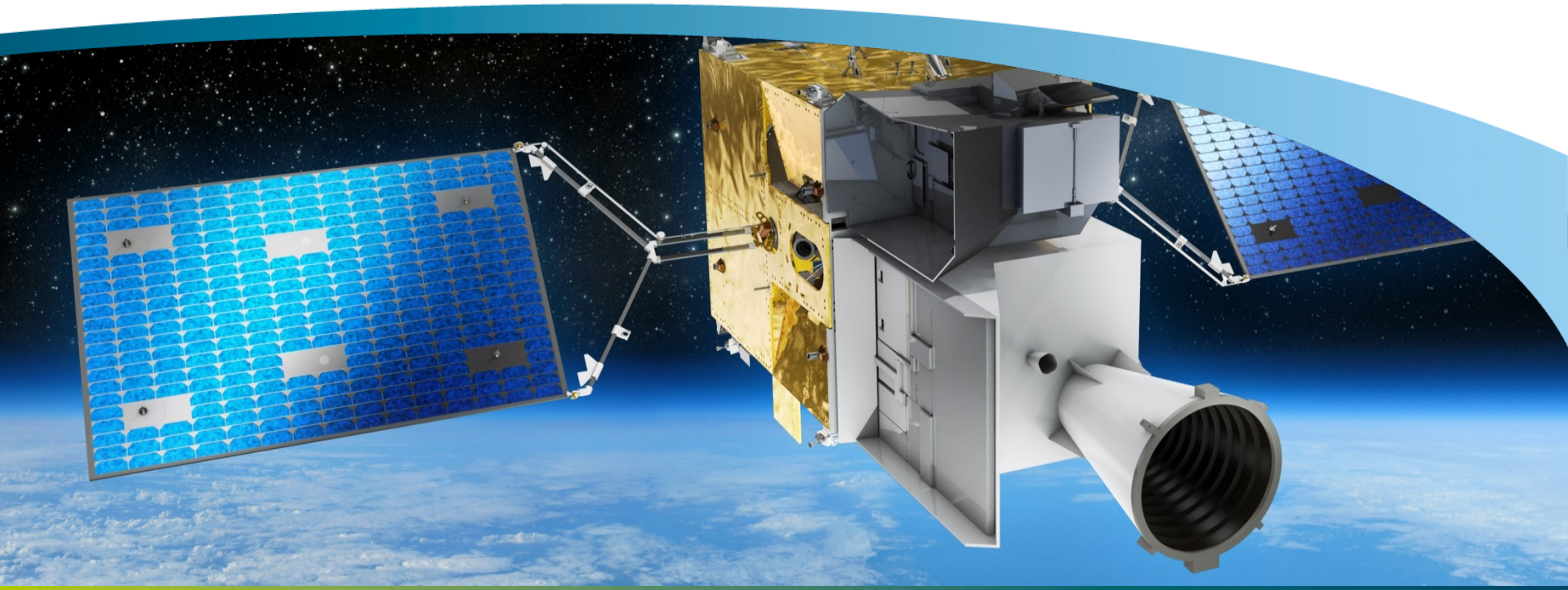
OHB System AG



SPACE SYSTEMS

ESA High End Digital Processing Technologies and EEE componets for Space WS

P.Pierrot 2018/10/01

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Radar Systems

- Trend of radar payloads goes towards multi-channel radars and “digital radar”,
  i.e. early digitisation and subsequent digital on-board processing,
  e.g. for digital beamforming (high resolution wide swath) & on-board data reduction

- Examples of future Earth observation missions with need for FPGA based on-board processing
  - Copernicus Space Segment Expansion / L-Band SAR Mission (LSAR)
  - Tandem-L
  - EE9 SKIM

- Typical Requirements
  - LEO orbit (500 km to 900 km)
  - Full in-flight FPGA-based re-programmability
  - instantaneous input data rates in the order of 50 to 200 Gbit/s split over multiple channels
  - instantaneous output data rates in the order of 1 Gbit/s to 10 Gbit/s

  → the processing power of available space-qualified FPGA is not sufficient to cope with the needed processing power in terms of number of I/O, RAM and DSP cores

  → use of high-performance mil-grade FPGA could be a solution

HyperSpectral Systems

- The **trend** for hyperspectral payloads goes towards higher and higher data throughputs, resulting from a need for increased ground resolution and reduced revisit times. The limited downlink rate - bottleneck - imposes more complex **on-flight data processing** in order to reduce the data volume to be transmitted without loss of information
- Consequently, there is a need for more efficient data compression algorithms and for faster hardware (FPGA, memories, interfaces)
- The **algorithm research trends** are:
  - Predictive, instead of transform (wavelet) compression
  - Near-lossless instead of lossy or lossless compression
  - Data reduction by means of cloud screening and removal
  - SW defined processing for complex algorithms
- The **Hardware trends** in parts selection are:
  - High capacity and fast FPGAs to sustain fast and complex algorithms
  - High capacity and fast memories to store numerous frames
  - Fast interfaces as Wizard-link, Space-Fibre and CML and VML for optical and electrical physical layers respectively

Opportunities

- Examples of future Earth Observation missions with hyperspectral and similar payloads are the Copernicus Sentinels and in particular the Copernicus expansions of:
  - Copernicus CHIME hyperspectral instrument
  - Copernicus CO2M: CO2, NO2, Cloud Imager and MAP Instruments

High Level Requirements

For example the following data processing requirements apply for the the CHIME instruments:

- Capability to manage high data rates (**up to 3Gbps**).
- Capability to correct pixel data (individual **pixel gain and offset**) in real time to enhance the compression ratio.
- Capability to apply, in-orbit, real-time data reduction in order to avoid useless areas (cloud removal); the data reduction process implies the use of **wide memory buffers** capable of storing many frames, these are then processed in order to take the decision to discard or not the data.
- Capability to compress data according to **CCSDS 123.0-P-1.1 standard** (**predictive compression**) in different ways (**2D, 3D**) and by using different methods (neighbour or column oriented); capability to sustain an input data throughput of at least **150Mpix/s**.

Low level Requirements

- The previous high level requirements can be translated to lower level hardware requirements, as follows:
  - Use of adequate electrical and optical interfaces able to sustain the above data rates (SpaceFibre for optical and Wizard-link for both).
  - Multiple Input data streams for SWIR, VNIR and VIS channels.
  - Use of FPGAs (e.g. Xilinx Virtex 5 and Microsemi RGT-4) able to implement 150 Mpix/s compression algorithms
  - Use of large /fast memory devices (SDRAMs and DDRs) able to store the necessary number of frames requested by the compression algorithm and to provide the necessary access times in order to guarantee real-time execution.
  - On-flight re-programmability for data reduction algorithms that require tuning (e.g. cloud screening and removal)

Communication Payloads

- Trend for GEO/MEO communication payloads;
  - (V)HTS GEO/MEO satellite payloads require powerful digital transparent processors (DTP)
  - The shift to 28 nm (e.g. FDSOI) or lower ASIC technology allows the implementation of DTP capable of several hundreds of Gbps throughput with a SWAP compatible with the current large satellite platforms
  - These DTP offer a high level of mission versatility and re-configurability now required by satellite system operators
  - The DTP available on the market are modular and can fit on medium and small platforms as well
  - The availability of high digital processing power in a relatively small SWAP factor allows the on-board implementation of new functionalities, e.g. on-board interference detection, mitigation and - possibly - localisation
  - There is a definite interest for multi-mission payloads and a regain of interest for fully processed payloads for some specific future missions

Communication Payloads

- Technologies for high performance DTP (Digital and Mixed-Signal)
  - Despite the recent progresses in FPGA capability, ASIC technology constitutes the only viable solution to the required processing power and still offers higher tolerance to radiation than the latest high performance FPGA
  - As the availability of 14 or 12 nm IC technology is announced for the near future ASIC will keep this advantage in future implementations
  - Depending on the type of mission direct digital sampling up to Ka-band uplink frequencies is achievable with custom designed front-end ADC, though with limited dynamic range and to the detriment of higher power consumption compared to front-end implementing sampling at an IF stage, e.g. L to C-band
  - This current limitation might not be an issue for commercial payloads but military communication payloads require a higher dynamic range

Communication Payloads

- OHB experience
  - Use of re-programmable FPGA for active equipment, generic design (cost optimization) with firmware customization during the manufacturing phase depending on mission specific requirements (e.g. flexible MPM with E2PROM and SRAM-based FPGA)
  - Implementation of a fully regenerative ASIC-based digital processor on-board the Hispasat AG1 mission
  - 2 different digital on-board processors are currently being implemented on the H2SAT mission and will allow to carry out different signal processing and COTS SRAM-based FPGA radiation tolerance experimentations in GEO orbit
  - Thanks to the in-orbit re-configurability of these OBP additional experiments might be carried out, e.g. validation of the performance of a specific air-interface, validation of interference processing algorithms, precoding…
  - Concepts developed and validated thanks to OTS SDR equipment, e.g. interworking, might be of interest for non GEO satellite missions

Overall considerations

- Multiplicity of ASIC digital, analog, mixed-signal processes and technologies, one has to identify the right technology for the right application at the right time
- DSP clusters a potentially interesting solution for some future applications
  - Use of high level programming language
  - Fast track from algorithm definition to algorithm validation
  - Require adequate training for highly specialised engineers
  - Supplier development support may exist but some application require an adequate level of confidentiality
- “Standard” high performance ASICs a very promising solution for implementing high performance OBP if their performance could match the performance of custom ASICs
- Interestingly - but not surprisingly - one could see a convergence between FPGA, DSP based SoC ands “standard” ASIC
- Dissemination of knowledge and skills within company departments or company subsidiaries requires adequate organisation to foster synergies