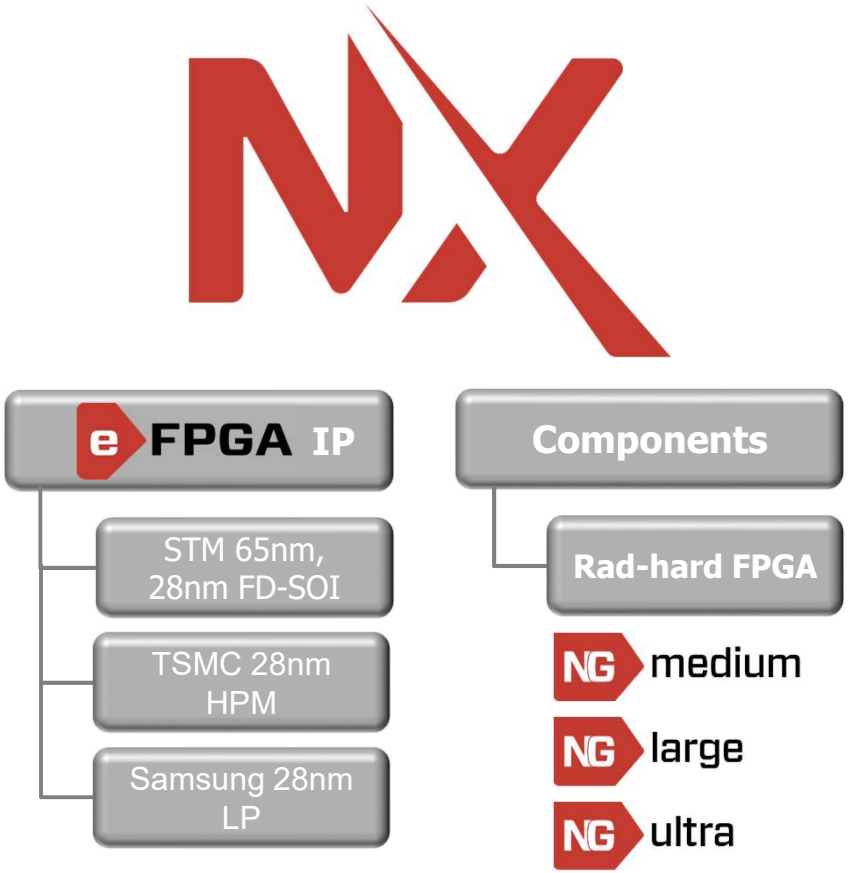
ESTEC Noordwijk, NL, 1st Oct 2018

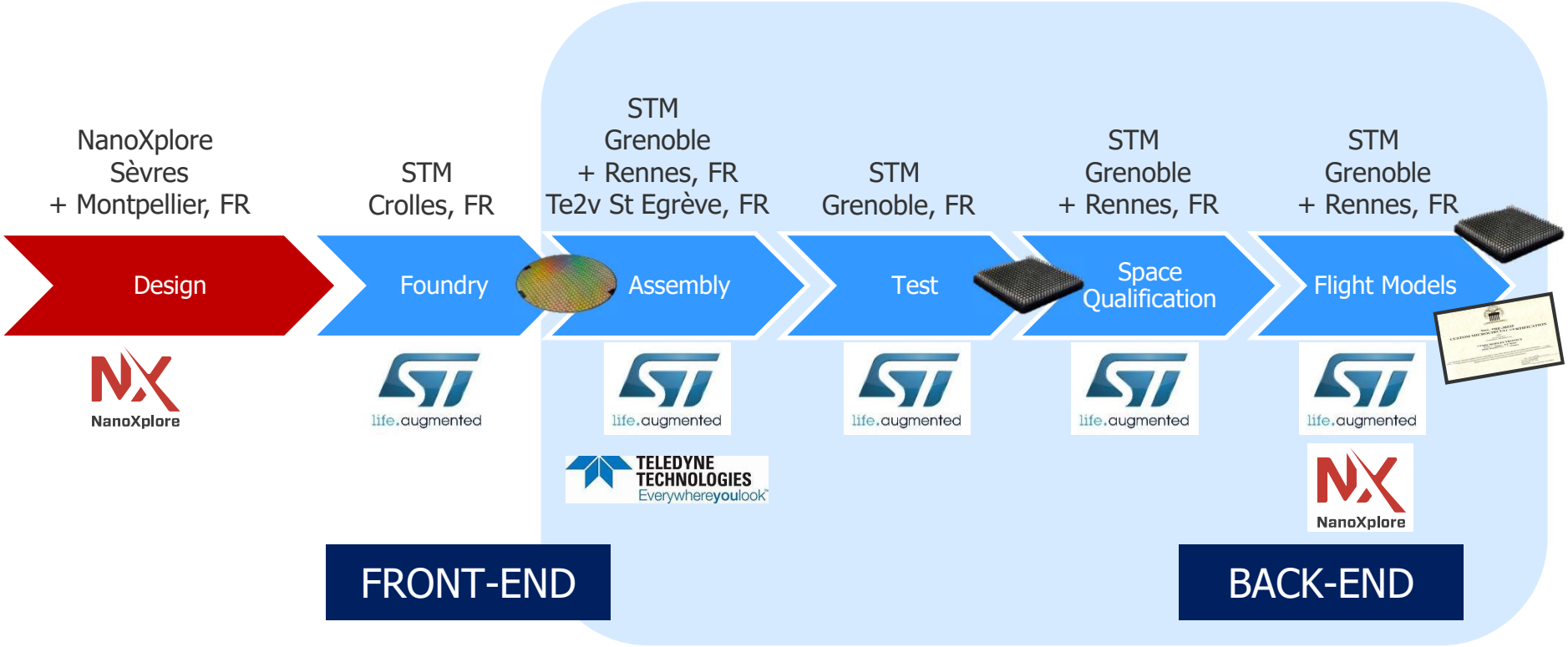
NanoXplore Overview



- **Created in 2010** by three veterans of semiconductor industry with long experience in the design, test and debugging of FPGA cores.
- **Fabless** semiconductor company headquarter in France
- R&D engineers in two offices in France:
  - Sèvres: Hardware developments
  - Montpellier: Software developments
- **NanoXplore is a leader in the design of large scale programmable logic arrays for state of the art FPGA cores**
- The company is focusing on 2 main activities:
  - Offer hard block embedded FPGA core IP (NX-eFPGA)
  - Developing rad-hard FPGA qualified for space applications (from BRAVE contract)

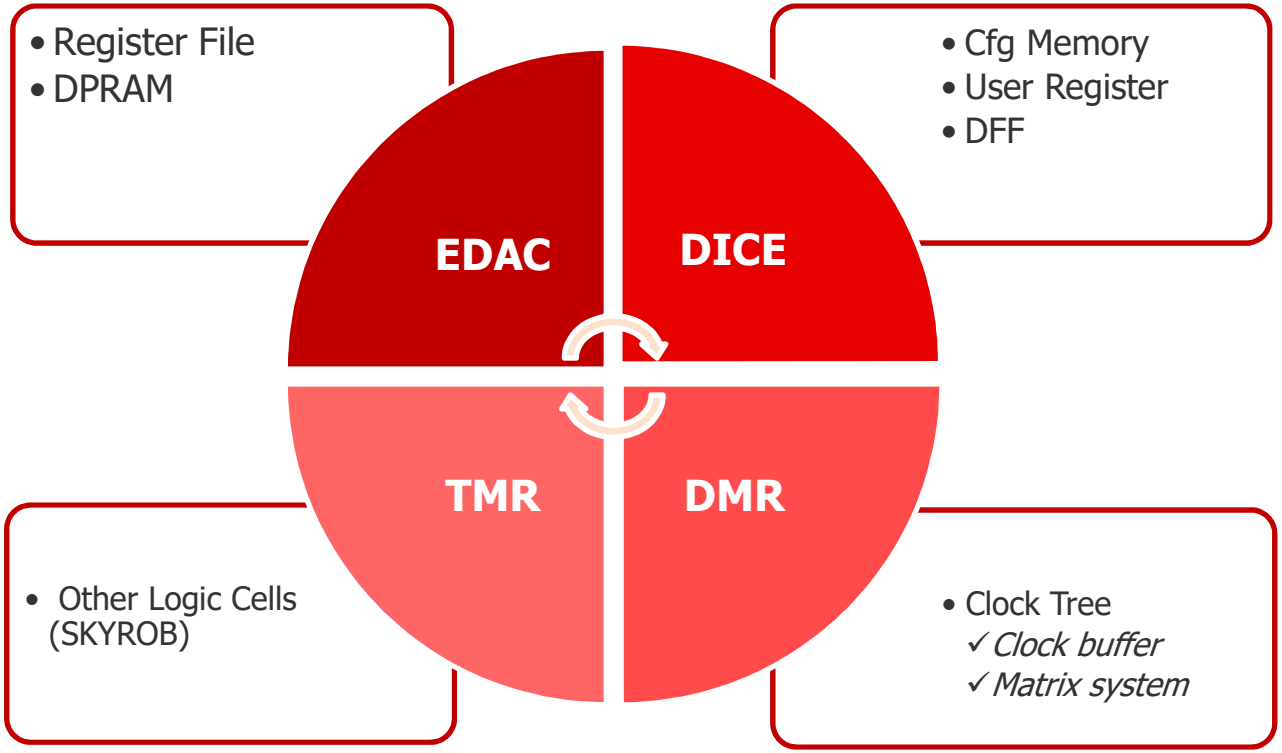
NanoXplore – Space Supply-Chain

- **From Space FPGA Design to Flight Models deliveries**



NX FPGAs are Rad Hardened

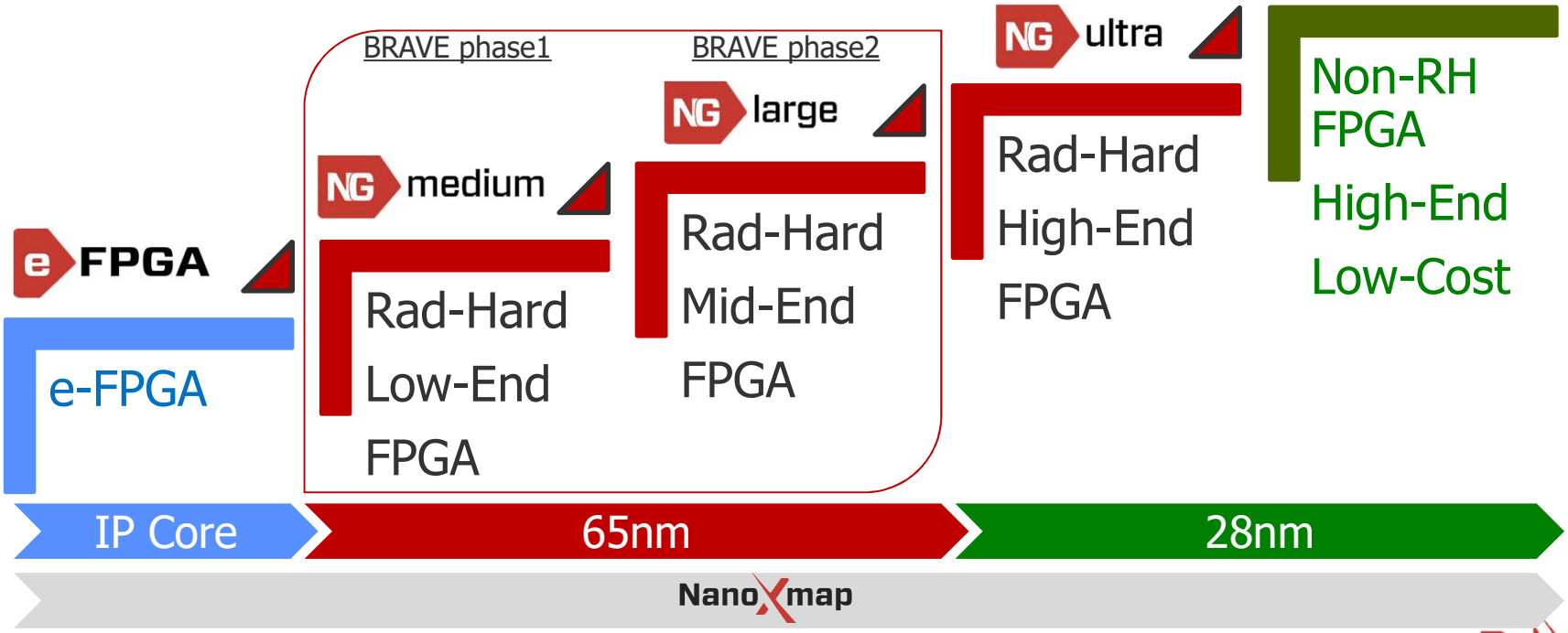
All logic of NX FPGAs is hardened by design (RHBD)
and simulated with TFIT software



On top of it,
Embedded Configuration Memory Integrity Check ("CMIC")

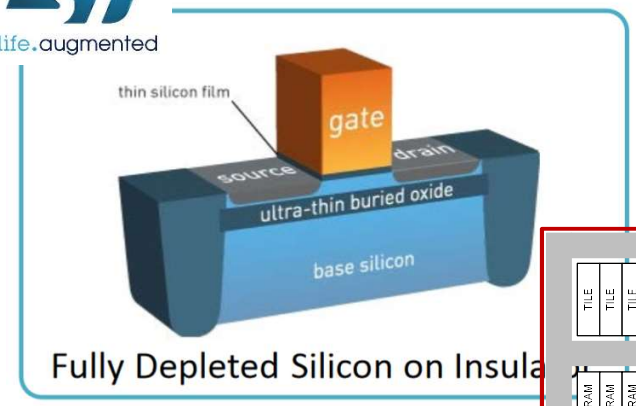
NX - From eFPGA to BRAVE & beyond

- NX has a strong experience in developing eFPGA cores on the most advanced technology nodes.
- **Hi-rel** markets (like space) require specific features: Radiation hardening, High-Reliability, Security etc.
- European funding to support that initiative: CNES, ESA, EC, DGA, DGE, BPI, EDA …
- Space market has many synergies with **additional market such as Avionic, Military, Railway and Medical, even Automotive**
  - Limited competition and clear technology advantages.



NG ultra 1st RHBD High-End SoC FPGA

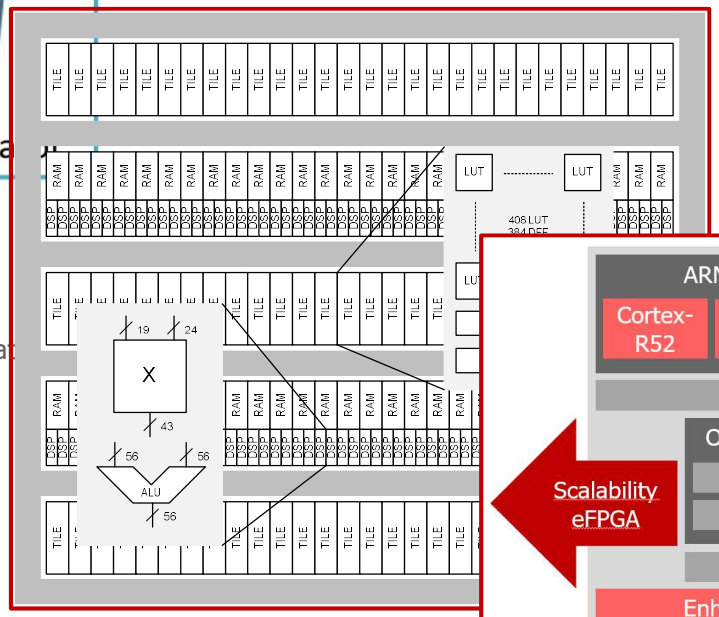
28nm



- Low Power
- High Performance:
  - Logic: **500MHz** (Toggle ra
  - DSP: 800MHz
  - Diff I/O: 1Gbps
- High Reliability
- Hardening performance
  - Fully hardened by design
  - TID > 50 Krads TID
  - No Single Event Latch up (LET>60 MeV-cm2/mg)
  - Fully SEU immune up to 60 MeV-cm2/mg

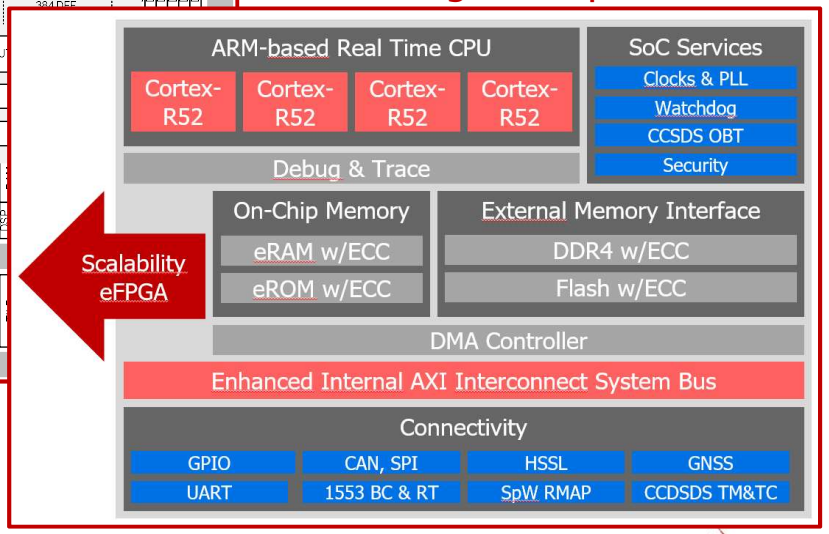
+ Large FPGA Fabric

- 540KLUT4 + 500K HDFFs + 45Mb RAM
- 1760 DSP blocks
- 32x HSSL 12,5Gbps
- Flip-Chip assembly

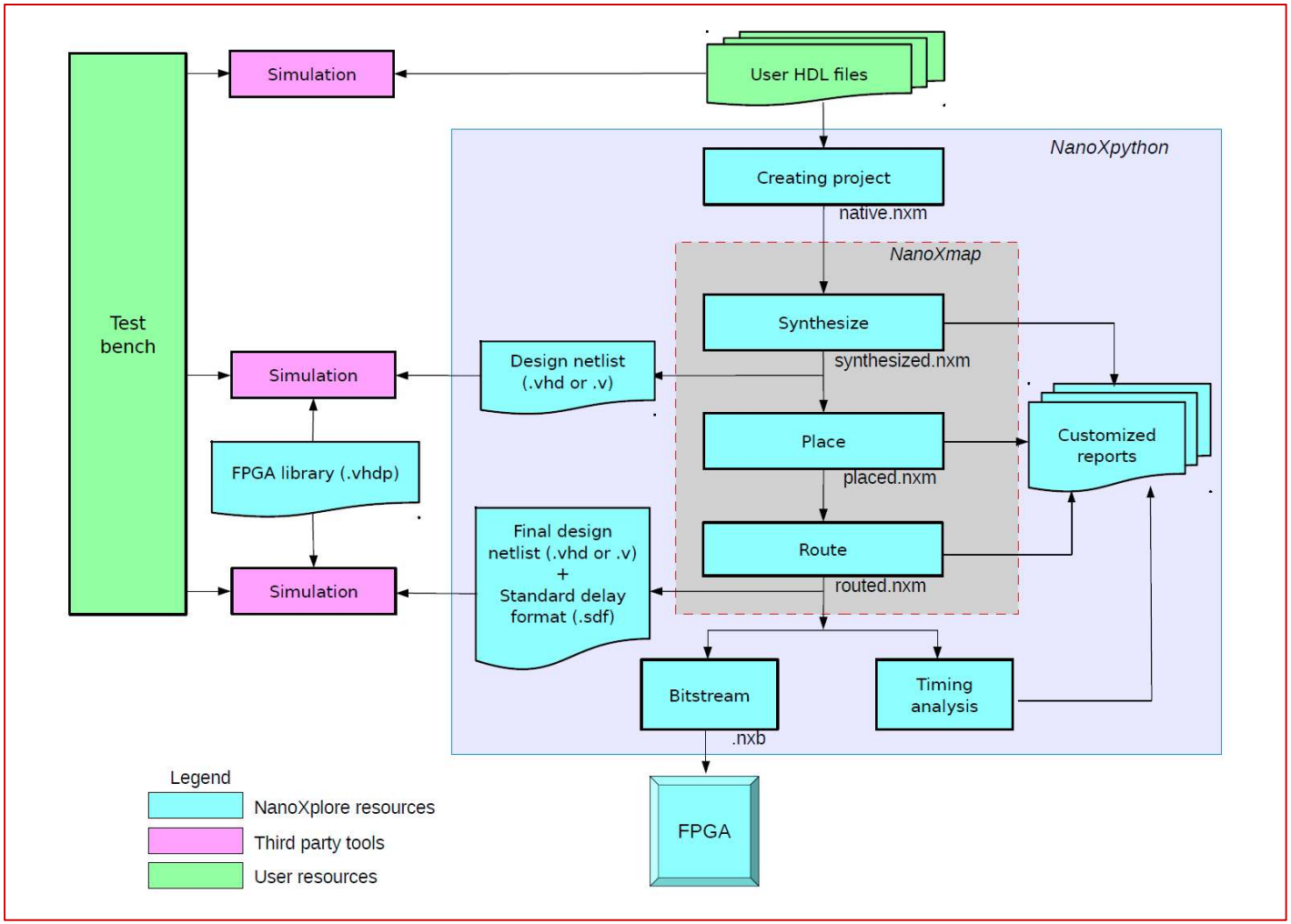


+ High-Performance SoC

- Quad-Cores ARM Cortex R52 (Advanced Processor for Safety)
- 4000 DMIPS performance
- Designed to face New Challenges of Space

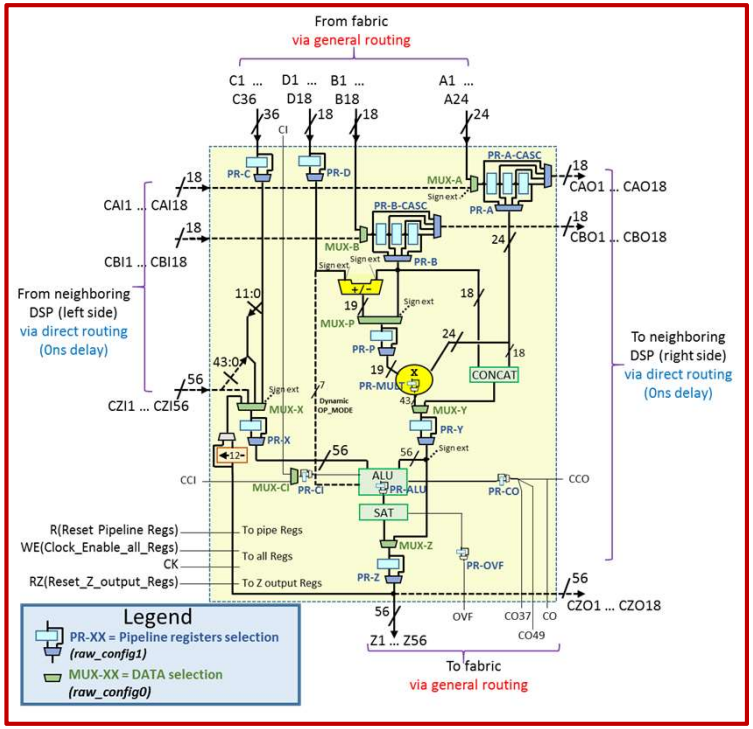


Programming Software: NanoXmap Overview

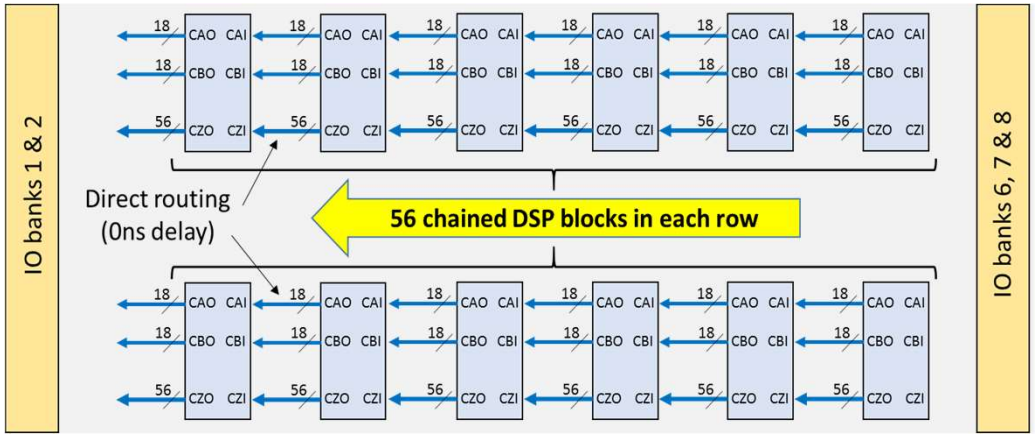


High-Perf. DSP applications with NG medium

- Each DSP block includes :
  - Signed/unsigned 24 x 19-bit multiplier
  - 56-bit post-adder/accumulator
  - 18 + 18-bit, 19-bit result pre-adder
  - User selectable pipeline registers for maximum performance
  - Direct routing (0ns delay) with neigboring DSP blocks



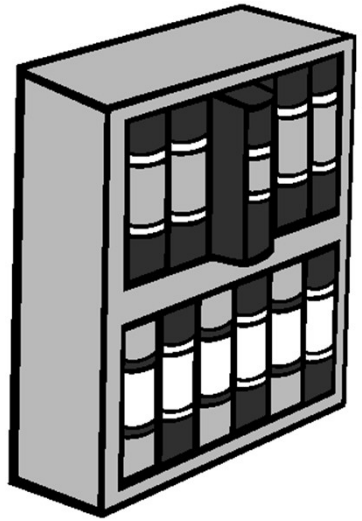
- NG-Medium has 2 rows of 56 cascadable DSP blocks



- DSP blocks can be infered in VHDL source code. NanoXplore provides templates and examples

NX Cores

Nxcores is NanoXplore IP core generation tool



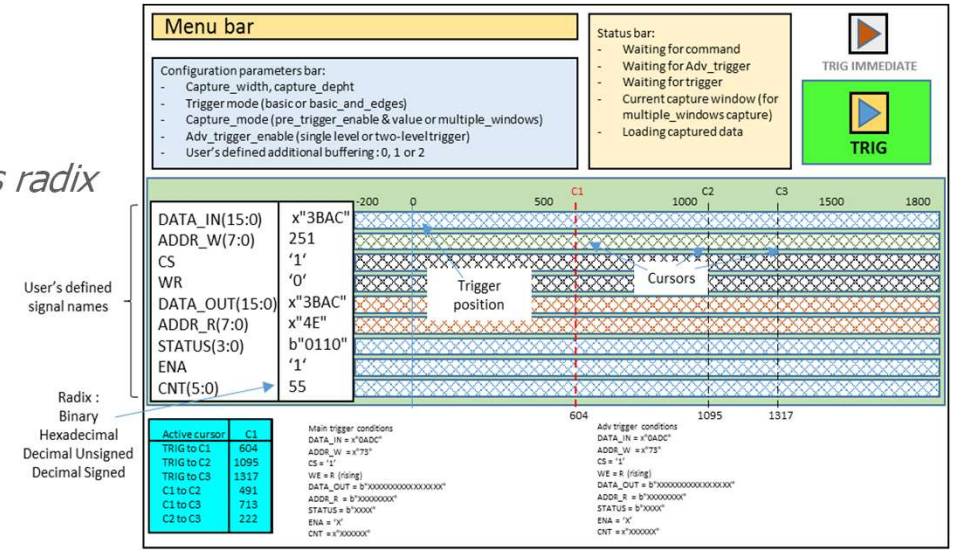
- SpW IP core inside v2.9.0 (tested by ESA + GMV)
- **Planned within next NanoXmap versions**
  - *DDR Interface (DFI2.1)*
  - *Parallel FIR filters generator (sample frequency > 200MHz),*
  - *Multi Multiplier-Accumulator (MAC sequencial filters*
- **Planned H1CY19**
  - *Sinus/Cosinus tables,*
  - *Numerically Controlled Oscillator (NCO), Direct Digital Synthetizer (DDS)*
  - *Extended Precision Multipliers,*
  - *Complex Multipliers, …*
- **From NX Eco-system**
  - Adentis/Maya Technology*: Mil-Std-1553B BC/RT,*
  - Cobham Gaisler*: Leon2/3, GRLIB …*
  - Skylabks*: PicoSkyFT-L, and PicoLIB (UART, Timer, I2C, GPIO, …)*
  - STAR Dundee*: SpaceWire, SpW CODEC, RMAP, Routing Switch, even High Perf. FFTs, Image Processing, Camera Interface, CAN…*

NX

NXscope

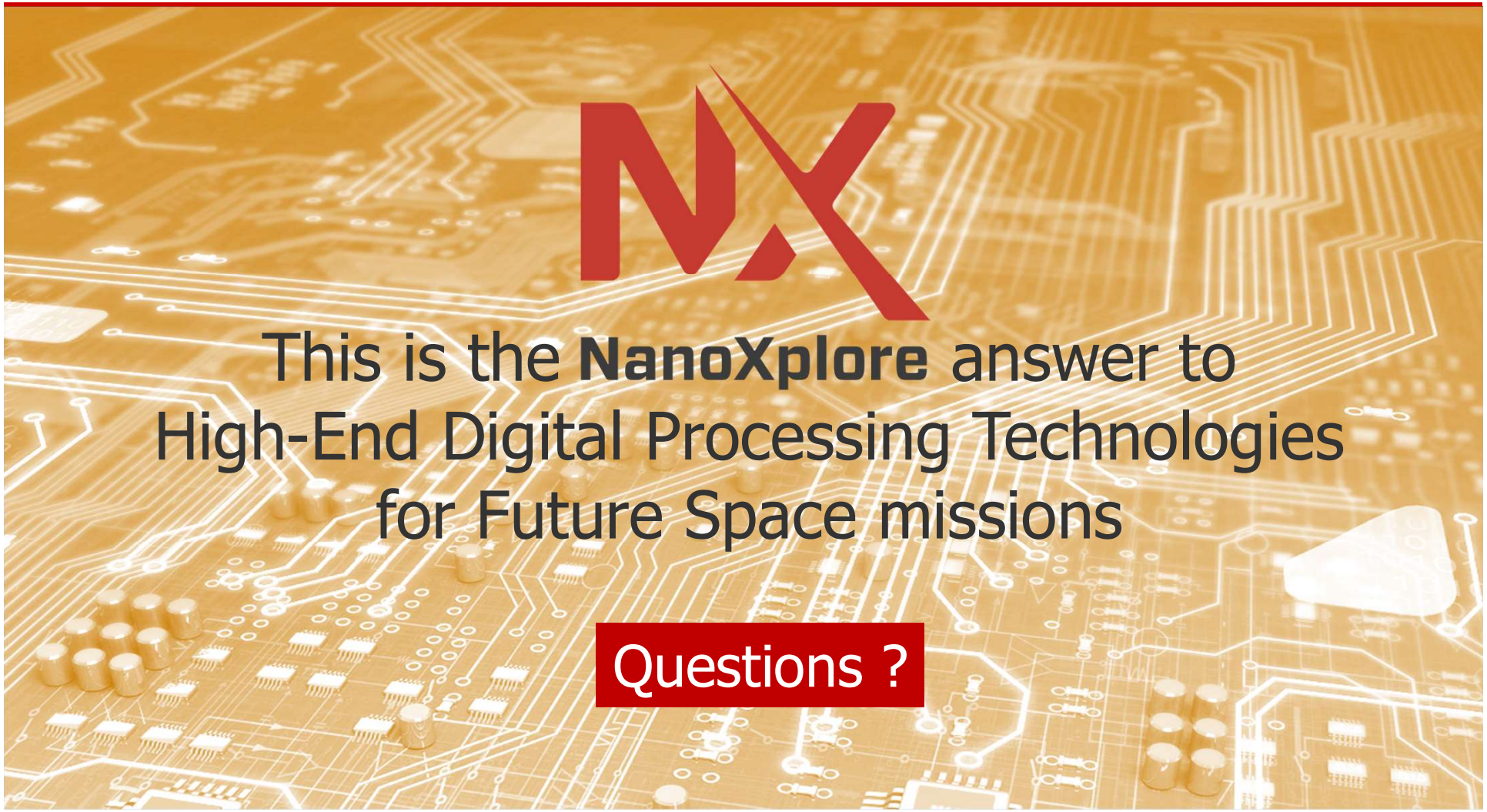
NXscope is NanoXplore Embedded Logic Analyser IP core

- Process
  - Nxscope is driven via ANGIE JTAG adapter and NXbase2 (delivered with EK),
  - Create your own ZLA IP core with NanoXplore tools
  - Instantiate the IP Core in the source code of your design
  - Implement the design and check the results
  - Generate the bitstream
  - Launch the Logic Analyzer GUI
    - *Configure the FPGA with the bitstream*
    - *Configure the graphic waveform and signals radix*
    - *Save the graphic setup*
    - *Launch the trigger*
    - *Analyze the results*

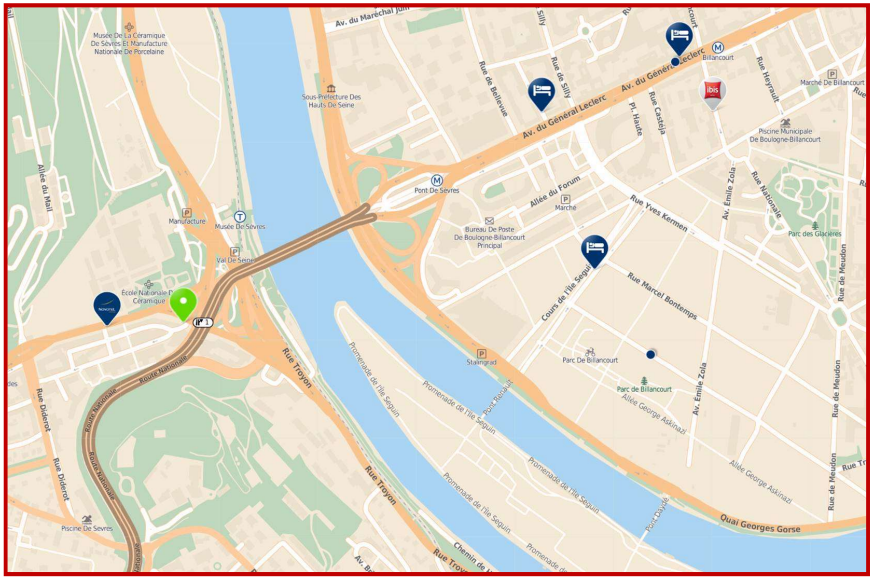


- Features
  - Up to 64 sampled lines,
  - Up to 32 trigger lines,
  - Flexible trigger conditions
    - Detection of values and/or edges on trigger lines
    - Programmable pre-trigger samples
    - Multi conditions trigger

Q&A



Thank you



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