Workshop on High End Digital Processing Technologies and EEE Components for Future Space Missions

CNES View

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Outline

- **CNES orientations**
- **CNES Experience on High End Digital components**
- **Main Challenges**

CNES Orientations

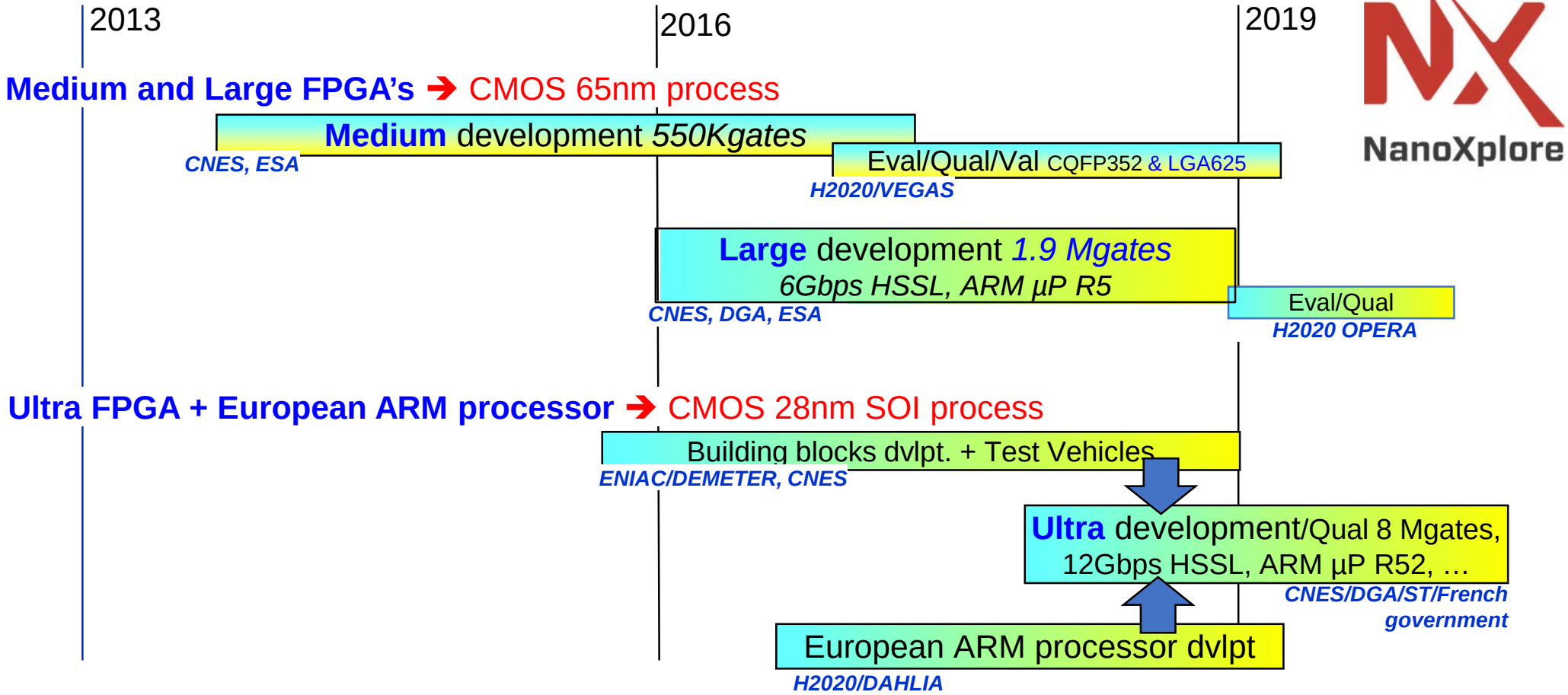
Strong involvement on :

- “Strategic” High End Space Components
  - Developments, Evaluations, Qualification, Radiation Hardness Assurance, …
  - Main “strategic” families : FPGA’s, ASIC’s, Advanced Converters, … (See examples next slides)
- High End Commercial components
  - Evaluations of State of the Art FPGA’s, Memories, …
  - Complementary approach with appropriate standardization (ECSS Q60-13)

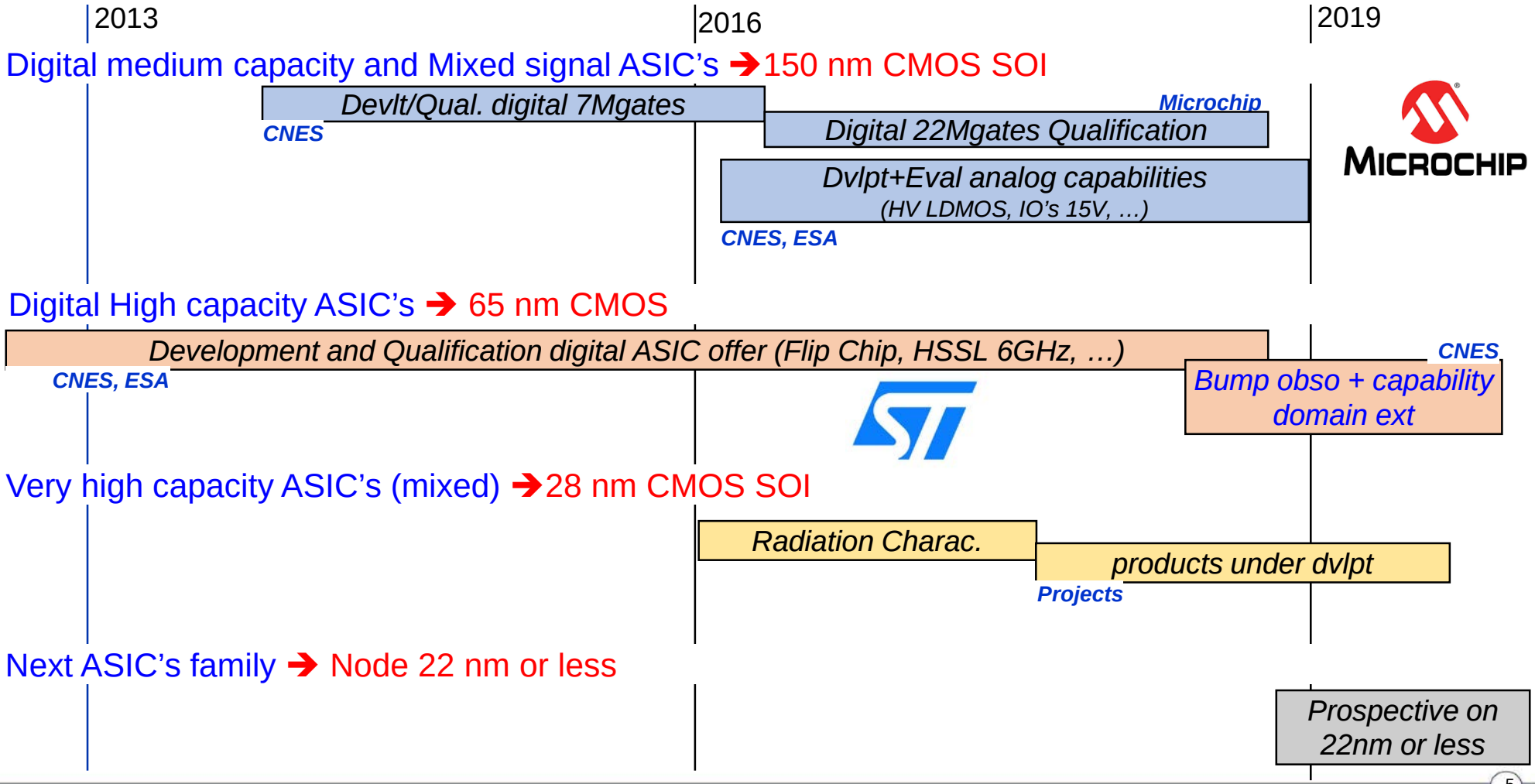
Harmonize/Coordinate activities via Working Groups/Cooperation with:

- European Agencies, Primes, manufacturers via the **European Space Component Coordination (CTB)**
- **French DoD** (Converters, ASIC’s, FPGA’s, RF, …) and **SGDSN** (COSPACE)
- French primes and equipment makers via the **French Components Multi-partnership** (in particular for commercial components use)
- JAXA …

Example of CNES FPGA's « Space » Components Roadmap



Example of CNES « Space » ASIC's Roadmap



CNES Experience on High End Digital components

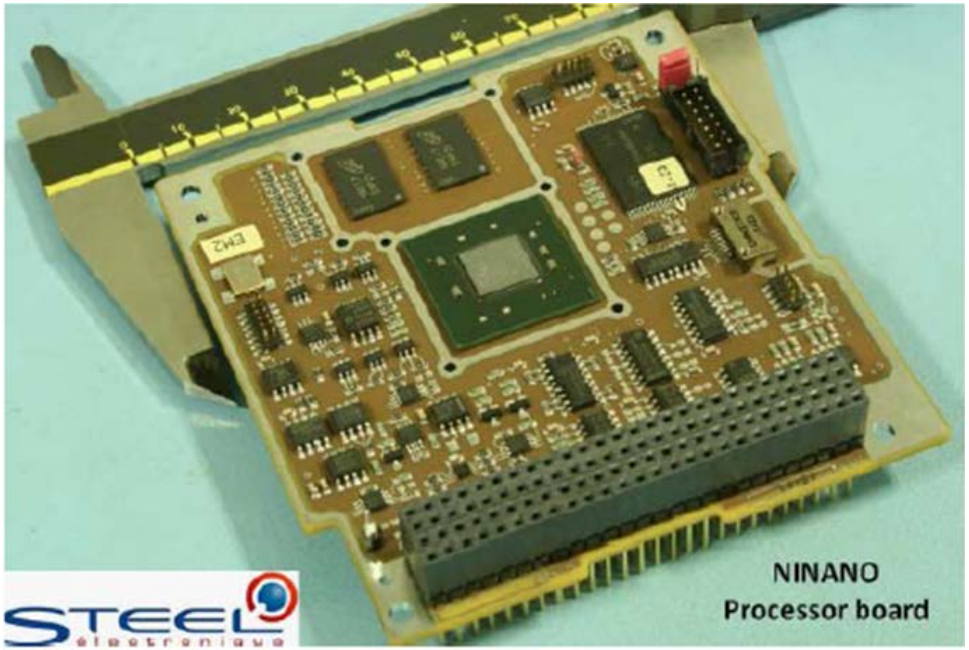
High end commercial components massively used @ CNES since 1988

- State of the art Components (memories, DSP, µP, µC, FPGA, RF, …) See example next slides
  ➔ mandatory for high performances and not available in “Space level”
- Continuous evaluation programs of SOA components *(Yearly CNES R&T and “Projects” funds)*
- Very good results in orbit ➔ No in flight failure on FPGA, µP, High-speed Tx/Rx, EEPROM, …

Creation of the “French Multi-partnership” in 1998 to :

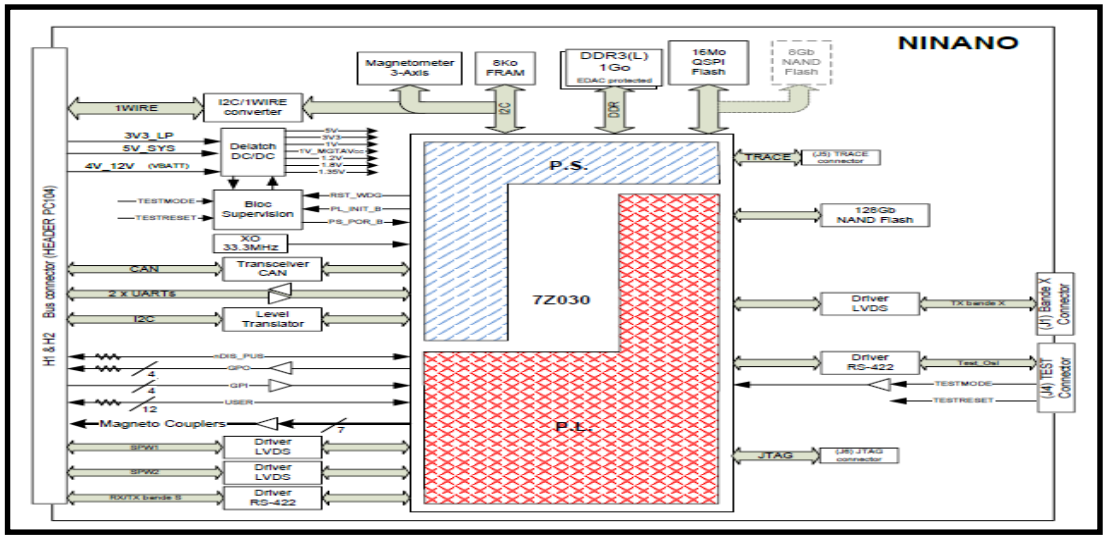
- Anticipate needs and Select right candidates ➔ Common needs/work list yearly updated
- Share efforts and budgets (mainly for evaluation tests) and avoid duplications
  ➔ Obtain reliable evaluation results as quick as we can
- Share results in real time through a database (740 reports exchanged since 1998, around 40 identified actions each year)

Example of CNES Embedded computer board, ZYNQ based



Features :

- Zynq 7030 (28nm)
- RS485/RS422 transceivers
- FRAM 8kbytes
- NAND Flash 128Gbytes
- 1Go DDR3
- 16Mbytes Quad SPI Flash for Bootloader
- …



Lots of commercial components used on this board

Example of CNES Embedded computer board, ZYNQ based

Destructive SEE realised at component level through several campaigns

Non-destructive SEE realised at CERN facility to characterise mitigations at board level

Example of CNES Embedded computer board, ZYNQ based

First Flights planned in 2018 and 2019

Main Challenges for High End Components

“Strategic” Space Components

- Devt/ Hardening + Eval + Qual Costs of NG components (ASIC’s, FPGA’s, …)
- Time to market for 1st FM’s
- Work/cost for qualification maintenance
- Manufacturer viability
- Lead free (Assembly and Packaging)
- Organic substrates for Flip Chip
- Plastic Packages

Commercial Components

- Selection of the good candidate
- Avoid duplications
- Reliable Radiation tests
- Accurate SEE risk prediction *(Simulation tools to quantify the number of SEE’s)*
- Lead free use *(assembly and packaging)*
- “Strategic” lots *(in case of good rad results)*
- Certified Rad Tolerant products *(by the manufacturer itself)*

Two complementary approaches for high-end components

Thank you for your attention