Workshop on High End Digital Processing Technologies and EEE Components for Future Space Missions

Mass Memory Storage and the use of Commercial Off the Shelf (COTS) EEE Components.

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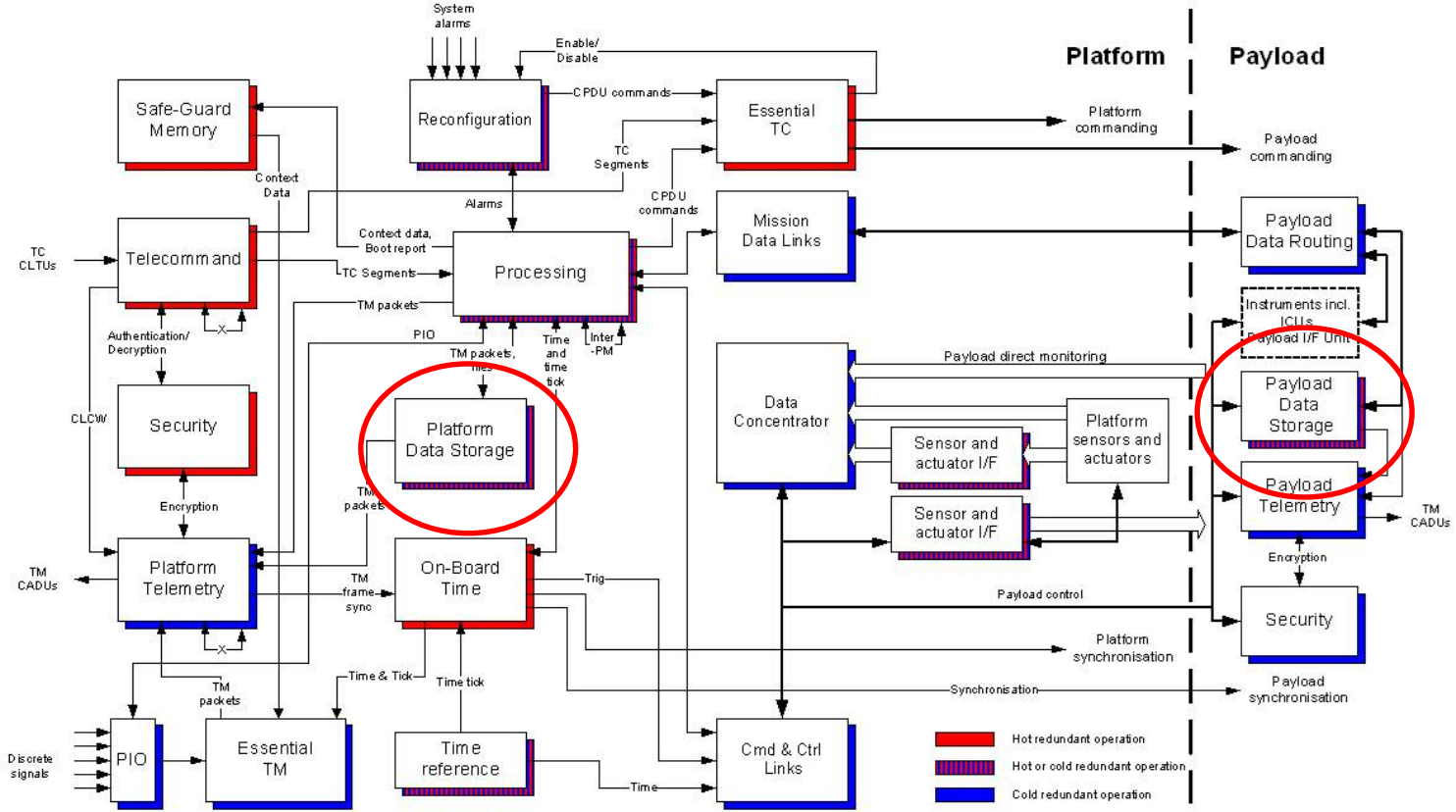
Introduction

- The increased data volumes produced by spacecraft payload instruments coupled with increased data downlink rates are key technology drivers for on-board Solid State Mass Memory (SSMM) storage units.
- In traditional avionics architecture, SSMMs are utilised as separate units to serve platform and payload level needs.
- In some cases (e.g. JUICE), to save precious on-board resources single unit SSMMs are utilised to cater for both payload and platform applications.
- SSMMs consist of a variety of technologies to achieve stringent requirements.
- Due to the often high capacity storage required, COTS memory devices are employed together with space qualified EEE Components.
- Careful consideration has to be made when selecting and designing based on COTS devices.

JUICE SSMM

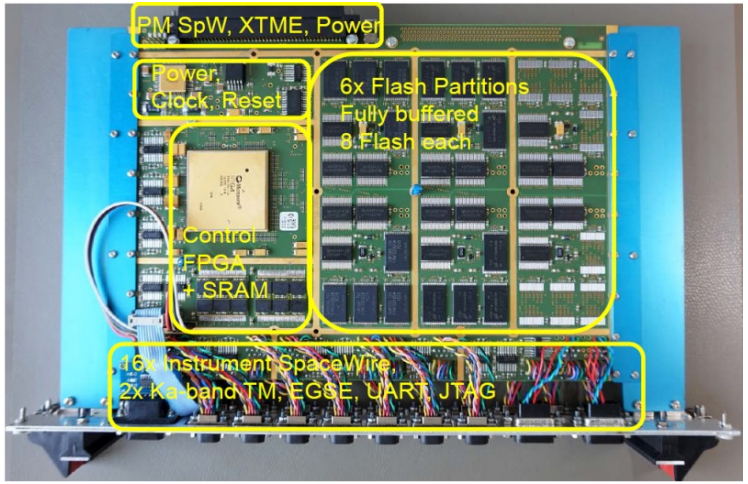
From “Embedded Mass Memory in the On-Board Computer”, Torbjörn Hult et. Al. DASIA 2017.

SAVOIR Avionics Reference Architecture

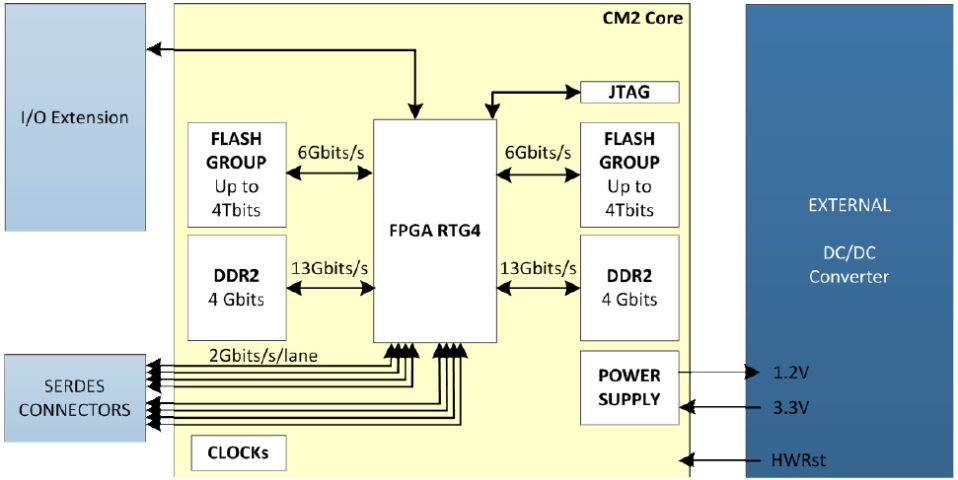


Traditional Avionic Architecture illustrating separate payload and platform data storage functions.

SSMM Architecture



JUICE SSMM architecture from “Embedded Mass Memory in the On-Board Computer”, Torbjörn Hult et. Al. DASIA 2017.



SSMM Architecture from “SpaceFibre based Mass Memory”, Richard Wiest et. al. SpW conference 2018.

Major SSMM building blocks

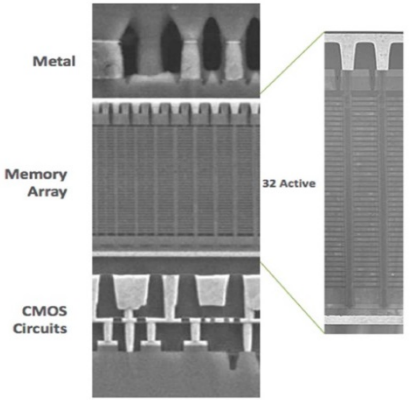
- The SSMM may be divided in the following major blocks such as:
    1. System control block. The system control block may consists of an FPGA performing the supervisory function of the SSMM and handling high speed communication to and from the storage blocks.
    2. Large capacity memory block: Contains memory banks for instrument and platform related data (could be FLASH - COTS).
    3. Buffer memory block: High speed memory utilised as buffer for large capacity memory storage block(fast DDR devices - COTS).
    4. I/O links block. Interface to instruments, OBC and TMTC. Instruments with high data throughput require a high speed Serialiser / Deserialiser (SerDes) + protocol (e.g. SpW, SpaceFibre, non-standardised custom).
    5. Power block: Provision of power to SSMM.

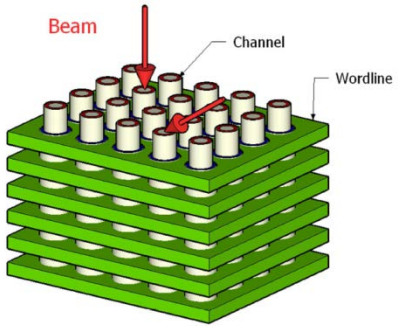
Use of COTS on SSMM (1)

- For large capacity high throughput SSMMs, currently no space qualified large capacity Non Volatile Memory devices are available.
  - SSMMs therefore employ or plan to use COTS FLASH memory devices where development for terrestrial applications is proceeding at high speed.
  - The technology has reached 10 nm in production (SAMSUNG, INTEL, MICRON). Expected shrink timeline (x2 every 3 years per original version of Moore's law), has recently been accelerated (for NAND FLASH) to a factor of 2 every 2 years.
  - As the feature size of cells reach the limit further density increases will be driven by wider levels of MLC and 3-D stacking.
  - The decrease in endurance and increase in uncorrectable bit error rates that accompany feature size shrinking shall then be compensated by improved error correction mechanisms.

Use of COTS on SSMM (2)

- Use of COTS in any space system has to be carried out with great care with considerations made both at component and system level.
  - At component level rigorous screening is required to asses component suitability for flight in it specific application (in some cases components not testable). This goes hand in hand with the necessity of traceability information. Cost of ownership important.
  - At system level particularities of COTS components shall be properly mitigated to meet system reliability and availability requirements (e.g. EDAC, stringent redudency requirements, change of operational conditions, etc.).
- FLASH memories (as for DDRs) are associated with complex radiation and aging related effects requiring comprehensive characterisation. Future 3D FLASH potentially represent great leap in capacity for SSMM. However, with multilevel cell die achieving 256Gbyte per die the associated problems may be exacerbated.
- Future advanced, COTS technologies may also increase system level efforts to develop reliable SSMMs.





"Effects of Heavy-Ion Irradiation on Vertical 3-D NAND Flash Memories", M. Bagatin et.al. IEEE Trans.NUC. SCI, VOL. 65, NO. 1, JANUARY 2018

Conclusion

- The SSMM is an important part of the avionics architecture. A desire to combine SSMM and OBC is observed for some applications cases.
- Payload instruments with high data volume at high speed place stringent requirements on SSMMs:
    - Gbit serial links (high speed SerDes) with standardised protocol.
    - Large capacity Non Volatile Memory (e.g. FLASH) + fast buffer memory (e.g. DDR).
- COTS components are necessary in particular for large capacity non volatile memory where Space Qualified alternatives does not exist.
- Utilisation of COTS devices in SSMMs provide improved capabilities but is associated with high cost to ensure suitability for flight. Design mitigation techniques have to be implemented to ensure reliability and availability requirements are reached.